Extending Moore’s Law with Integrated Photonics (and Packaging)

Dr. Nicholas Harris
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Industry-Wide Challenges
Challenges

Chip power is exploding. The death of Dennard scaling\(^1\) is evident. Water cooling is widely deployed. Immersion is up next.

AI will consume 80% of data center power by 2040. Overall data center power usage is growing much slower than AI hardware deployments. Both growth rates are massive.

AI models will be 1000x larger in 2030. Deployed AI models double in size every year. Research models double 6x faster.

Notes
\(^1\)Dennard Scaling [article].
\(^2\)Publicly available data.

Notes
\(^1\)Interpolation based on [EA]. There are estimates from 6% to 35% annual growth rate.
\(^2\)Averaged CAGR over 2026–2040 smoothed down from 35% growth rate from 2026 – 2030. Source: [EA].
\(^3\)Actual data center growth rate is not agreed upon in academia. Source: [OpenAI “AI and Compute” article].
Compute requirements for AI will increase **1000x** over the next decade, conservatively.
Performance and Cost Challenges

Transistor performance improvements are slowing. Compute performance is bound by thermal limitations at the package level.

Chip design cost is exploding. Exponential growth in development costs for creating next-generation processors.
Heterogeneous Integration

Okay, transistors have issues. Let's use packaging to help.

Driven by
- Dev. and wafer cost
- Integration of multiple nodes, IP
- Si-node yield resiliency
- TTM
- Higher memory density (HBM)
- Energy efficiency
- Compute scaling
Chiplet ≠ Monolithic

Bandwidth Requirements

BISECTION BANDWIDTH

MORE HOPS, MORE ENERGY

SIGNALING SCHEMES

Beachfront and bandwidth are fundamentally linked in chiplet processors. Big chips are at odds with high yield.

Each chiplet hop adds to communications energy consumption. Building large chiplet arrays this way will incur significant energy costs.
Silicon Photonics
300mm CMOS Fab
A Sense of Scale
Optical fibers versus nanophotonic waveguides

127 µm

40X
Interconnect density per waveguide layer.

127 µm
What does silicon photonics look like?
Why bring optics closer to the SoC?
- PCB trace losses too high for long, high-speed links
- Data closer to compute
- Disaggregation
- SoC die sizes max’d out, can’t accommodate large #’s of LR SerDes
- Reduction in interconnect power
- Increased bandwidth over pluggables
- Higher bandwidth density at die edge
- Bypass intermediate stages (PCIe)

Enabling new communications technologies

Gen I
Pluggable Optics

Gen II
On-board Optics

Gen III
2.5D Co-packaged Optics

Optical Links
Electrical Links
Pluggable Optical Transceiver
On-board Optics Module
Disaggregated Laser Supply
Co-packaged PIC

*Used with permission from Dr. John Bowers and adapted from an article in Applied Physics Letters (2021)
Challenges with Silicon Photonics
Optical Fiber Attach

Expensive, low throughput
Optical Fiber Beachfront Density

Fibers are massive

XPU (850mm²)

Max Fiber Count

200
Chiplets and Co-packaged Optics

Scaling challenges

**CHIPLET BISECTION BANDWIDTH**

100 Tbps ≠ 3.2 Tbps

**MORE HOPS, MORE ENERGY**

Each chiplet hop adds to communications energy consumption. Building large chiplet arrays this way will incur significant energy costs.

**CHIPLET XPU & CPO**

- Fibers have low beachfront density
- More wavelengths, more BW
- Static interconnect

Beachfront and bandwidth are fundamentally linked in chiplet processors. Big chips are at odds with high yield.
System Level
Serviceability, manufacturability, yield

CO-PACKAGED OPTICS ALL-ALL
How can we solve these challenges leveraging state-of-the-art packaging technologies?
PASSAGE™
PASSAGE SILICON PHOTONICS & TRANSISTORS

LID

8x CUSTOMER ASICS

FIBER ARRAY

ORGANIC SUBSTRATE
Let’s put it into context

Lightmatter, the next generation

Gen I
Pluggable Optics

Gen II
On-board Optics

Gen III
2.5D Co-packaged Optics

Gen IV
3D Co-packaged Optics

*Used with permission from Dr. John Bowers and adapted from an article in Applied Physics Letters (2021)
Cross Section
Chip-on-wafer Packaging

- Cooling solution depends on tile ASIC TDP.
- Up to 0.9W/mm² via TSVs
# Intra (inside)-System Comparison

<table>
<thead>
<tr>
<th>Communication</th>
<th>Photonic Waveguides</th>
<th>Optical Fibers</th>
<th>Electrical Traces + DAC/AOC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency</td>
<td>SerDes latency (&lt;5ns) + time-of-flight + (possibly FEC)</td>
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</tr>
<tr>
<td>Bandwidth density</td>
<td>200 Tbps/mm</td>
<td>0.2 Tbps/mm</td>
<td>0.02 Tbps/mm</td>
</tr>
<tr>
<td>Max Chip I/O</td>
<td>Area-limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Assuming 1/3 area of 400mm² dedicated to UCle 16GT I/O:</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>~670 Tbps</td>
<td></td>
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<tr>
<td></td>
<td>Shoreline-limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Assuming entire shoreline of 20x4 mm:</td>
<td></td>
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<tr>
<td></td>
<td>80 mm x 0.2 Tbps/mm = 16 Tbps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SerDes compatibility</td>
<td>USR/XSR SerDes</td>
<td></td>
<td>VSR or MR SerDes</td>
</tr>
</tbody>
</table>

**Passage**

**CPO**

**Electrical / Pluggable Optics**
## Inter-System Single-Tile Fiber Export Comparison

<table>
<thead>
<tr>
<th>Communication</th>
<th>Optical fibers via Edge Attach</th>
<th>Optical Fibers</th>
<th>Pluggable Active Optical cables</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Density</td>
<td>Max Tile export, assuming 32 fibers per 20mm edge = 0.72 Tbps/mm 2x4 Passage I/O Fiber Escape for ½ area = 115.2 Tbps * a 1x1 passage tile w/ x32 fibers on 4 edges yields 57.6 Tbps @ 56Gbps modulation and 8 lambda ** 96% fiber yield, via attach redundancy, results in high I/O density (i.e. more fibers v. CPO)</td>
<td>Max Chip I/O for 20mmx20mm (4 edges) = 0.2 Tbps/mm</td>
<td>Max Chip I/O w/ 400G DAC = 20Gbps/mm</td>
</tr>
<tr>
<td>Reach / Ease of scaling out</td>
<td>&lt;1 km via fibers and optically circuit switched. Packet switching capable (more lasers required)</td>
<td>&lt;1 km via fibers</td>
<td>20 cm for VSR, 50 cm for MR; Standard packet switching technology available.</td>
</tr>
<tr>
<td>Fiber Losses</td>
<td>0.2 dB/km</td>
<td>0.2 dB/km</td>
<td>0.2 dB @ 28 GHz (VSR), 40 dB @ 28 GHz (MR), Depends on modulation frequency.</td>
</tr>
</tbody>
</table>

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- **Passage**
- **CPO**
- **Pluggable Optics**

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**NOTE:**
- IMAPS 19th Conference on DEVICE PACKAGING | March 13-16, 2023 | Fountain Hills, AZ USA
- LichtMatter
First Silicon Success

The world's first photonic wafer-scale interconnect

**Passage™ Alpha Silicon**
- <50 Watts
- 32 channels per site, 1.024 Tbps
- 32 Gbps per channel NRZ
- 48 x 800mm² tiles
- 288x 50 mW Lasers
- 6,144 DACs
- 6,144 MZIs
- 150,000 photonic components
- JTAG interface
- Integrated Lasers, transistors, photonics
- Programmable interconnect topologies

Photonic waveguides with ~4 µm pitch.
Solutions LM is Driving

A variety of applications

DISAGGREGATION

MEMORY POOL

ACCELERATOR POOL

MEMORY POOL

DYNAMIC COMPUTE ALLOCATION

& AIR GAP ISOLATION

LESS THAN 1MS LATER

USER 1

USER 2

USER 3

USER 4
Call to Action
Systems and Packaging

- Heterogeneous packaging technologies provide a platform for photonic integration and open opportunities to innovate in:
  - Power delivery
  - Thermal management at package/system level
  - Fiber attach process development to improve throughputs
  - Scaling physical dimensions
- Drive standardization of ecosystem and consolidate supply chain
- Pluggable connectors for fiber attach
Conclusion

Rapid advances in AI and HPC enabled by photonics.

Passage™

3D programmable photonic interconnect that pushes the limits of high bandwidth and low latency... and it makes your deployment simpler.
THANK YOU

Q & A