Driving Adoption of Advanced IC Packaging in Automotive Applications

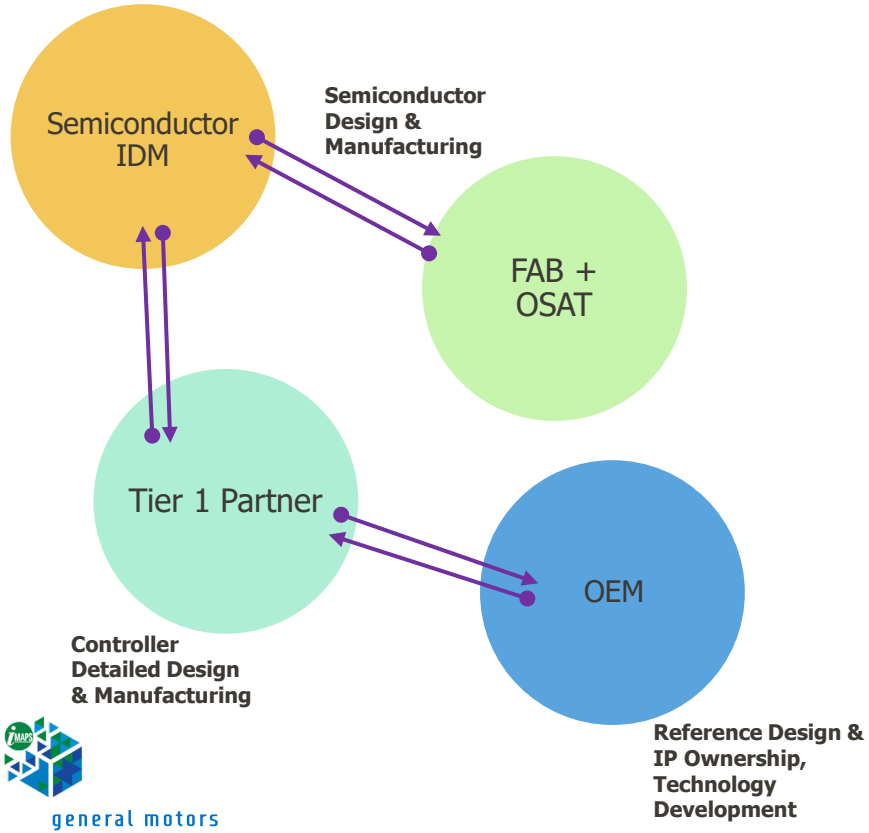
Bassam Ziadeh
Global Technical Specialist
General Motors

Introduction

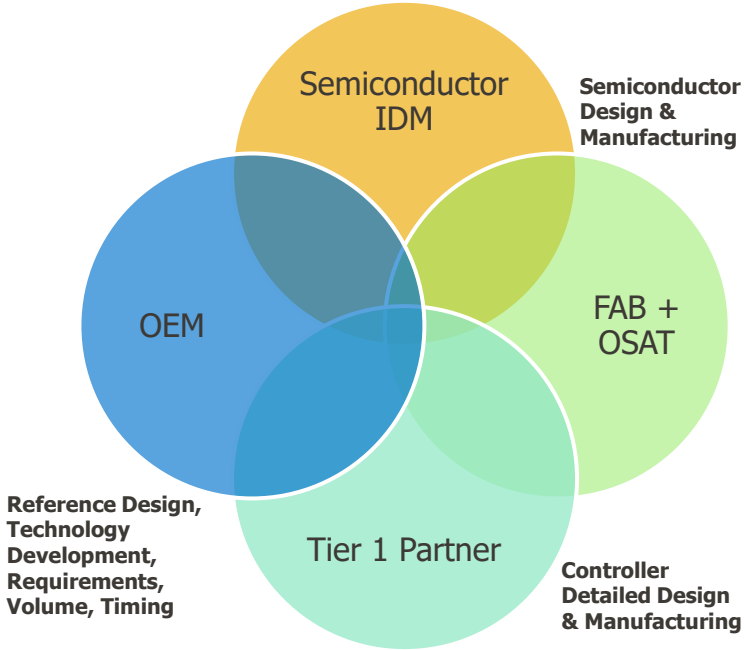
- Shift in Automotive Semiconductor Sourcing
- Importance of Manufacturing On-shoring
- Drivers for Increased Compute Power – ADAS, SDV, & IVI
- Drivers and Pain Points of Advanced Packaging
- Standardization of Chiplets and Advanced Packaging

Evolution of Automotive Semiconductor Supply Chain

Current State of Sourcing – Linear Relationships



Target End State – Fully Integrated Partnerships



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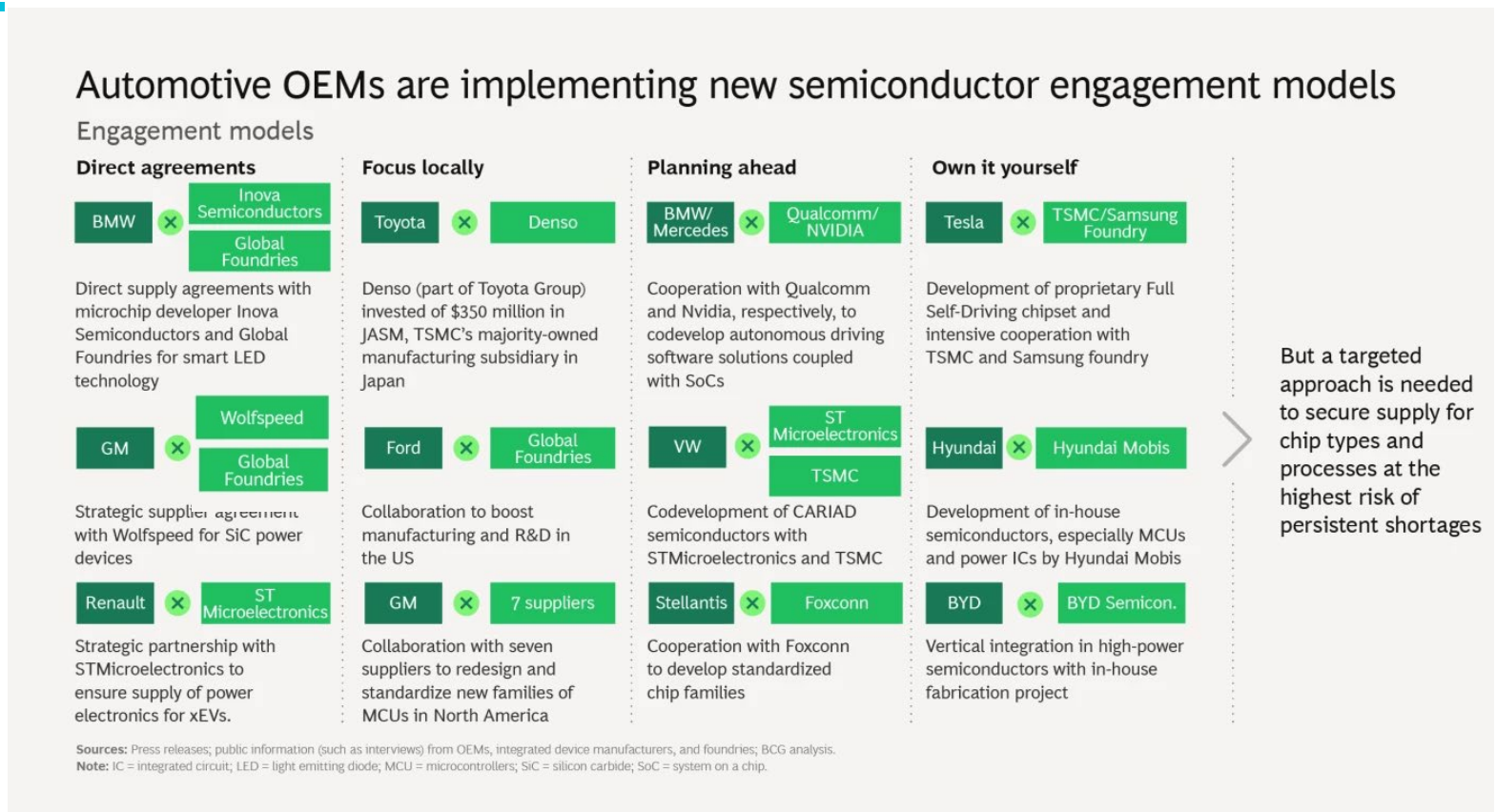
Evolution of Automotive Semiconductor Supply Chain



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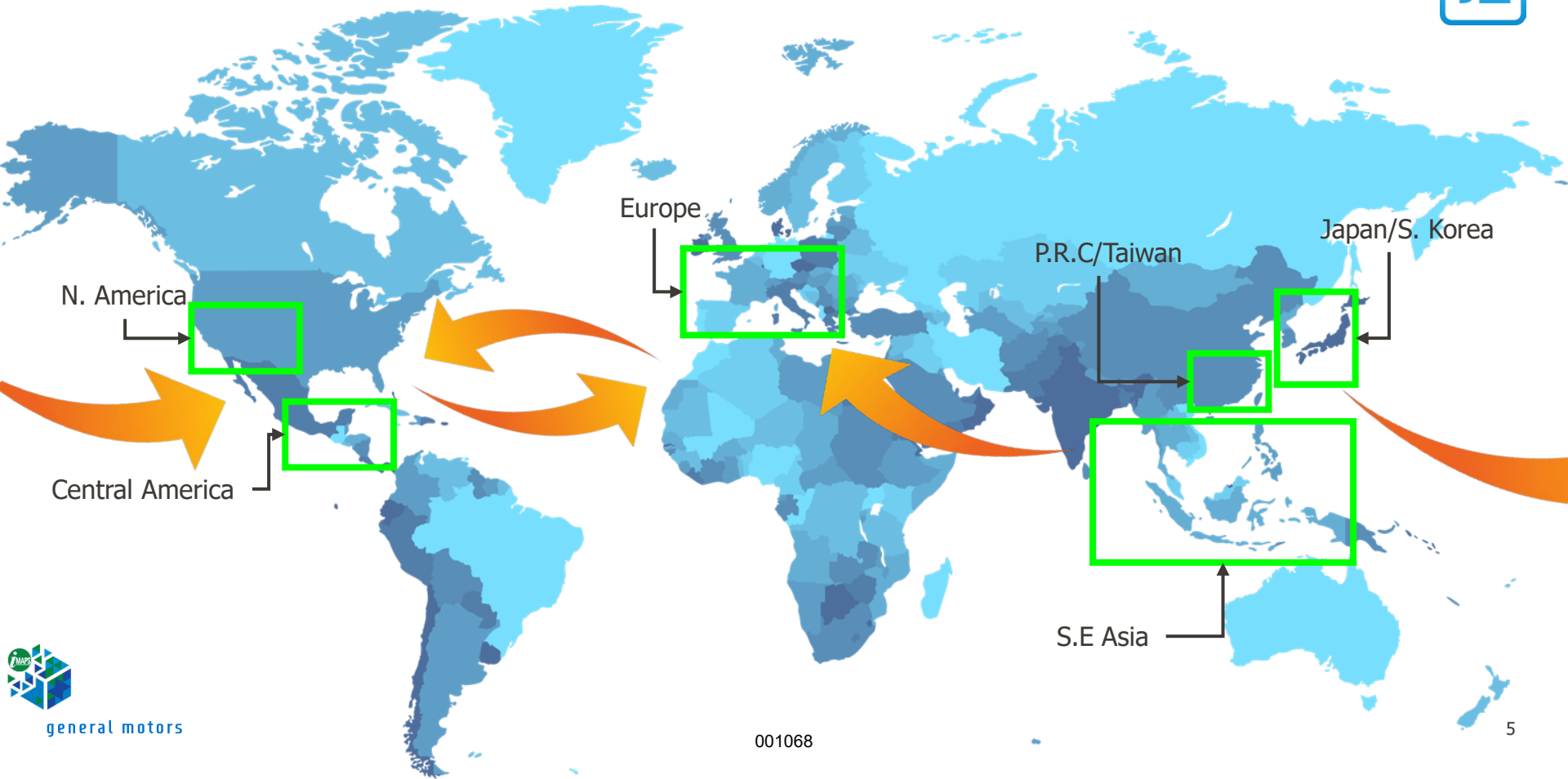
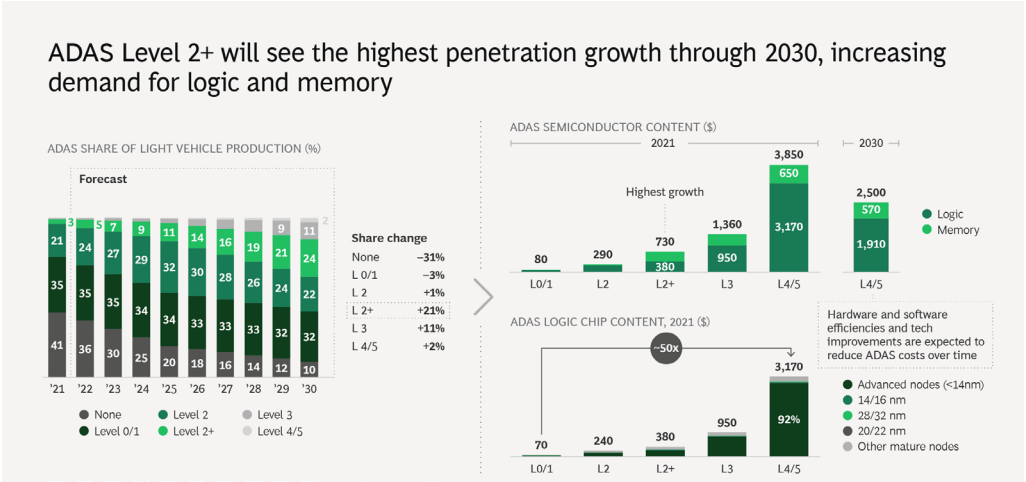
Diversification of Critical Semiconductor Infrastructure

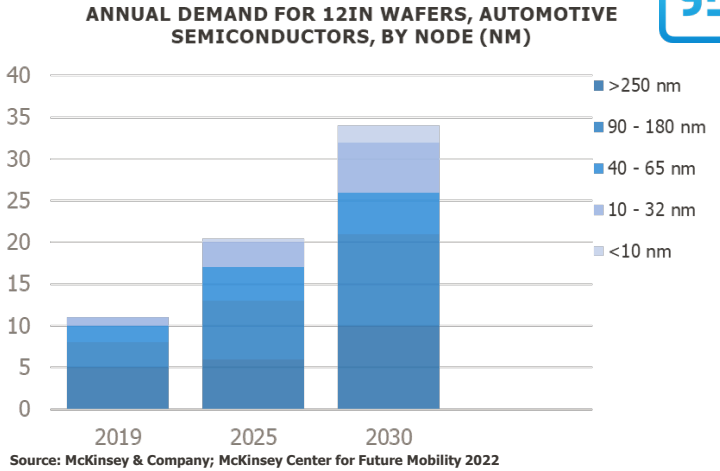


Transition to Modern Si Nodes

- Innovation in Automotives is driving significant uptick in adopting advanced nodes
- Drivers include advancements in ADAS, content rich IVI, and Autonomous driving features (L2+)



Source: Gartner; Strategy Analytics; BCG Analysis.



Source: McKinsey & Company; McKinsey Center for Future Mobility 2022

- Benefits of up-integration of heterogeneous integration drawing interest to advanced packaging
- Advanced nodes providing improved scaling, power consumption, IPs, and access to advances in MCP designs (UCIe, HBM, 2.5D+, MoP, etc)

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Automotive Architecture – Zonal to Centralized SDV

Today's Electrical Architecture

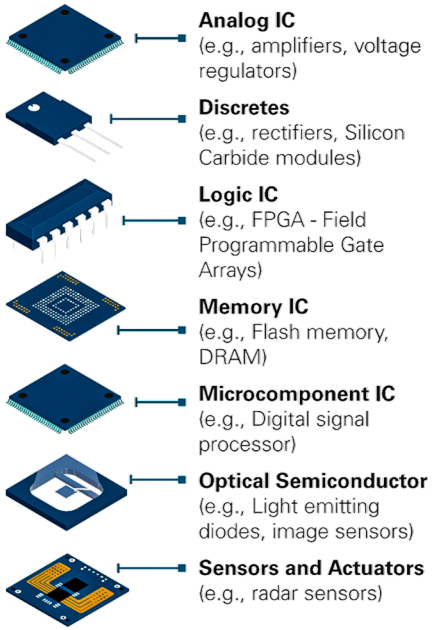
- Highly distributed, unscalable, massive integration required for compute upgrades
- 50+ individual ECU per program, 100's different VIP ECUs
- 70+ Unique MCUs - uncontrolled supply chain
- Single program cost optimized
- Fast time to market, but still limited by architectural constraints

Centralized SDV

- Centralized, highly scalable, upgradable by customers in field
- ~50% reduction in ECU per program
- Semiconductors with 7-year design life, secure supply control
- Enterprise cost optimized, new sales opportunities after SOP
- Industry leading time to market for software development

The Automotive Renascence – SDV, IVI, and ADAS

Products examples



Analog IC
(e.g., amplifiers, voltage regulators)

Discretes
(e.g., rectifiers, Silicon Carbide modules)

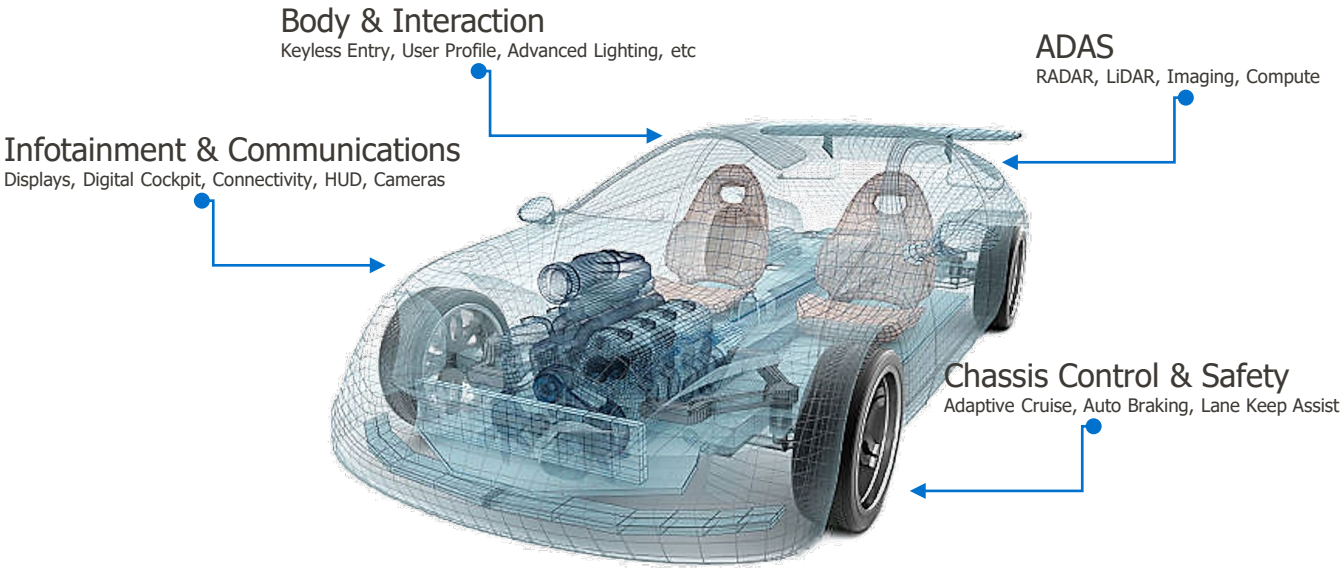
Logic IC
(e.g., FPGA - Field Programmable Gate Arrays)

Memory IC
(e.g., Flash memory, DRAM)

Microcomponent IC
(e.g., Digital signal processor)

Optical Semiconductor
(e.g., Light emitting diodes, image sensors)

Sensors and Actuators
(e.g., radar sensors)



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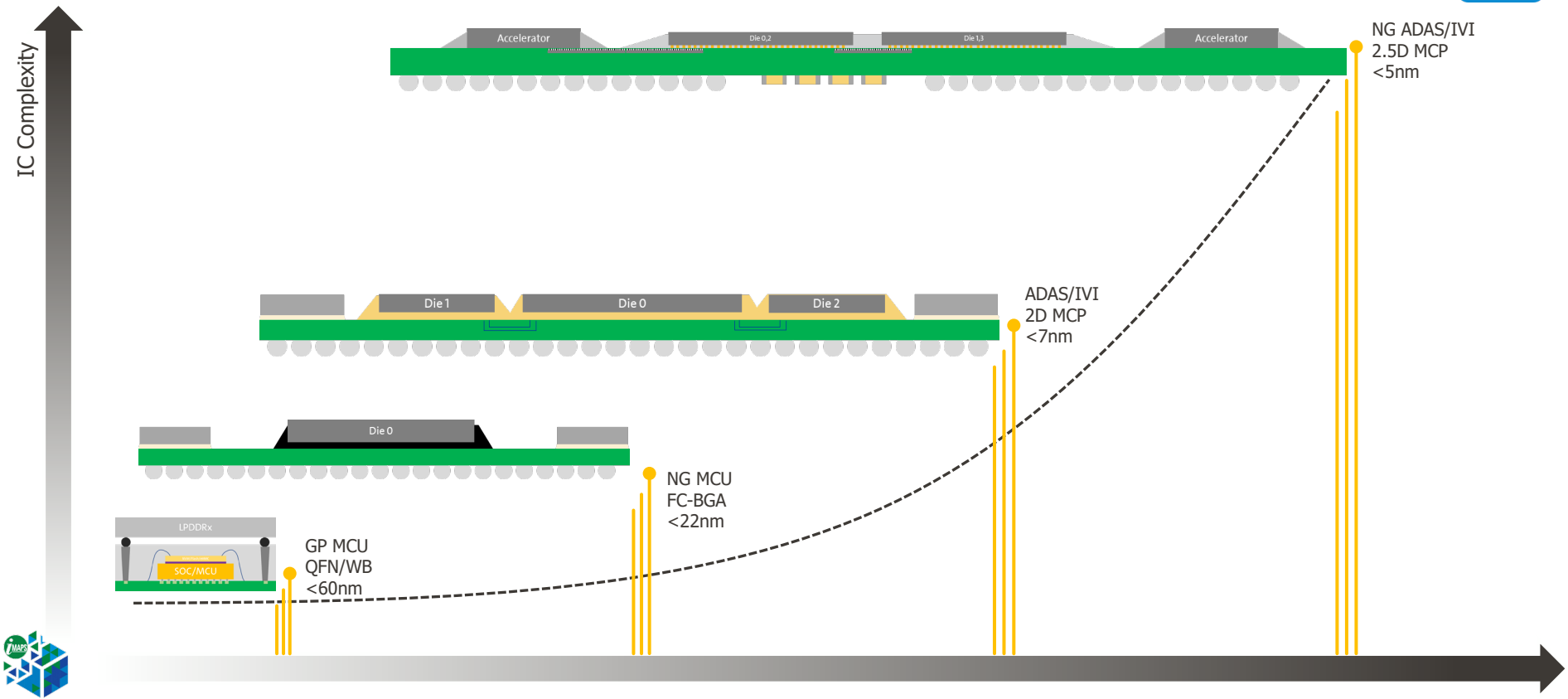
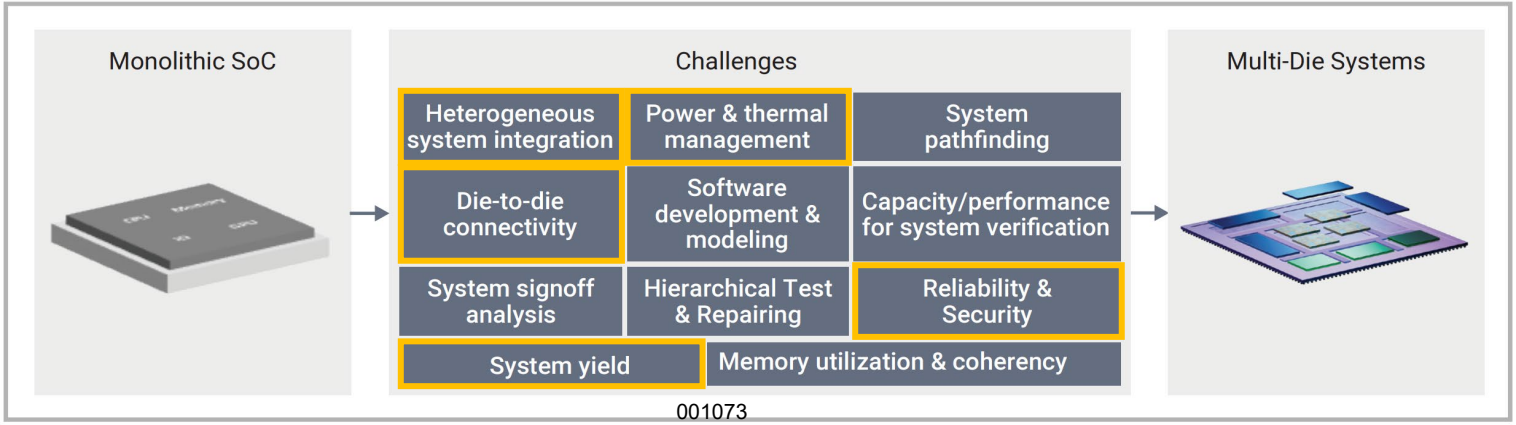
Adoption of Advanced Nodes, IP, and Packaging



Challenges in Adopting Advanced Packaging

- **Benefits of Disaggregated Architectures**
  - Reuse of Specialized IP
  - Improved Yield
  - Optimization of Node Selection
  - Reduced Si Cost
  - Improved Time-to-Market
  - Improved Scalability across vehicle trims/stack

- **Main Challenges to Resolve**
  - Power/Thermal Management
  - Standardizing FF & D2D Communication
  - System Design & Characterization
  - Qualification and Reliability (+ Automotive)
  - Chiplet Compatibility and Integration



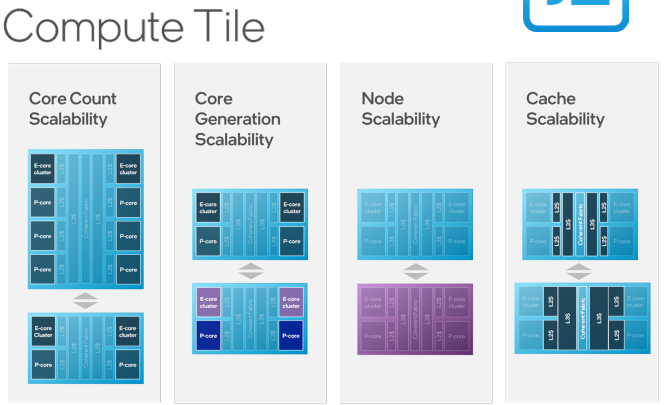
Source: Synopsys; 2023

Drivers in Adopting Advanced Packaging – Chiplet Scaling

- Scalability through entire silicon/trim stack is critical to deployment
  - Reduced BOM cost
  - Predictable performance scaling
  - Optimized Node Selection
  - Improved Time to Market

- Enabling "off the shelf" IP Blocks or **Auto-Ready Chiplets**
  - Reduces qualification time by ensuring reliability
  - Standardized interconnect protocols and packaging requirements
  - Standardized form factors to enable generational refresh with minimal redesign of substrate, bridge/interposer, etc

- Integrating critical Automotive IPs at older nodes
  - SerDes, Memory, NVM/Flash, xPU, Safety Island, XCVR

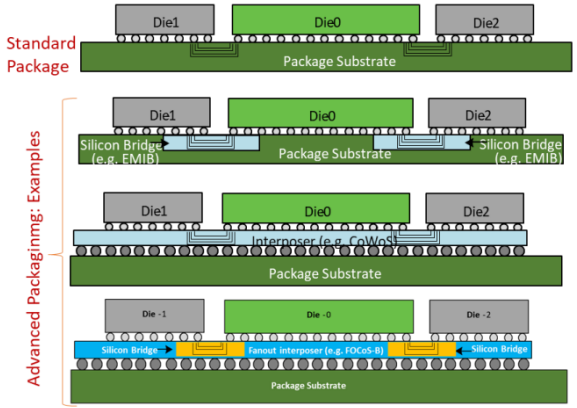


Source: Intel; Hot Chips 2022

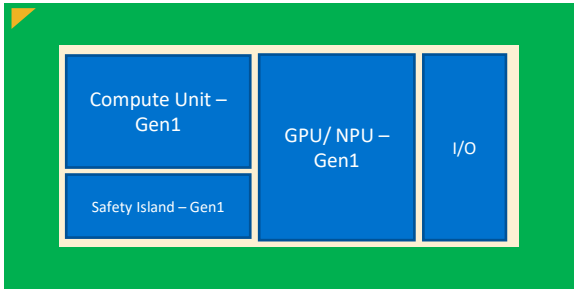
Challenges in Adopting Advanced Packaging – Chiplet Standardization

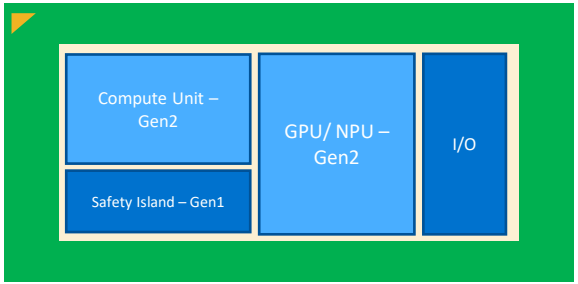
Standardized Protocols & Form Factors

- Concentrated efforts to unify communication protocols (UCIe, ODSA, etc)
- Standardized Form Factors and Bump Maps (similar to JEDEC DRAM) promote intergeneration refresh & enables IP to be provided as OTS chiplets
- Flexible implementation based on bandwidth, latency, and cost
  - EMiB, CoWoS, FOCoS, BoW, etc



(b. Packaging Options: 2D and 2.5D)





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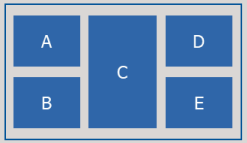
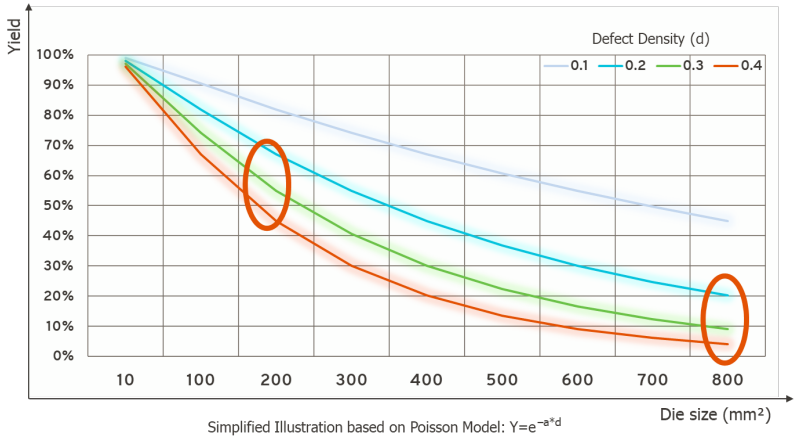
Drivers in Adopting Advanced Packaging –Yield, Cost, & Node Optimization

- Automotive ICs are moving towards advanced nodes for improved performance, advanced IPs, access to on-shored Fabs, and enabling advanced packaging
- Proliferating the use of Known Good Die through singulated die sort/test further improves packaging yield and enables march towards Zero Defect at EOL
- Node Optimization allows for further cost balancing by allowing lower scaling IP (analog) and older IP (Flash, SaIl, etc) to remain optimized on older nodes while critical IP (xPU, Memory, Cache) scale on newer nodes

	5nm Si Node				
	Area	Yield	Cost/KGD	PAT Cost	**Total Cost**
	800mm²	~20%	~$1700	~$150	**~$1850**
	1200mm² (5x200mm²) *Includes D2D I/F	~80%	~$150x5	~$250	**~$1000**

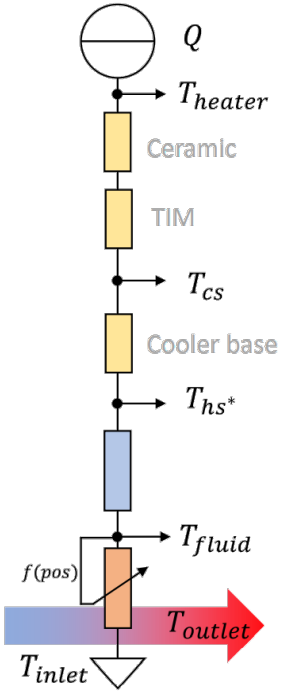
Source: Synopsys; 2023

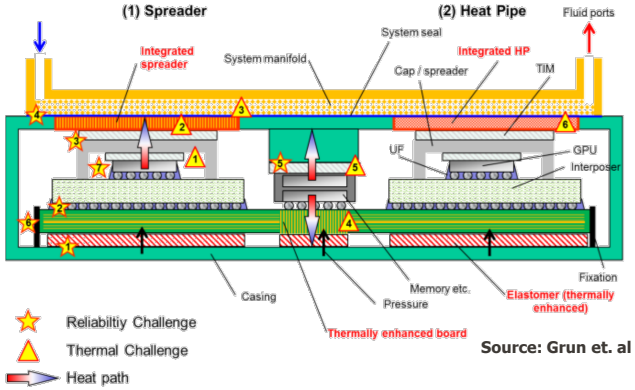


Simplified Illustration based on Poisson Model: $Y=e^{-a*d}$

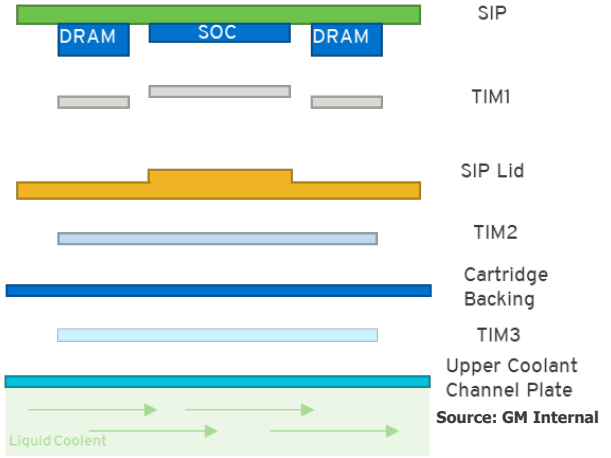
Thermal Solutions for Automotives – TIMs and Liquid Cooling[

- Automotive compute is transitioning to central ECUs and leveraging liquid cooling
- Ambient requirements transitioning to Auto Grade 1; relaxing REL requirements
- TIM development (TIM1 and TIM2) needed to ensure optimal Tjc
  - How do we move metal-based and carbon-based TIMs into Auto qual
- Development on liquid compositions and cold plate designs (direct liquid contact, optimized block designs, additive mfg)





Source: Grun et. al IEEE



Source: GM Internal

Closing Remarks

- Automotive Industry is going through a shift in sourcing, compute requirements, and engagement
- Development of advanced packaging with Automotive Deployment in Mind
  - "Data Centers on Wheels" needs Data Center development
- Emergence of Advanced Packaging and Heterogeneous Integration critical to scaling and deployment
- Standardized D2D Protocols enabling various fab nodes mission critical

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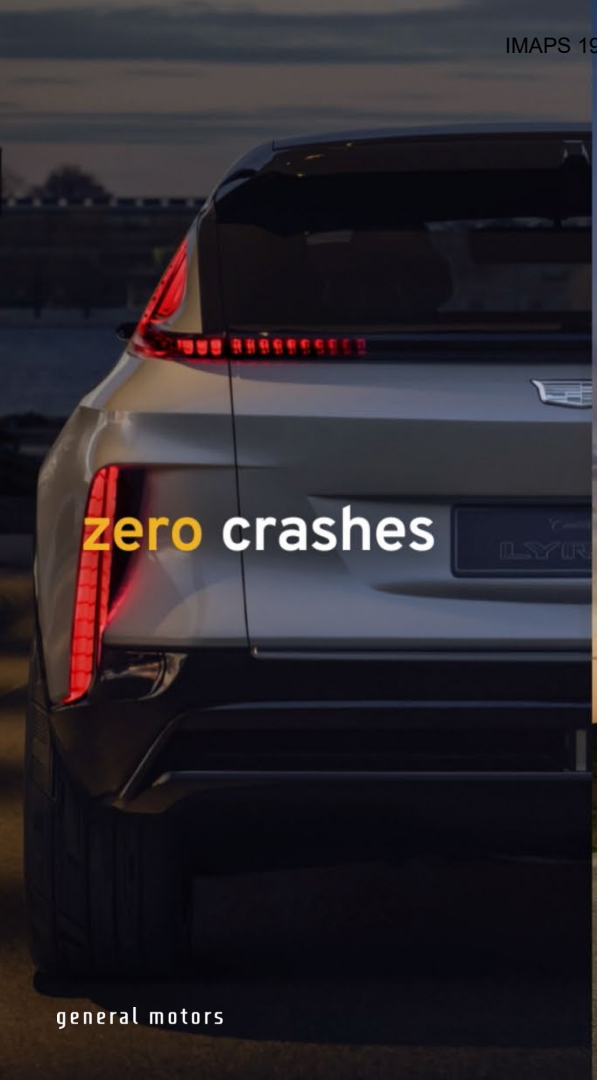
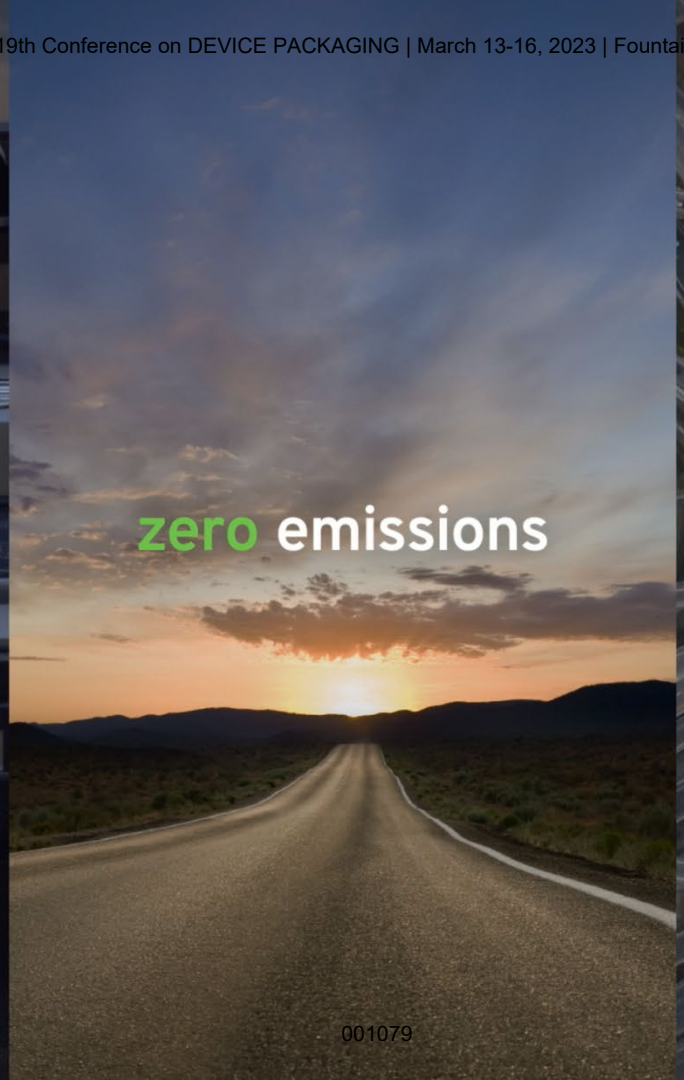
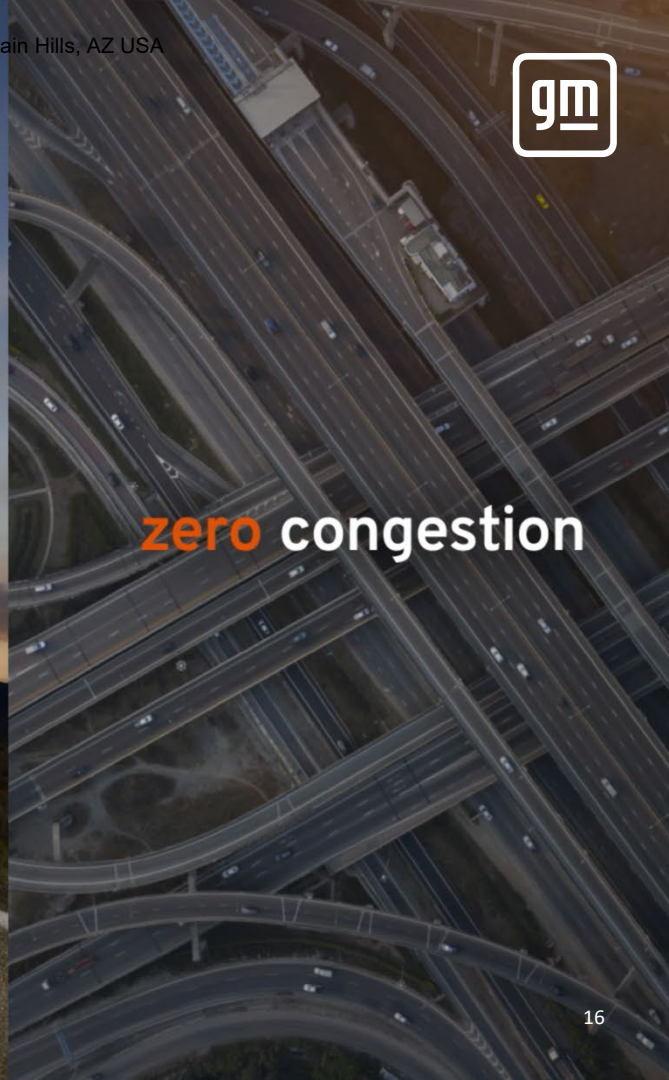

zero crashes


zero emissions


zero congestion

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Challenges in Adopting Advanced Packaging - Thermals

Warpage

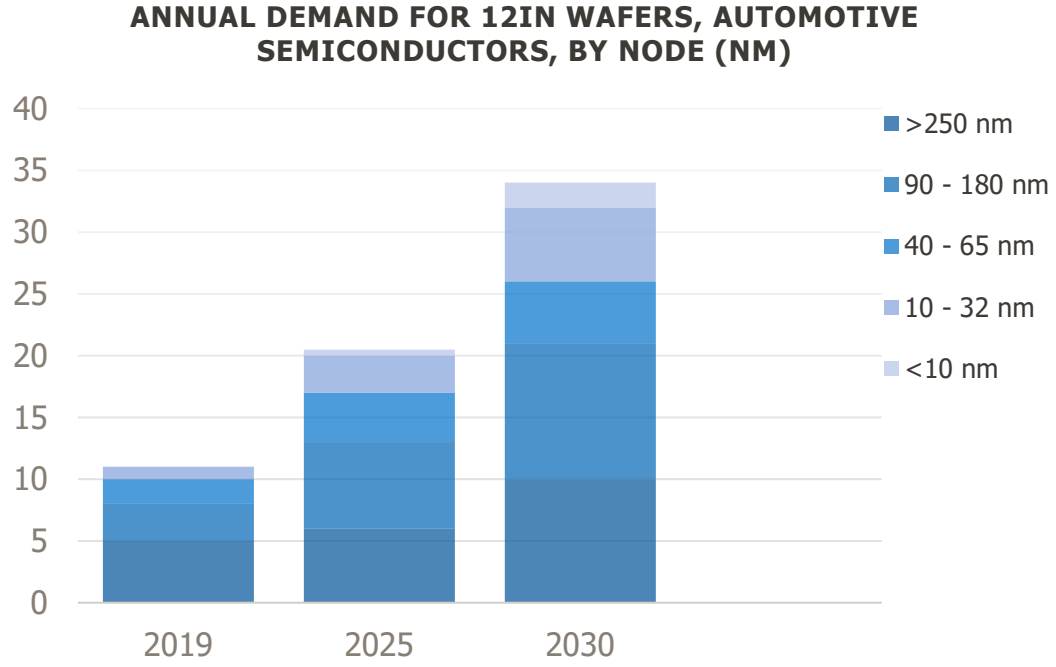
- Improved monitoring of package

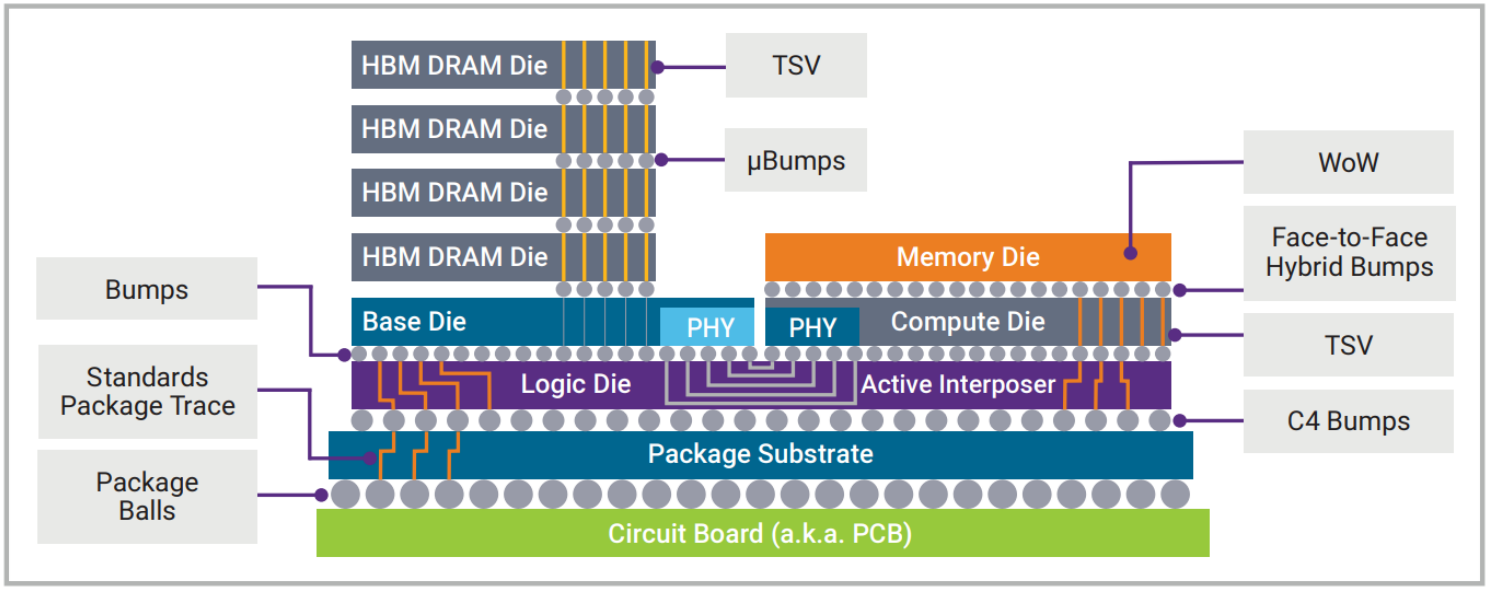
- Material Development

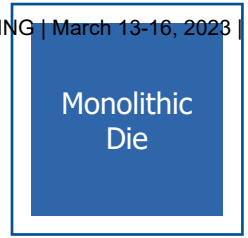
- System Interactions

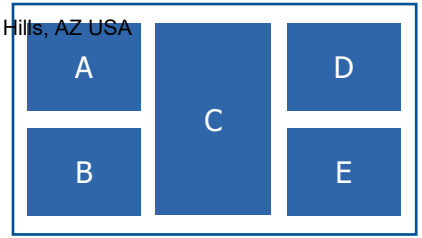
Presentation Overview

- Overview of Automotive Semiconductors
  - Types of Semiconductors and Classifications
- Changes to Automotive Supply Chains
  - ~~Changes in strategic partnerships~~
  - Transition to Newer Nodes as Legacy Nodes drop Capacity
  - ~~Onshoring of Fab and Packaging~~
- Transition from Zonal to Centralized Software Defined Vehicles
  - ~~Image of Zonal vs Centralized E/E Architecture~~
- What's Driving the Automotive Semiconductor Renaissance
  - ADAS; IVI; Communication
  - ~~Transition to newer nodes; adopting advanced packaging for improved performance~~
- Challenges to Adopting Advanced Semiconductors
  - Packaging
  - Thermals
  - Qualification
  - ~~Scalability~~


ANNUAL DEMAND FOR 12IN WAFERS, AUTOMOTIVE SEMICONDUCTORS, BY NODE (NM)
40
35
30
25
20
15
10
5
0
2019
2025
2030
>250 nm
90 - 180 nm
40 - 65 nm
10 - 32 nm
<10 nm


HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
TSV
µBumps
WoW
Face-to-Face Hybrid Bumps
Memory Die
Bumps
Base Die
PHY
PHY
Compute Die
TSV
Standards Package Trace
Logic Die
Active Interposer
C4 Bumps
Package Substrate
Package Balls
Circuit Board (a.k.a. PCB)





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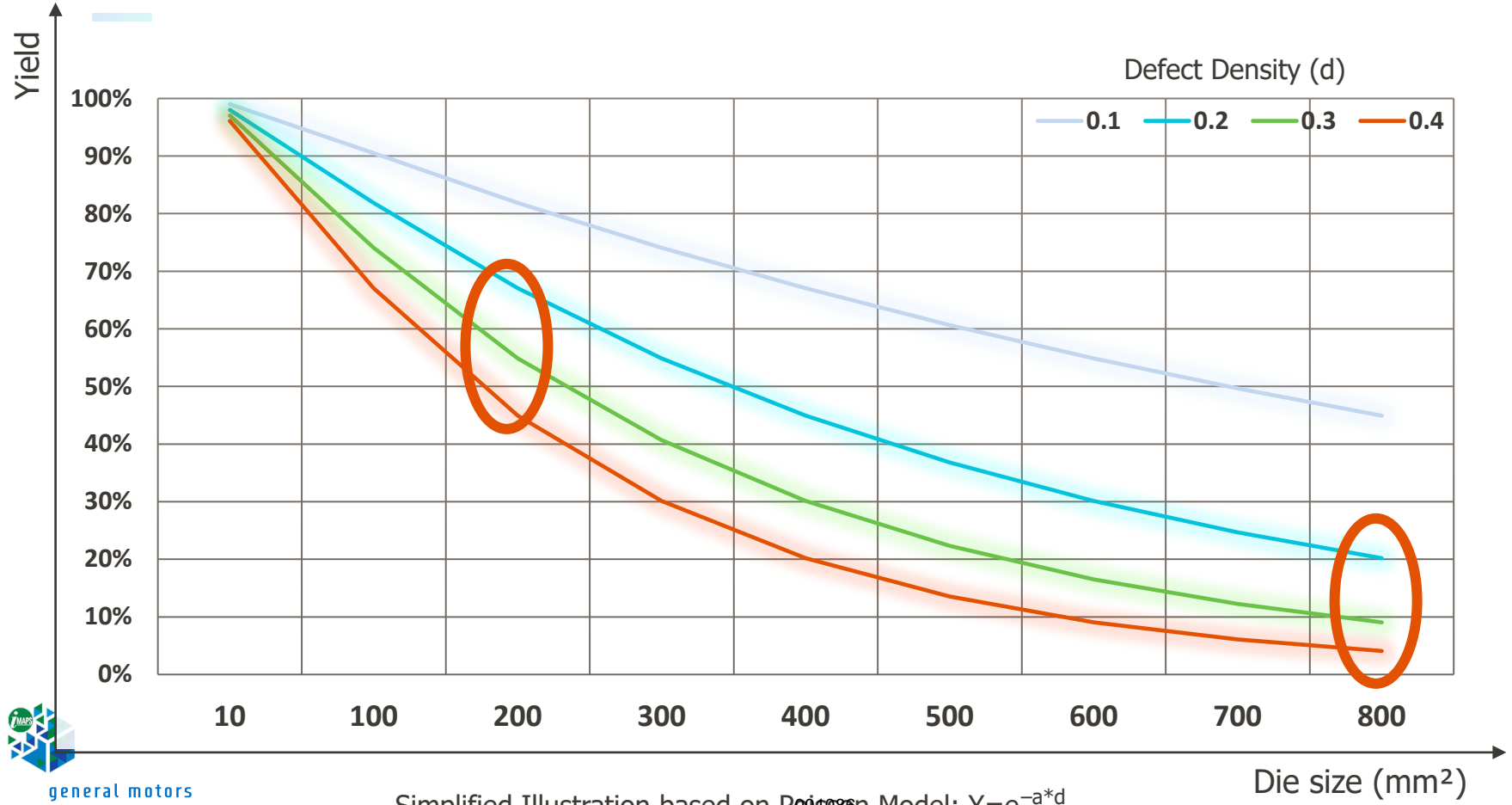

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