Driving Adoption of Advanced IC Packaging in Automotive Applications

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General Motors
Introduction

• Shift in Automotive Semiconductor Sourcing
• Importance of Manufacturing On-shoring
• Drivers for Increased Compute Power – ADAS, SDV, & IVI
• Drivers and Pain Points of Advanced Packaging
• Standardization of Chiplets and Advanced Packaging
Evolution of Automotive Semiconductor Supply Chain

Current State of Sourcing – Linear Relationships

- Semiconductor IDM
- FAB + OSAT
- Tier 1 Partner
- OEM

Controlled Design & Manufacturing
Reference Design, Technology Development, Requirements, Volume, Timing

Target End State – Fully Integrated Partnerships

- Semiconductor IDM
- FAB + OSAT
- Tier 1 Partner
- OEM

Controlled Design & Manufacturing
Reference Design, Technology Development, Requirements, Volume, Timing
### Automotive OEMs are implementing new semiconductor engagement models

**Engagement models**

<table>
<thead>
<tr>
<th>Direct agreements</th>
<th>Focus locally</th>
<th>Planning ahead</th>
<th>Own it yourself</th>
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</thead>
<tbody>
<tr>
<td>BMW</td>
<td>Toyota</td>
<td>BMW/Mercedes</td>
<td>Tesla</td>
</tr>
<tr>
<td>Inova Semiconductors</td>
<td>Denso</td>
<td>Qualcomm/NVIDIA</td>
<td>TSMC/Samsung Foundry</td>
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<tr>
<td>Global Foundries</td>
<td>Denso (part of Toyota Group)</td>
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<tr>
<td></td>
<td>Invested $350 million in JASM, TSMC’s majority-owned manufacturing subsidiary in Japan</td>
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<tr>
<td>GM</td>
<td>Ford</td>
<td></td>
<td>Tesla</td>
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<tr>
<td>Global Foundries</td>
<td>Collaboration to boost manufacturing and R&amp;D in the US</td>
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<tr>
<td>Renault</td>
<td>GM</td>
<td></td>
<td>Hyundai</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>7 suppliers</td>
<td></td>
<td>Hyundai Mobis</td>
</tr>
<tr>
<td></td>
<td>Collaboration with seven suppliers to redesign and standardize new families of MCUs in North America</td>
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<td></td>
<td></td>
<td>Codevelopment of CARIAD semiconductors with STMicroelectronics and TSMC</td>
<td>Development of In-house semiconductors, especially MCUs and power ICs by Hyundai Mobis</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cooperation with Foxconn to develop standardized chip families</td>
<td>Vertical integration in high-power semiconductors with In-house fabrication project</td>
</tr>
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</table>

**But a targeted approach is needed to secure supply for chip types and processes at the highest risk of persistent shortages.**

**Sources:** Press releases, public information (such as interviews) from OEMs, integrated device manufacturers, and foundries; BCG analysis.

**Note:** IC = integrated circuit; LED = light emitting diode; MCU = microcontrollers; SiC = silicon carbide; SoC = system on a chip.
Diversification of Critical Semiconductors Infrastructure
Transition to Modern Si Nodes

• Innovation in Automotives is driving significant uptick in adopting advanced nodes
• Drivers include advancements in ADAS, content rich IVI, and Autonomous driving features (L2+)

ADAS Level 2+ will see the highest penetration growth through 2030, increasing demand for logic and memory

- Benefits of up-integration of heterogeneous integration drawing interest to advanced packaging
- Advanced nodes providing improved scaling, power consumption, IPs, and access to advances in MCP designs (UCIe, HBM, 2.5D+, MoP, etc)
Automotive Architecture – Zonal to Centralized SDV

**Today’s Electrical Architecture**

- Highly distributed, unscalable, massive integration required for compute upgrades
- 50+ individual ECU per program, 100’s different VIP ECUs
- 70+ Unique MCUs - uncontrolled supply chain
- Single program cost optimized
- Fast time to market, but still limited by architectural constraints

**Centralized SDV**

- Centralized, highly scalable, upgradable by customers in field
- ~50% reduction in ECU per program
- Semiconductors with 7-year design life, secure supply control
- Enterprise cost optimized, new sales opportunities after SOP
- Industry leading time to market for software development
The Automotive Renaissance – SDV, IVI, and ADAS

**Chassis Control & Safety**
- Adaptive Cruise
- Auto Braking
- Lane Keep Assist

**Infotainment & Communications**
- Displays
- Digital Cockpit
- Connectivity
- HUD
- Cameras

**Body & Interaction**
- Keyless Entry
- User Profile
- Advanced Lighting

**ADAS**
- RADAR
- LiDAR
- Imaging
- Compute

**Products examples**
- Analog IC (e.g., amplifiers, voltage regulators)
- Discretes (e.g., rectifiers, Silicon Carbide modules)
- Logic IC (e.g., FPGA - Field Programmable Gate Arrays)
- Memory IC (e.g., Flash memory, DRAM)
- Microcomponent IC (e.g., Digital signal processor)
- Optical Semiconductor (e.g., Light emitting diodes, image sensors)
- Sensors and Actuators (e.g., radar sensors)
Adoption of Advanced Nodes, IP, and Packaging

- **GP MCU**
  - QFN/WB
  - <60nm

- **NG MCU**
  - FC-BGA
  - <22nm

- **ADAS/IVI**
  - 2D MCP
  - <7nm

- **NG ADAS/IVI**
  - 2.5D MCP
  - <5nm
Challenges in Adopting Advanced Packaging

- Benefits of Disaggregated Architectures
  - Reuse of Specialized IP
  - Improved Yield
  - Optimization of Node Selection
  - Reduced Si Cost
  - Improved Time-to-Market
  - Improved Scalability across vehicle trims/stack

- Main Challenges to Resolve
  - Power/Thermal Management
  - Standardizing FF & D2D Communication
  - System Design & Characterization
  - Qualification and Reliability (+ Automotive)
  - Chiplet Compatibility and Integration

Source: Synopsys; 2023
Drivers in Adopting Advanced Packaging – Chiplet Scaling

- Scalability through entire silicon/trim stack is critical to deployment
  - Reduced BOM cost
  - Predictable performance scaling
  - Optimized Node Selection
  - Improved Time to Market

- Enabling “off the shelf” IP Blocks or Auto-Ready Chiplets
  - Reduces qualification time by ensuring reliability
  - Standardized interconnect protocols and packaging requirements
  - Standardized form factors to enable generational refresh with minimal redesign of substrate, bridge/interposer, etc

- Integrating critical Automotive IPs at older nodes
  SerDes, Memory, NVM/Flash, xPU, Safety Island, XCVR
Challenges in Adopting Advanced Packaging – Chiplet Standardization

Standardized Protocols & Form Factors

- Concentrated efforts to unify communication protocols (UCIe, ODSA, etc)

- Standardized Form Factors and Bump Maps (similar to JEDEC DRAM) promote intergeneration refresh & enables IP to be provided as OTS chiplets

- Flexible implementation based on bandwidth, latency, and cost
  - EMiB, CoWoS, FOCoS, BoW, etc

(b. Packaging Options: 2D and 2.5D)
Drivers in Adopting Advanced Packaging – Yield, Cost, & Node Optimization

- Automotive ICs are moving towards advanced nodes for improved performance, advanced IPs, access to on-shored Fabs, and enabling advanced packaging

- Proliferating the use of Known Good Die through singulated die sort/test further improves packaging yield and enables march towards Zero Defect at EOL

- Node Optimization allows for further cost balancing by allowing lower scaling IP (analog) and older IP (Flash, SaIl, etc) to remain optimized on older nodes while critical IP (xPU, Memory, Cache) scale on newer nodes

<table>
<thead>
<tr>
<th>5nm Si Node</th>
<th>Area</th>
<th>Yield</th>
<th>Cost/KGD</th>
<th>PAT Cost</th>
<th>Total Cost</th>
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<tbody>
<tr>
<td>Monolithic Die</td>
<td>800mm²</td>
<td>~20%</td>
<td>~$1700</td>
<td>~$150</td>
<td>~$1850</td>
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<tr>
<td>A, B, C, D, E</td>
<td>1200mm² (5x200mm²)</td>
<td>~80%</td>
<td>~$150x5</td>
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Source: Synopsys; 2023
• Automotive compute is transitioning to central ECUs and leveraging liquid cooling

• Ambient requirements transitioning to Auto Grade 1; relaxing REL requirements

• TIM development (TIM1 and TIM2) needed to ensure optimal $T_{jc}$
  – How do we move metal-based and carbon-based TIMs into Auto qual

• Development on liquid compositions and cold plate designs (direct liquid contact, optimized block designs, additive mfg)
• Automotive Industry is going through a shift in sourcing, compute requirements, and engagement

• Development of advanced packaging with Automotive Deployment in Mind
  – “Data Centers on Wheels” needs Data Center development

• Emergence of Advanced Packaging and Heterogeneous Integration critical to scaling and deployment

• Standardized D2D Protocols enabling various fab nodes mission critical
zero crashes  zero emissions  zero congestion
Challenges in Adopting Advanced Packaging - Thermals

Warpage
• Improved monitoring of package

• Material Development
• System Interactions
Presentation Overview

• Overview of Automotive Semiconductors
  – Types of Semiconductors and Classifications

• Changes to Automotive Supply Chains
  – Changes in strategic partnerships
  – Transition to Newer Nodes as Legacy Nodes drop Capacity
  – Onshoring of Fab and Packaging

• Transition from Zonal to Centralized Software Defined Vehicles
  – Image of Zonal vs Centralized E/E Architecture

• What’s Driving the Automotive Semiconductor Renaissance
  – ADAS; IVI; Communication
  – Transition to newer nodes; adopting advanced packaging for improved performance

• Challenges to Adopting Advanced Semiconductors
  – Packaging
  – Thermals
  – Qualification
  – Scalability
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*Includes D2D I/F*
Simplified Illustration based on Poisson Model: \( Y = e^{-a \cdot d} \)

- Yield vs. Defect Density (d)
- Die size (mm\(^2\))

Graph shows the relationship between yield and die size for different defect densities. The curves represent different values of \( a \) (0.1, 0.2, 0.3, 0.4). Circles indicate specific points of interest.