Defluxing of Copper Pillar Bumped Flip Chips

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- Material Selection
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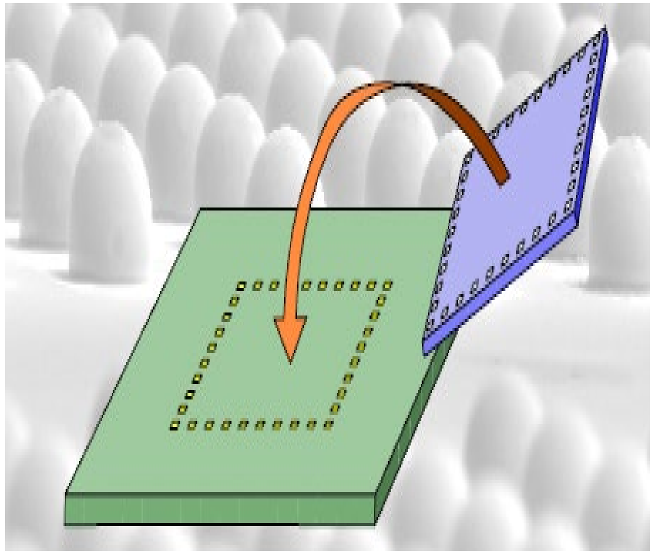
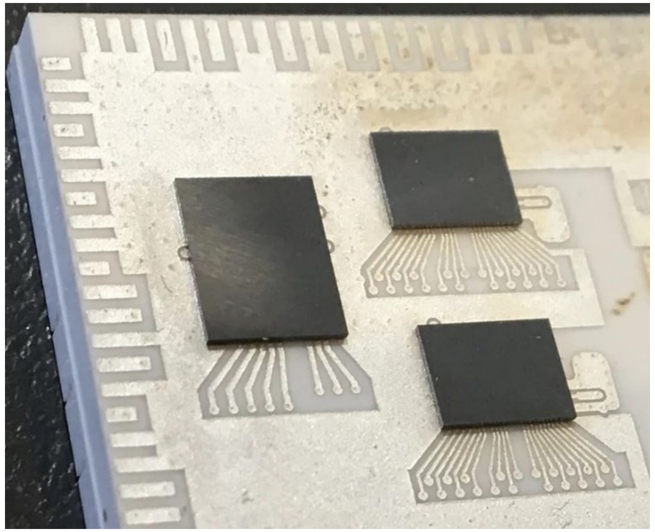
Overview

- Explores impact of flux cleaning using DI-water and well-balanced aqueous cleaning agent on copper pillar bumped flip-chips *(Phase I)*
- Scope of this study is limited to Cu-pillar bumped flip chips having pitch of 150µm and 30µm Cu pillar height
- Results verified via analytical test (IC, SEM/EDS, FTIR) and reliability test methods (TC, HTSL, MSL-3)

Introduction - Flip Chip Assembly

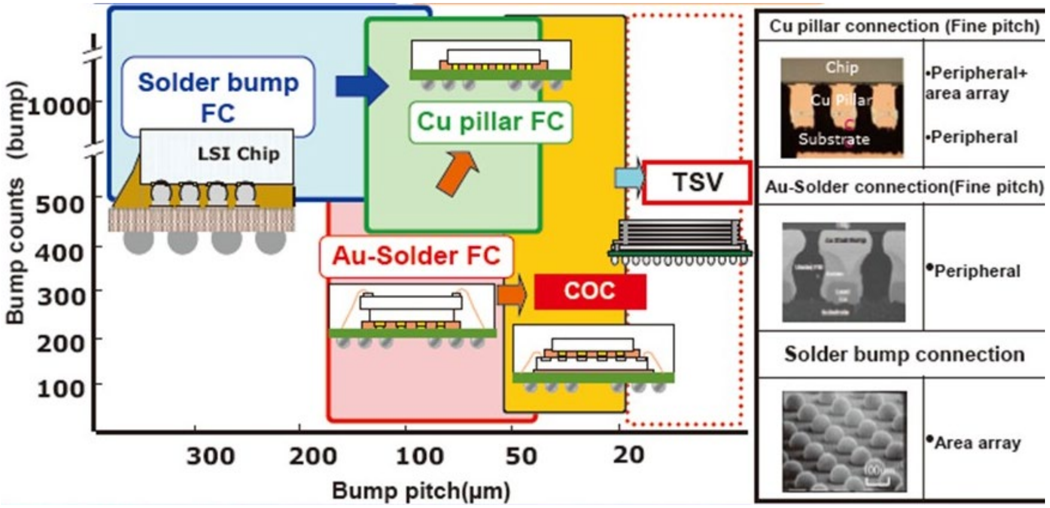
- Method to electrically connect the die to the package carrier
  - The bond wire is replaced with a conductive “bump” placed directly on the die surface
  - Underfill epoxy is used to secure the attachment and absorb stress
  - The chip is then “flipped” face down onto the package carrier using a reflow process
- Flip-chip Technology offers
  - Higher packaging density (more I/Os)
  - Higher performance (lower inductance)
  - Improved circuit reliability
  - Shortest interconnection



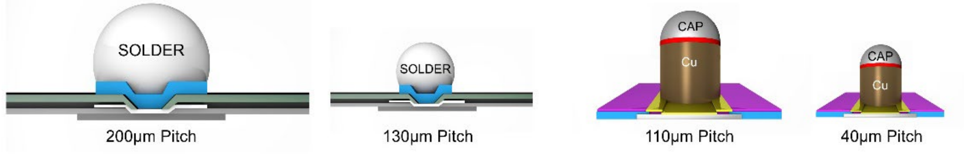


Introduction - Need for Copper Pillar?

- Smaller Pitch
- Solder bump technology is problematic below 150µm pitch to manufacture and assemble
- Excellent heat dissipation ability making them good candidates for microprocessors
- Superior electromigration performance
- Higher I/O density
- Lower cost fine pitch flip chip (FPFC) interconnect versus Au stud bump for high bump density designs



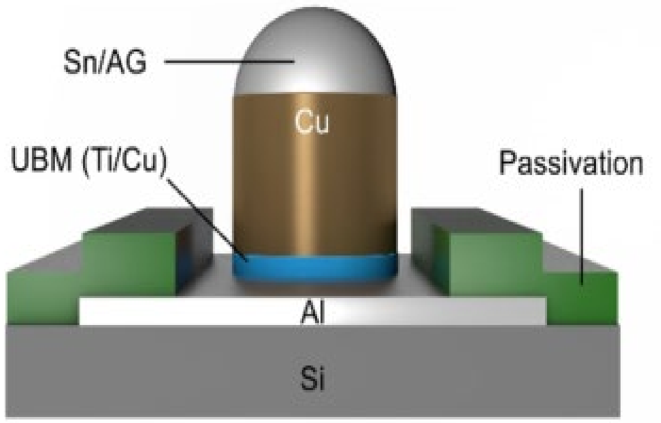
Ref: Renesas, Solid State Technology



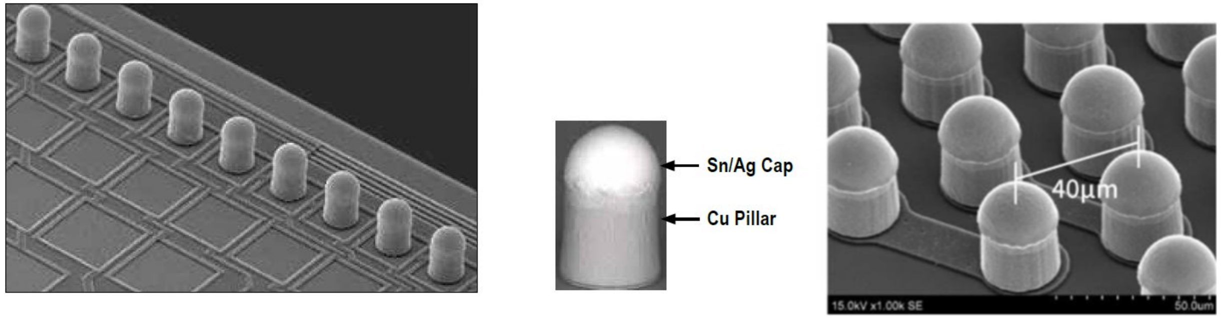
Flip-Chip Bump Miniaturization Typical Data

Introduction - Copper Pillar Typical Structure

- These bumps are in pillar form, with various shapes and sizes
- The pillar shape allows a high ratio of bump height to bump diameter
- Solder cap sometimes is formed on top of the pillar to help with connectivity with the mating chip
- They are formed on aluminum electrode pads of an IC chip



Copper Pillar Bump Typical Structure

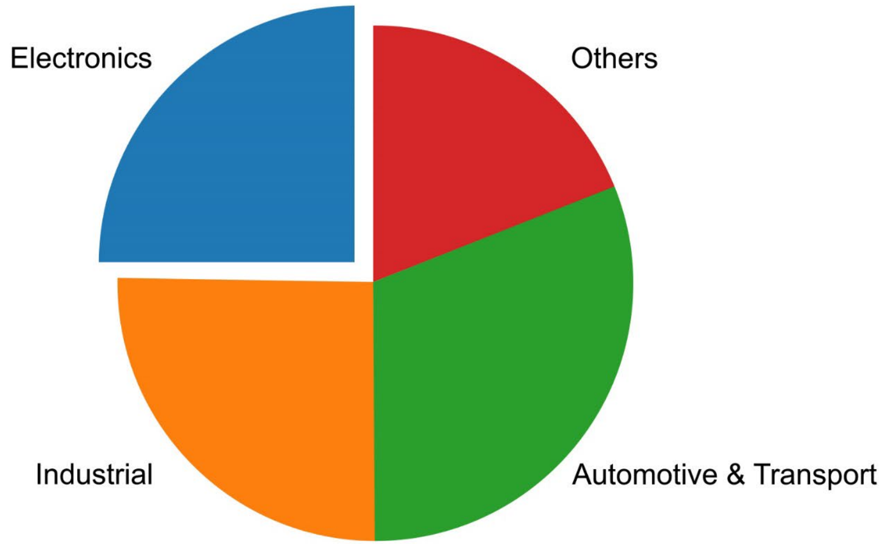


SEM image of Cu-pillar Bumps

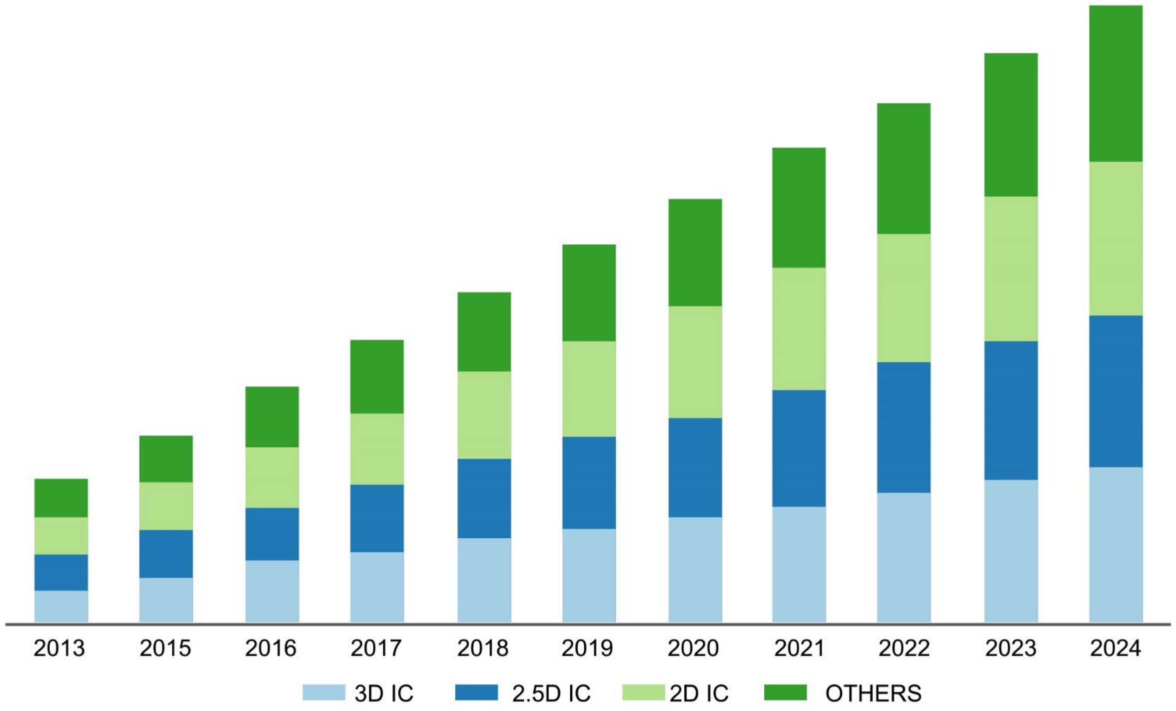
ZESTRON High Precision Cleaning

Introduction – Rapidly Growing Market

Global Copper Pillar Flip Chip Market Report 2019
Market share by application, 2019 (%)
www.marketintellica.com



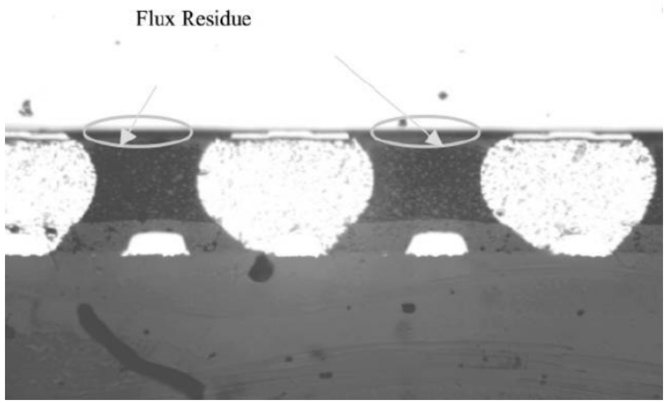
Global Copper Pillar Flip Chip Market Size, by product, 2013-2024 (USD Million)
www.marketintellica.com



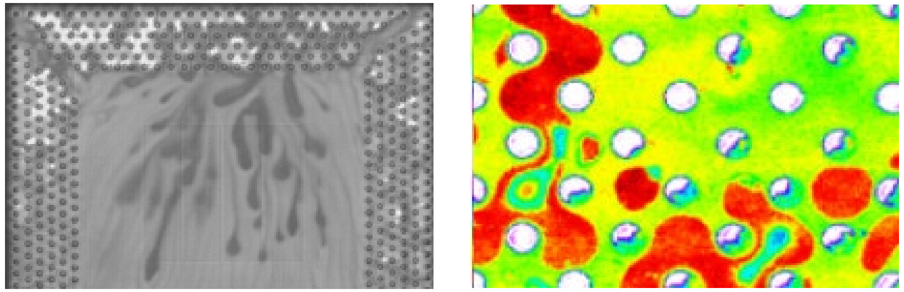
Copper pillar is likely to become the most dominant type of flip-chip interconnect in the coming years

Background - Why Clean Copper Pillar Packages?

- Flux Residues
  - More interconnects / surface area resulting in tighter pitch and lower standoff gaps
    - Less area to outgas during reflow
      - More active residues under the die
  - Can affect reliability two ways:
    - Thin films of residue can reduce interfacial adhesion between the flux and the surfaces on solder bump, substrates or die
    - By impeding the flow of underfill material
      - Encapsulating air and creating a void



2010 Proceedings 60th ECTC Conference

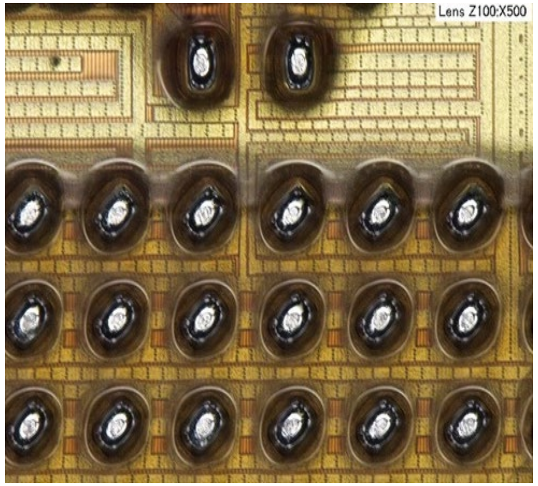


Flip chip underfill voids (red)

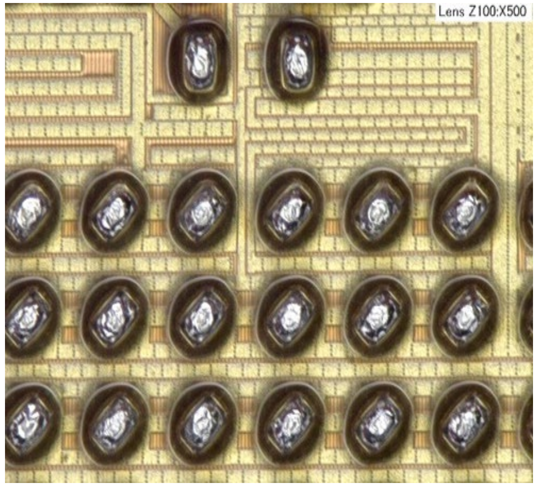
Most Copper pillar applications rely on cleaning with DI-Water only for OA flux removal

Introduction

- Latest advanced packages are trending towards a lower gap
  - Between the stacking chip and include new soldering material
  - To create reliable solder joints
- Flux residues left around the bumps are difficult to remove



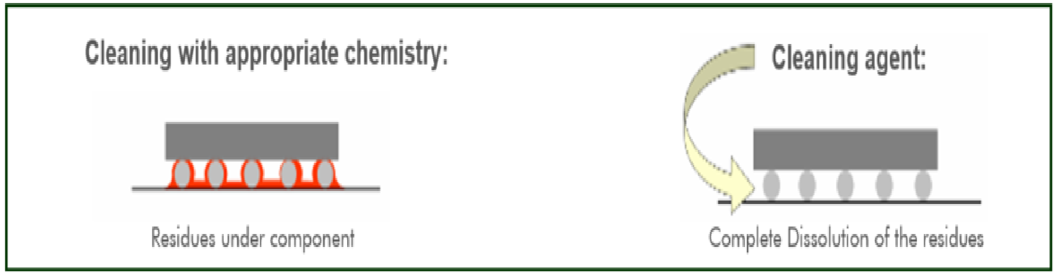
Space between bumps completely filled with flux

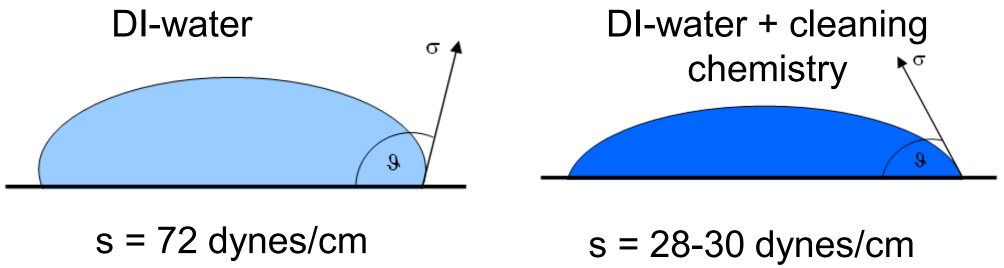


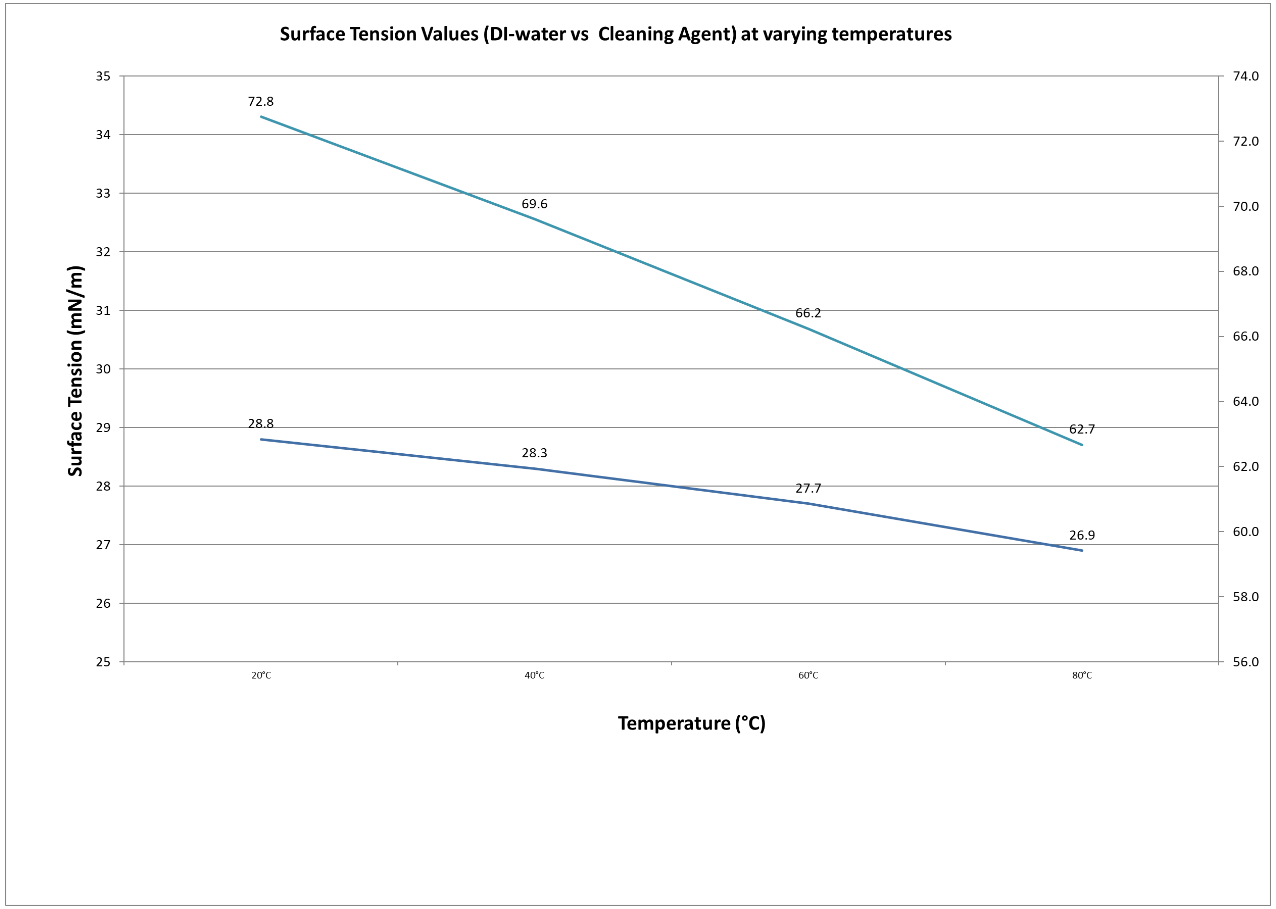
Isolated flux residues around bumps

Background - Limited Solubility in De-ionized Water

- Physical Properties
  - Surface tension, density & viscosity

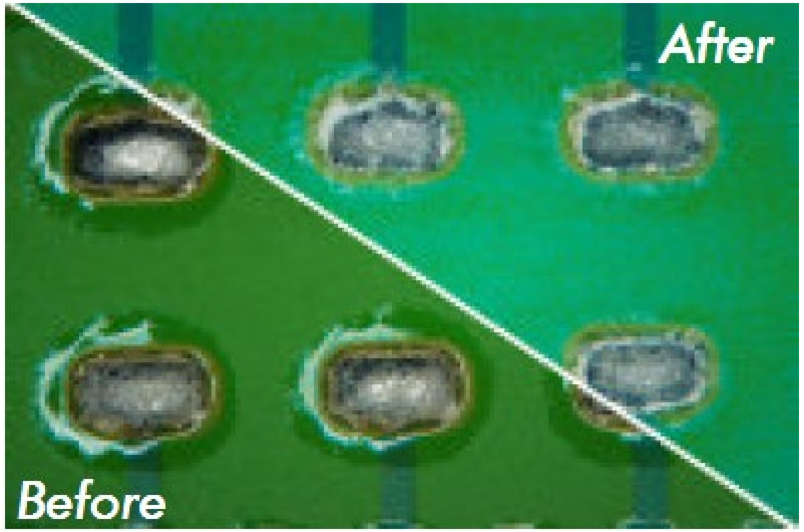


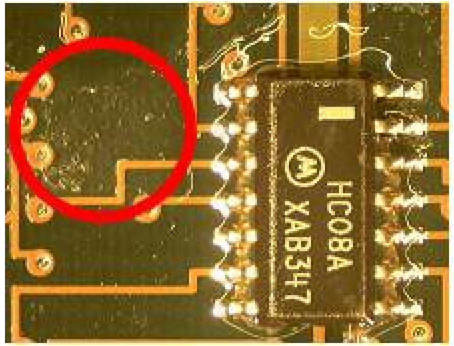




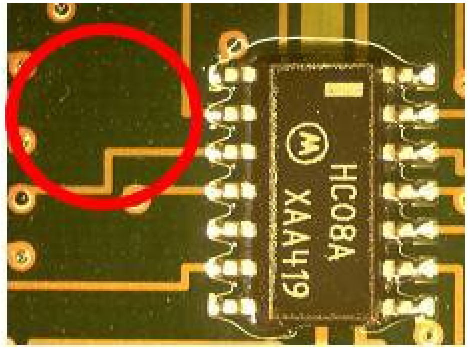
Background - Limited Solubility in De-ionized Water

- Removal challenges due to lack of solvency
  - Higher soldering conditions
    - baked flux residues
  - Increased amount of activators
    - to avoid oxidation at higher temperatures
  - Higher resin content used
    - to achieve low void rate resulting in more residues
- Foaming concerns
  - Frequent interruptions
    - Increased process and utility costs
  - Impact on subsequent processes





DI-water process

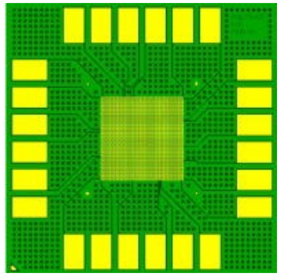


Cleaning agent process

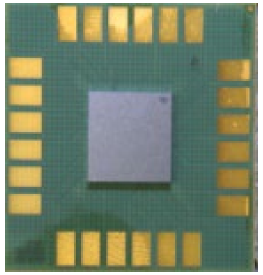
Material Selection

Substrate Specs:

Substrate material	Organic substrate
Thickness	960µm
Core Material	E-679FGR
Solder Resist	PSR4000-AUS703
Function	Daisy-chain
Electrode material	Electroless Ni/Au (ENIG) plating



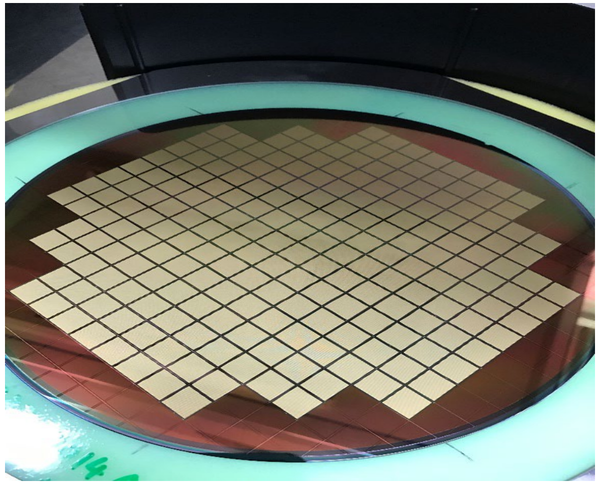
Bare Substrate



Chip Assembled on Substrate

Wafer Specs:

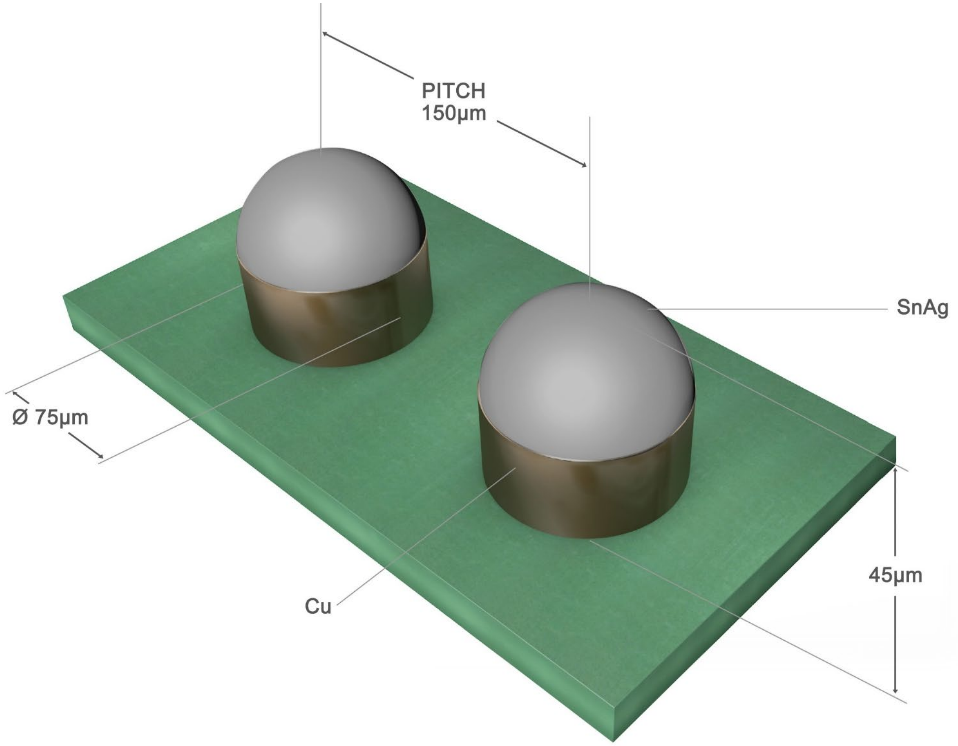
Wafer Composition	Material
Base Oxide Layer	PE-TEOS (poly-tetraethyl orthosilicate)
Metal Layer	TiN / Al-0.5%Cu
Passivation Layer 1	HDP / P-SiN
Passivation Layer 2	-
UBM Layer	TiW/Cu
Bump	Cu/Sn-2.5Ag



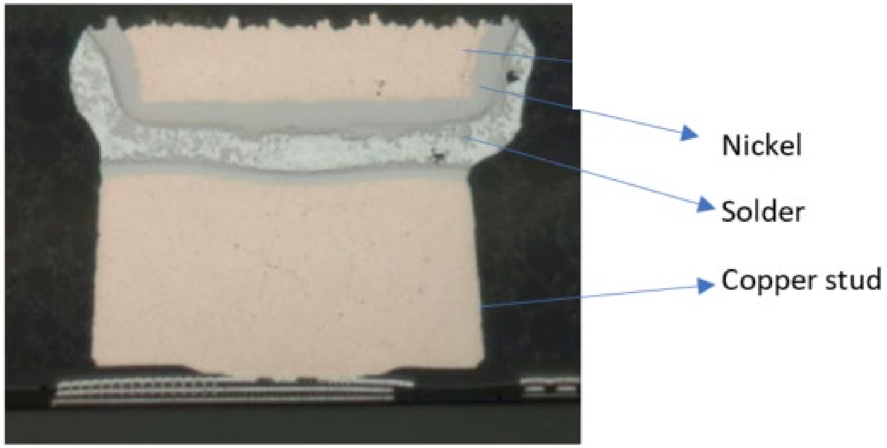
8” wafer

Material Selection

- Flip-chip Specs:
  - Die Size: 10mm x 10mm
  - Number of bumps: 3,721
  - Pitch: 150µm
  - Passivation Opening: Φ 80µm
  - Bump Height: Cu 30µm + SnAg 15µm
  - Bump Diameter: Φ 75µm



Chip Specification



Cross-section of Copper Bump

Material Selection

- Flux Specs:
  - Leading supplier of lead-free water-soluble tacky flux
    - Containing solvent, organic amine, polyoxyethyleneglycol and organic acid
  - Commonly used materials in semiconductor packaging including copper pillar bump applications

Assembly Process

Collaboration with Universal Instruments Advanced Process Lab to assemble and perform reliability testing

- Flux Application
  - Flux Dip Package
  - Using LTFA Technology, on-board dipping process
  - Uses a plate ~ 38 microns thick to create a film
- X-Ray Inspection
  - Post-placement, inspection done to ensure bump is aligned properly to the pad
  - First Article Inspection (FAI) performed on remaining lot and necessary adjustments were carried out

Linear Thin Film Applicator (LTFA)

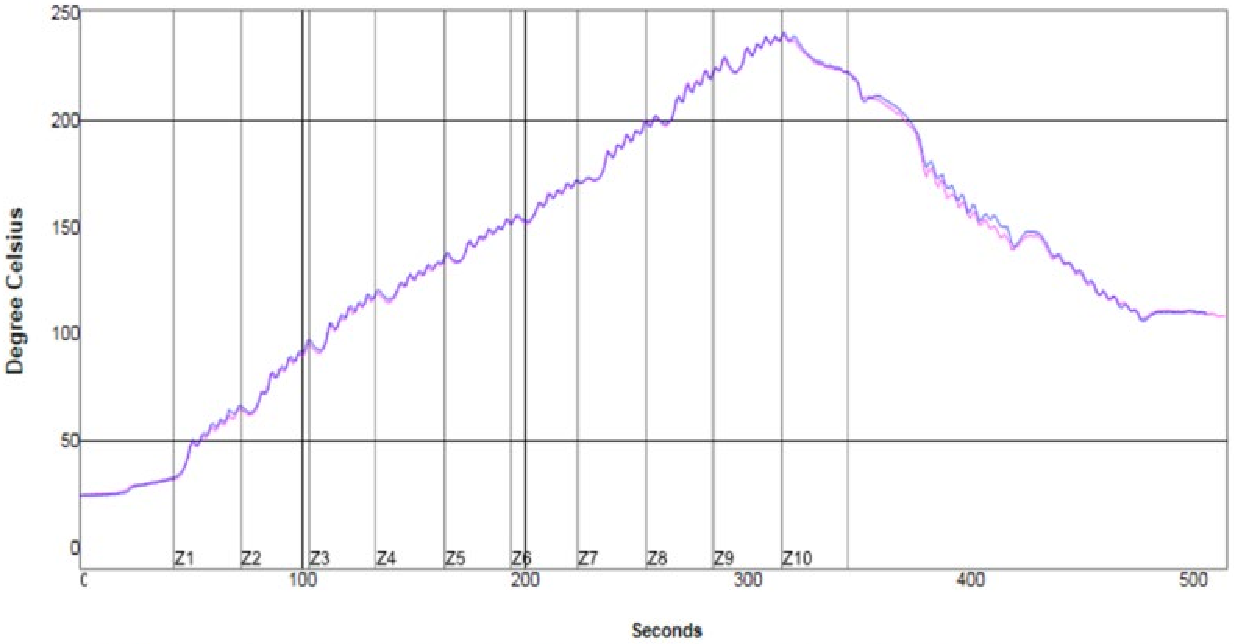
Assembly Process

- Reflow Profile
  - Using lead-free solder profile
  - 10-zone convection reflow oven under nitrogen (< 200 ppm)
  - Peak temperature of 250ºC
  - Controlled heating and cooling rate
    - To achieve optimum bump profile post-reflow
    - To minimize stress on the reflowed bump

Setpoints (Degree Celsius)

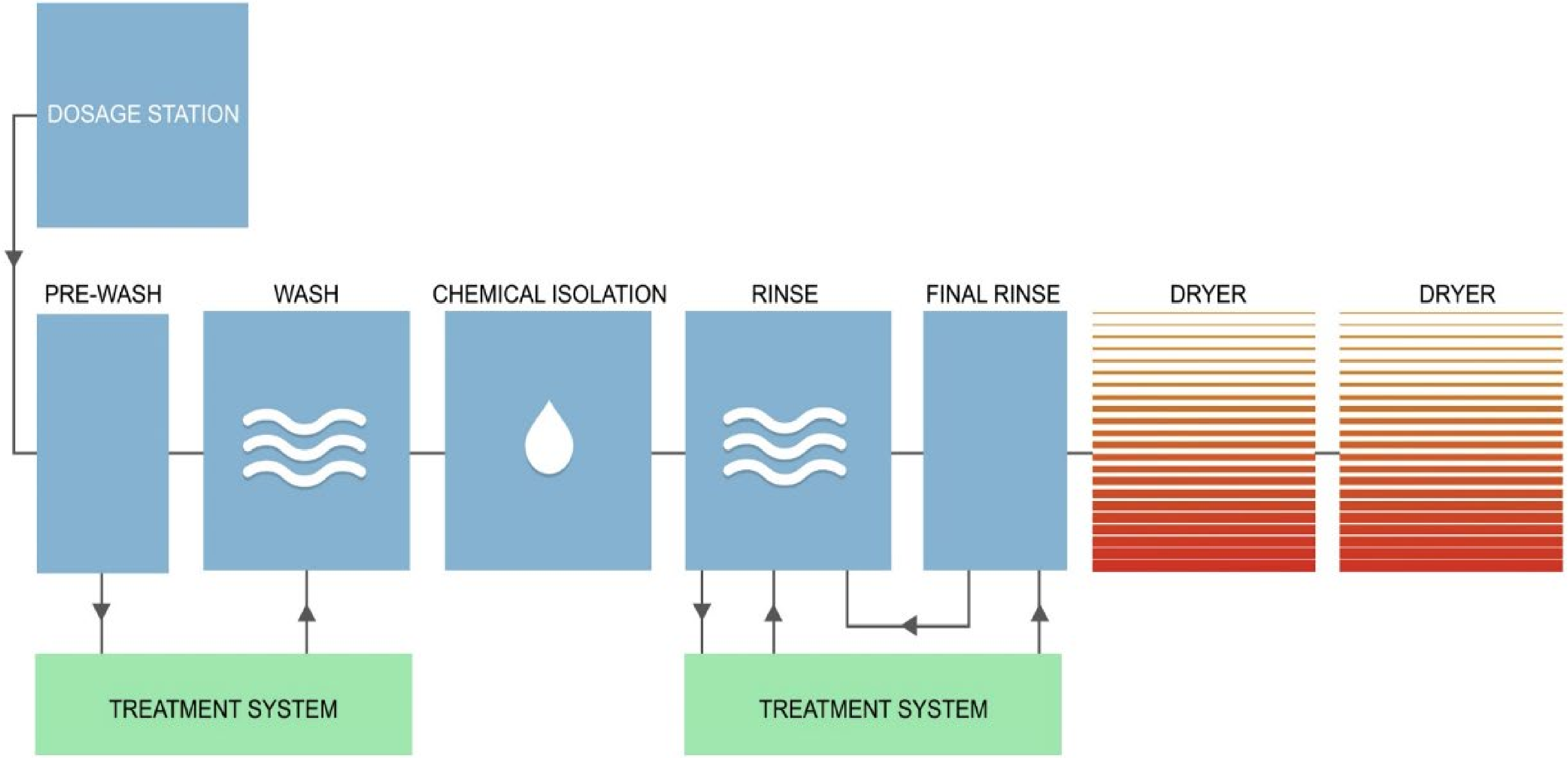
Zone	1	2	3	4	5	6	7	8	9	10
Top	96	132	159	166	187	206	241	274	285	219
Bottom	96	132	159	166	187	206	241	274	285	219

Conveyor Speed (cm/min): 61.8



PWI= 30%	Max Rising Slope		Max Falling Slope		Reflow Time /221°C		Peak Temp	
<TC2>	1.38	17%	-1.92	8%	65.97	30%	240.42	4%
<TC3>	1.37	15%	-1.79	21%	64.50	23%	241.65	17%
Delta	0.01		0.13		1.47		1.23	

Assembly Process



Schematic of conveyorized spray-in-air inline cleaning system

Assembly Process

- Cleaning Agents Used
  - Pure de-ionized water at 100% concentration (10 Meg-ohm resistivity)

- Cleaning Agent Specs:
  - Aqueous-based for removal of lead-free water-soluble fluxes
  - Excellent compatibility with variety of metals (Sn, Ag, Cu, Ni, Al, etc.)
    - Lack of corrosion inhibitors can easily attack these metals causing galvanic corrosion reactions
  - Specifically developed focusing on stacked copper pillar packages, 2.3D/2.5D/3D IC with FO packaging, fCBGAs and SiP packages having interposers
  - Recommended to be used in spray-in-air batch and inline cleaning processes

Experiment Performed

- Total of 216 substrates built for this study

Cleaning Agent	Concentration (%)	Belt Speed (fpm)	Wash Exposure Time (min)	Total Substrates to be cleaned
DI-water	100	2.0	2.6 (2 min 36 sec)	54
		3.0	1.73 (1 min 44 sec)	54
Cleaning Agent	5	2.0	2.6 (2 min 36 sec)	54
		3.0	1.73 (1 min 44 sec)	54
Total				216

Experiment Performed

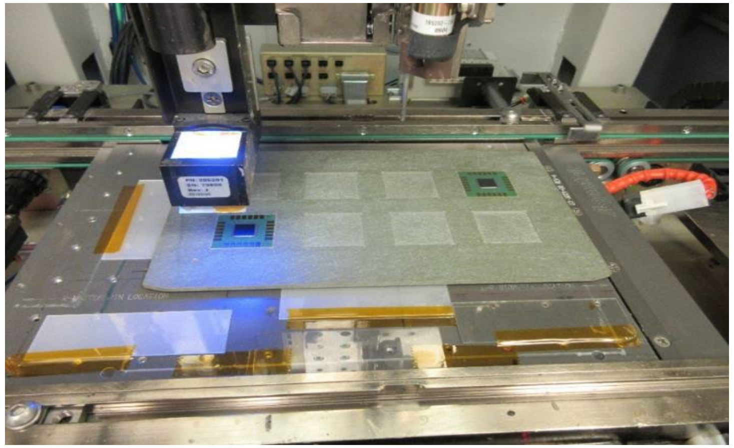
- Conveyorized spray-in-air inline cleaner process parameters

Wash Process	
Cleaning Agent (Concentration)	Cleaning agent (5%) Pure de-ionized water (100%)
Flux Used	Lead-free water-soluble tacky flux
Conveyor Belt Speed	2.0 & 3.0 fpm
Wash Spray Pressure	40 – 80 psi
Cleaning Temperature	150°F / 65.55°C
Chemical Isolation Pressure	30 PSI / 25 PSI

Rinse Process	
Rinsing Agent	DI-water
Rinse Spray Pressure	40 – 85 psi
Rinse Temperature	140°F / 60°C
Final Rinse Pressure	25 PSI / 25 PSI
Final Rinse Temperature	Room Temperature
Drying Process	
Drying Temperature	160 - 220°F

Experiment Performed

- Post-cleaning, the substrates were underfilled using a liquid epoxy encapsulant
- Process was carried out using Asymtek Axiom X-1020 dispensing system configured with Asymtek's DJ-9500 DispenseJet valve



Underfill process setup

Flip chip 10mm x 10mm in size on substrate (with underfill)

Experiment Performed

Reliability / Analytical Test	Description / Reference Document	DI-water process		Cleaning Agent Process	
		2.0 fpm	3.0 fpm	2.0 fpm	3.0 fpm
Thermal Cycling (1000 cycles at -40°C to 125°C)	JESD22-A104E	15	15	15	15
HTSL (1000 hours at 150°C)	JESD-22-A-103C	15	15	15	15
MSL-3	IPC test per J-Std-020E	15	15	15	15
Ion Chromatography	IPC-TM-650 Method 2.3.28	5	5	5	5
FTIR	FTIR mapping and spot measurements	2	2	2	2
SEM/EDS	SEM for electron imaging & EDS for Elemental Analysis	2	2	2	2

NOTE:

- IC testing performed on bare substrates (5 in total)
- IC testing performed on substrates having lead-free water-soluble tacky flux residues (5 in total)

Reliability Test Results

Cleaning Process	Total No. of Substrates Tested	Reliability / Analytical Test	Description / Reference Document	Results
De-ionized water at 2.0 fpm	15	Thermal Cycling (1000 cycles at -40°C to 125°C)	JESD22-A104E	Pass electrical test
	15	HTSL (1000 hours at 150°C)	JESD-22-A-103C	Pass electrical/visual
	15	MSL-3	IPC test per J-Std-020E	No delamination observed No external crack visible under 40X magnification
	2	SEM/EDS	SEM for electron imaging & EDS for Elemental Analysis	Organic residues visible on chip and Au-pad
	2	FTIR	FTIR mapping and spot measurements	Carbon/flux signals visible around bumps and Au-pad
	5	Ion Chromatography	IPC TM-650 Method 2.3.28.	Above pass/fail limits

Reliability Test Results

Cleaning Process	Total No. of Substrates Tested	Reliability / Analytical Test	Description / Reference Document	Acceptance
Cleaning Agent at 2.0 fpm	15	Thermal Cycling (1000 cycles at -40°C to 125°C)	JESD22-A104E	Pass electrical test
	15	HTSL (1000 hours at 150°C)	JESD-22-A-103C	Pass electrical/visual
	15	MSL-3	IPC test per J-Std-020E	No delamination observed No electrical test failure No external crack visible under 40X magnification
	2	SEM/EDS	SEM for electron imaging & EDS for Elemental Analysis	No residues visible on the chip and Au-pad
	2	FTIR	FTIR mapping and spot measurements	No carbon/flux signals visible on bumps and Au-pad
	5	Ion Chromatography	IPC TM-650 Method 2.3.28.	Below pass/fail limits

Reliability Test Results

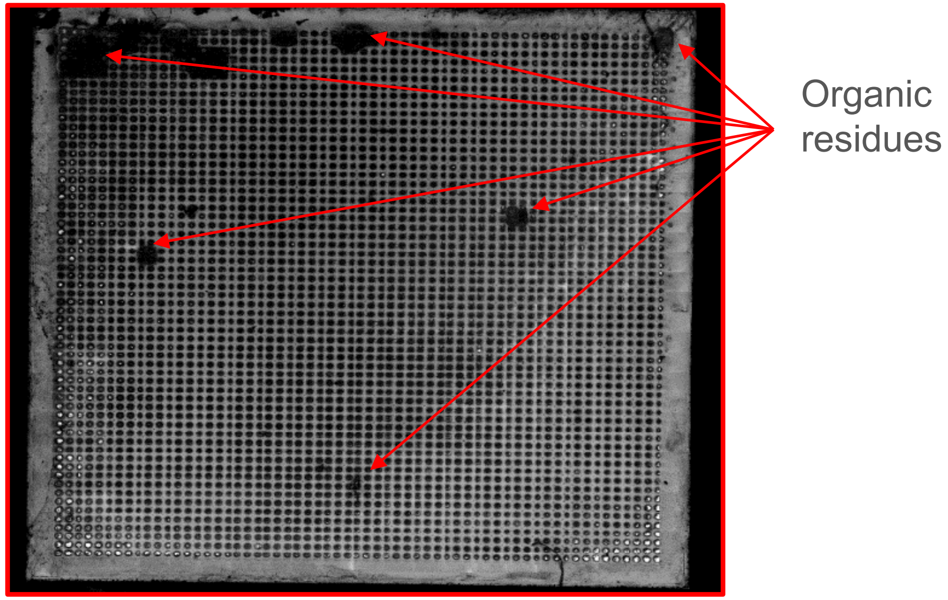
Cleaning Process	Total No. of Substrates Tested	Reliability / Analytical Test	Description / Reference Document	Acceptance
De-ionized water at 3.0 fpm	15	Thermal Cycling (1000 cycles at -40°C to 125°C)	JESD22-A104E	Fail electrical test
	15	HTSL (1000 hours at 150°C)	JESD-22-A-103C	Failed electrical/visual
	15	MSL-3	IPC test per J-Std-020E	Delamination observed between underfill/die and underfill/laminate
	2	SEM/EDS	SEM for electron imaging & EDS for Elemental Analysis	Significant amount of organic residues visible on chip and Au-pad
	2	FTIR	FTIR mapping and spot measurements	Significant amount of carbon/flux signals visible around bumps and Au-pad
	5	Ion Chromatography	IPC TM-650 Method 2.3.28.	Above pass/fail limits

Reliability Test Results

Cleaning Process	Total No. of Substrates Tested	Reliability / Analytical Test	Description / Reference Document	Acceptance
Cleaning Agent at 3.0 fpm	15	Thermal Cycling (1000 cycles at -40°C to 125°C)	JESD22-A104E	Pass electrical test
	15	HTSL (1000 hours at 150°C)	JESD-22-A-103C	Pass electrical/visual
	15	MSL-3	IPC test per J-Std-020E	No delamination observed No electrical test failure No external crack visible under 40X magnification
	2	SEM/EDS	SEM for electron imaging & EDS for Elemental Analysis	No resides visible on chip, very minor amount observed on Au-pad
	2	FTIR	FTIR mapping and spot measurements	No carbon/flux signals visible on bumps; very minor residues visible on the Au-pad
	5	Ion Chromatography	IPC TM-650 Method 2.3.28.	Below pass/fail limits

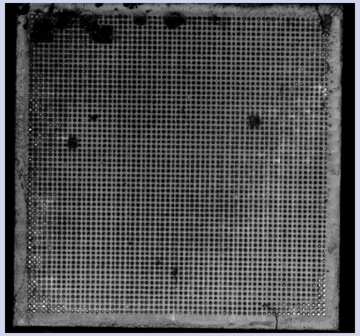
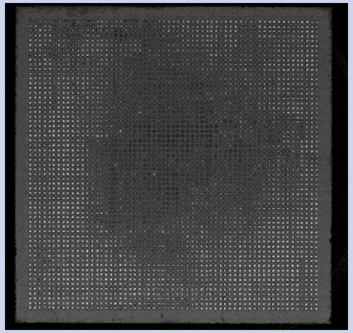
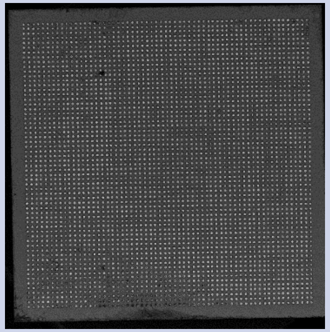
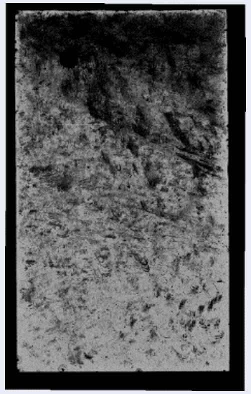
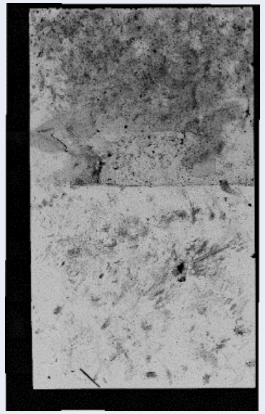
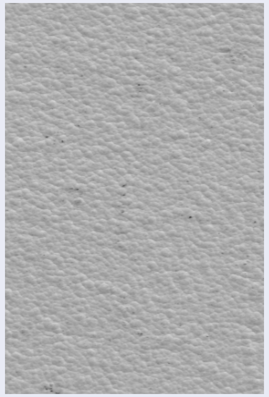
Reliability Test Results - SEM/EDS Analysis

- Performed using Zeiss Sigma 300VP and Oxford X-max^N 80^{TM}
- Entire surface scanned at 200X magnification
- BSE detector at 1.5kV used in this study
  - very sensitive to presence of organic contaminations
  - materials with high density looks brighter (e.g. metals)
  - materials with lower density looks darker (e.g. organics, flux residues)

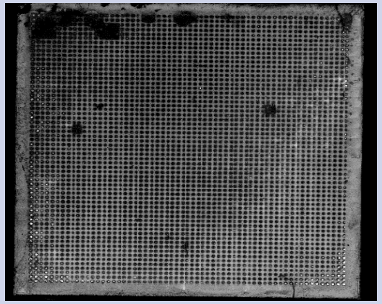
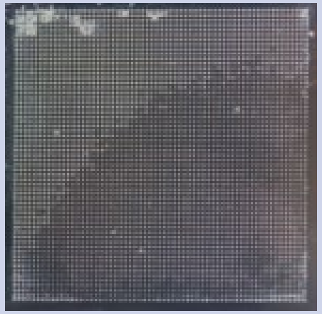
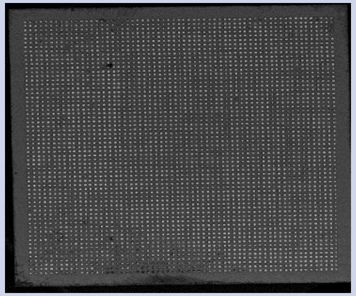
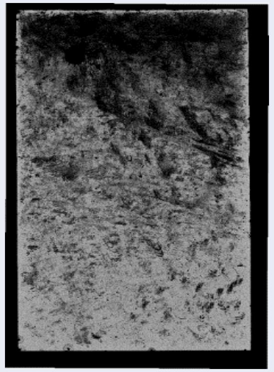
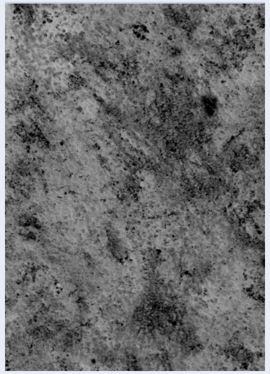


SEM of un-clean chip showing presence of organic flux residues

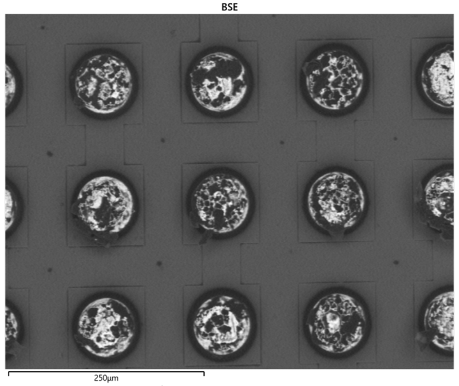
Reliability Test Results - SEM Analysis

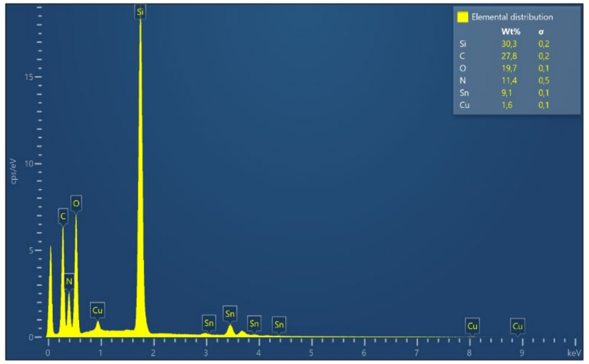
	Un-clean	De-ionized water at 2.0 fpm	Cleaning Agent @ 2.0 fpm
Chip backside (BSE detector)			
Au-pad (BSE detector)			
Results	High amount of organic residues visible on chip backside and all over the Au-pad (black)	Organic residues visible especially in middle area of chip and slight residues visible over the Au-pad (black/dark grey)	No residues visible on the chip and Au-pad

Reliability Test Results - SEM Analysis

	Un-clean	De-ionized water at 3.0 fpm	Cleaning Agent @ 3.0 fpm
Chip backside (BSE detector)			
Au-pad (BSE detector)			
Results	High amount of organic residues visible on chip backside and all over the Au-pad (black)	Significant amount of residues visible on chip and Au-pad (black/dark grey)	No residues visible on the chip, very minor amount observed in few small areas upper corner on Au-pad (black / dark grey)

Reliability Test Results - EDS Analysis

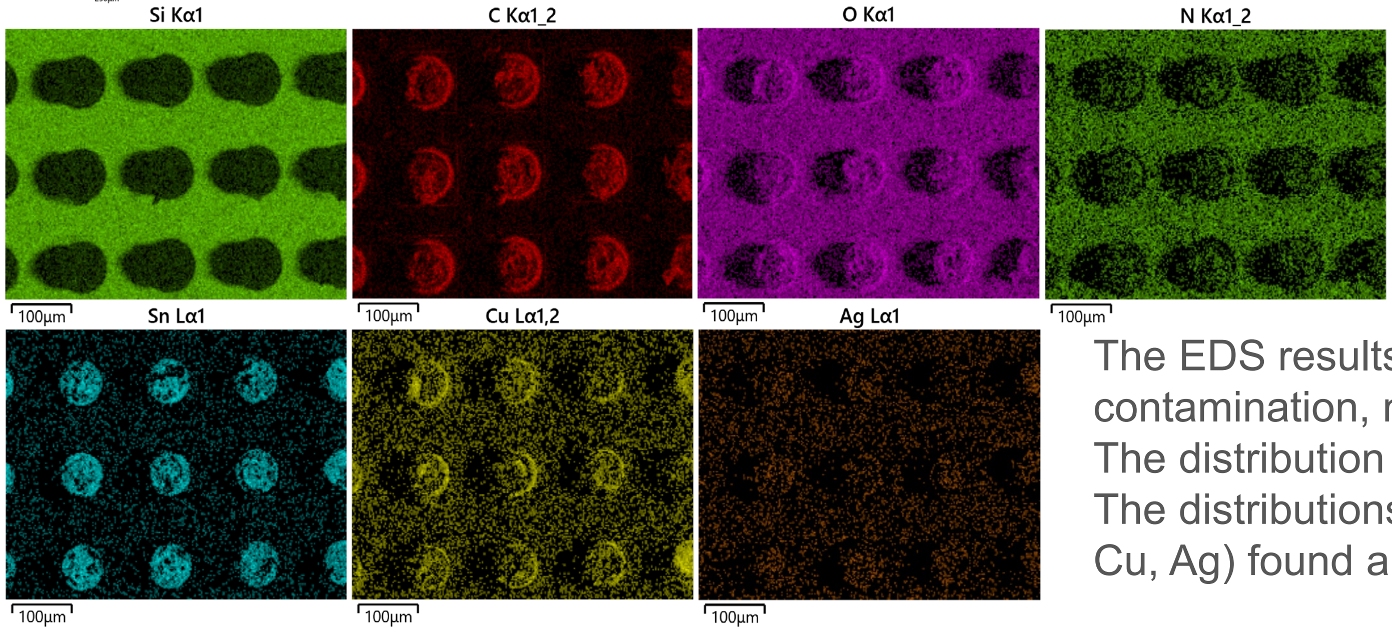




Elemental distribution	Wt%	σ
Si	30,3	0,2
C	27,8	0,2
O	19,7	0,1
N	11,4	0,5
Sn	9,1	0,1
Cu	1,6	0,1

EDS of the representative chip backside area was performed at 10 kV

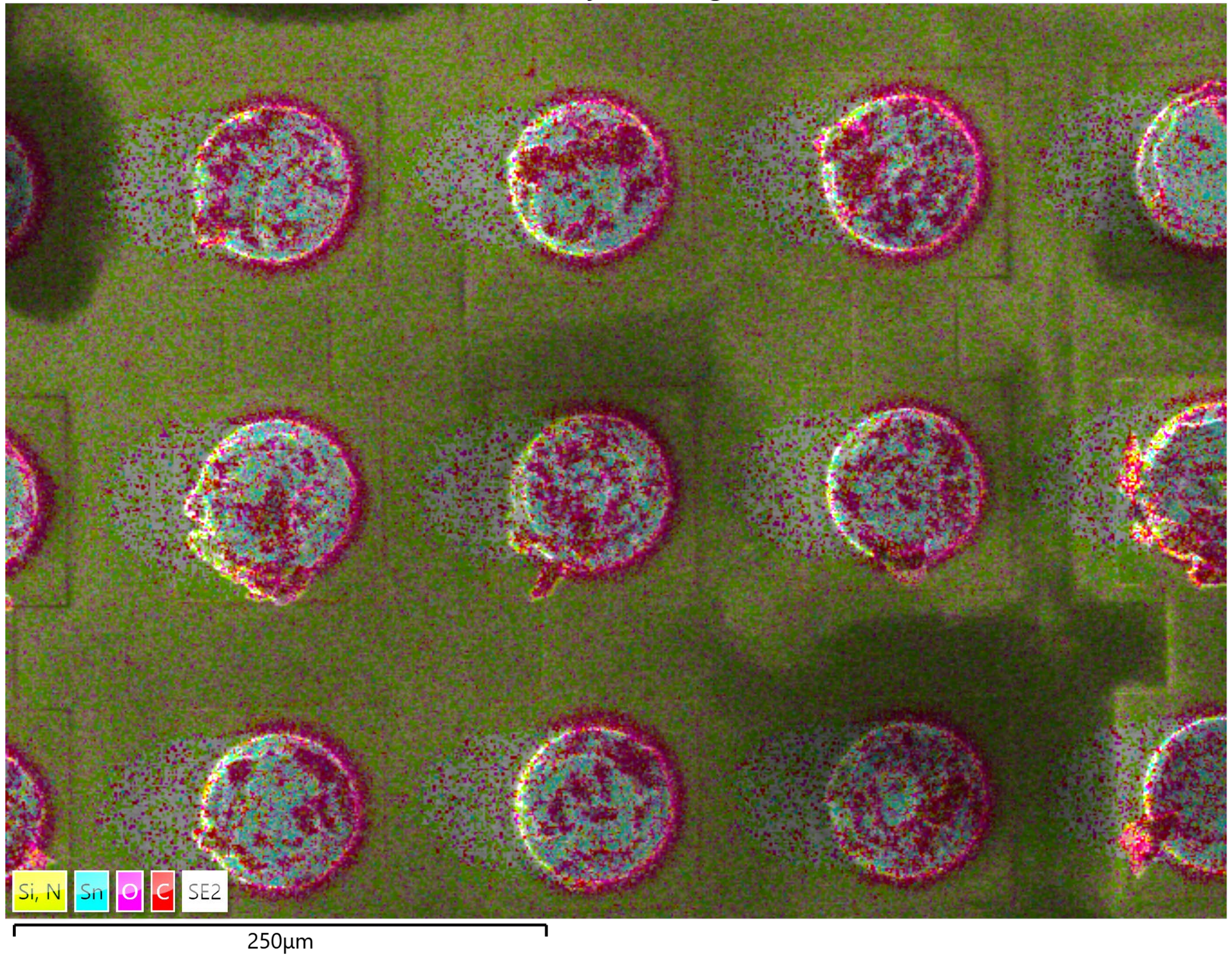
EDS mapping sum spectrum of the whole area was investigated



The EDS results indicate high amount of Carbon contamination, most likely flux, on the Chip backside.
The distribution of Carbon is shown in red.
The distributions of other elements (Si, O, N, Sn, Cu, Ag) found are also presented.

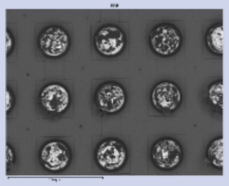
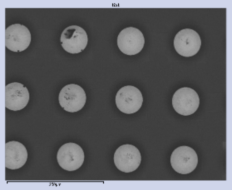
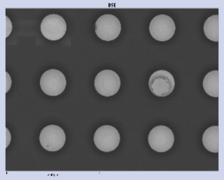
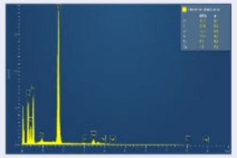
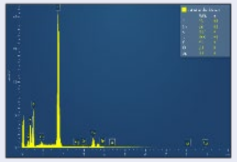
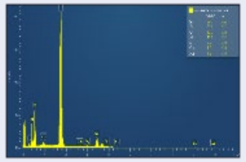
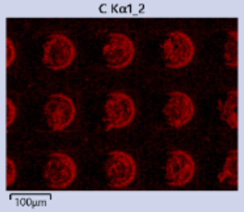
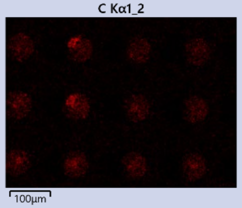
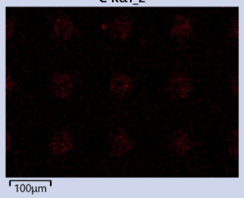
Reliability Test Results - EDS Layered Map (200X magnification)

EDS- Layered image

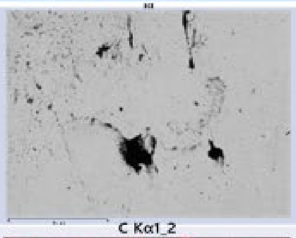
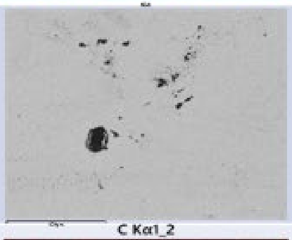
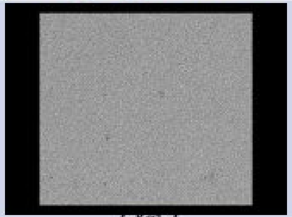
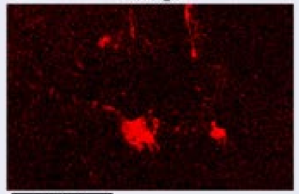
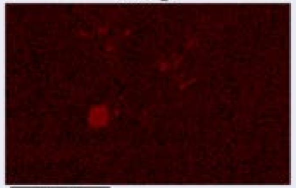
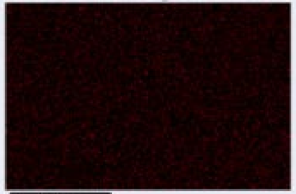
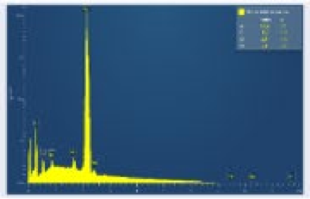
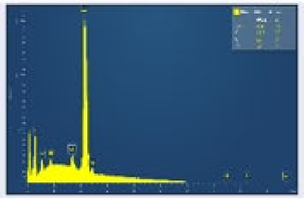
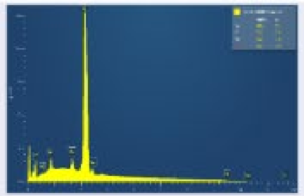


EDS performed at 10kV

Reliability Test Results - EDS Results on Chip Backside

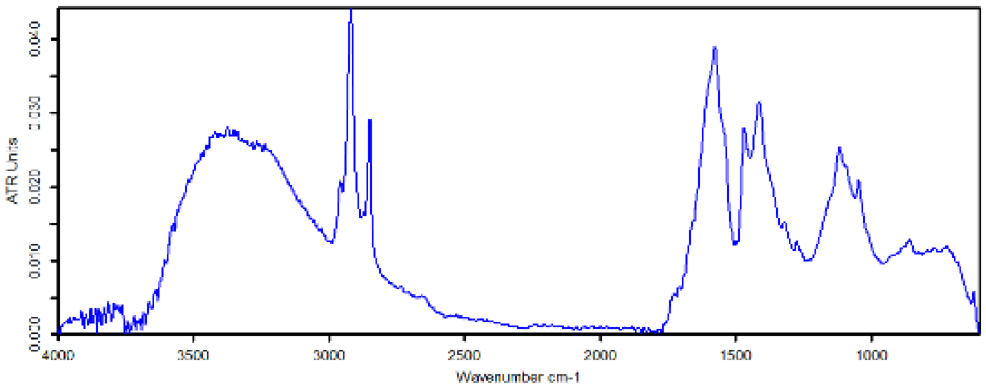
	Un-clean	De-ionized water at 2.0 fpm	Cleaning Agent at 3.0 fpm
Chip backside (BSE & EDS detector)			
			
	C Kα1_2 	C Kα1_2 	C Kα1_2 
	Elemental distribution Wt% σ Si 30,3 0,2 C 27,8 0,2 O 19,7 0,1 N 11,4 0,5 Sn 9,1 0,1 Cu 1,6 0,1	Elemental distribution Wt% σ Si 38,1 0,2 Sn 22,1 0,2 O 18,2 0,1 N 13,3 0,3 C 5,3 0,1 Cu 2,0 0,1 Ag 1,0 0,1	Elemental distribution Wt% σ Si 39,0 0,2 Sn 22,8 0,2 O 18,3 0,1 N 13,8 0,4 C 3,0 0,1 Cu 1,9 0,1 Ag 1,2 0,1
	High amount of carbon contamination, most likely flux is visible on chip backside.	Low to minimal amount of carbon contamination, most likely flux is visible on chip backside.	Very low (trace levels) of carbon contamination visible on chip backside.

Reliability Test Results - EDS Results on Au Pad

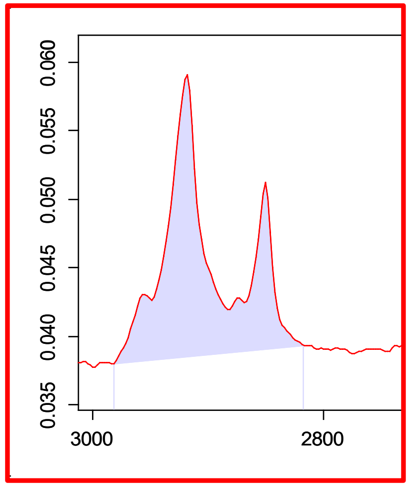
	Un-clean	De-ionized water at 2.0 fpm	Cleaning Agent at 3.0 fpm
Au-pad (BSE & EDS detector)			
	C Kα1_2  100µm	C Kα1_2  100µm	C Kα1_2  100µm
	Elemental distribution Wt% σ Au 81,4 0,2 C 13,2 0,1 O 2,9 0,1 Ni 2,4 0,1	Elemental distribution Wt% σ Au 84,0 0,2 C 11,5 0,1 O 2,5 0,1 Ni 2,1 0,1	Elemental distribution Wt% σ Au 89,5 0,2 C 5,7 0,1 Ni 4,3 0,1 O 0,5 0,1
			
	High amount of carbon contamination, most likely flux is visible on the Au-pad.	Low to minimal amount of carbon contamination, most likely flux is visible on the Au-pad.	Very low (trace levels) of carbon contamination is visible on the Au-pad.

Reliability Test Results - FTIR Analysis

- Performed using Bruker LUMOS™ equipment equipped with liquid nitrogen cooled detector
- Measurements performed in ATR (attenuated total reflection) mode

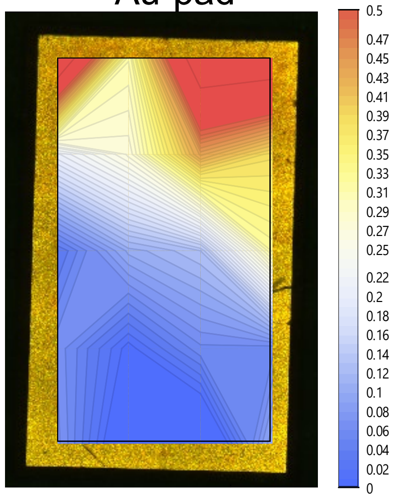


Spectrum of organic flux residue (uncleaned part) used as reference for organic flux residue.



Integration: 2980.9 – 2817.2 cm^{-1}

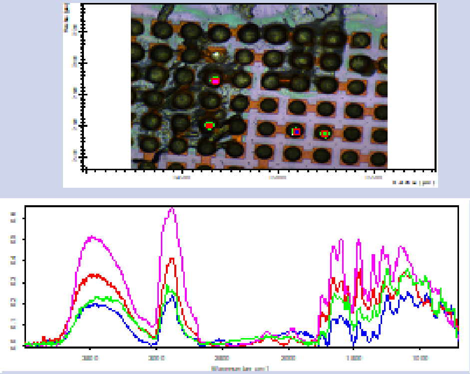
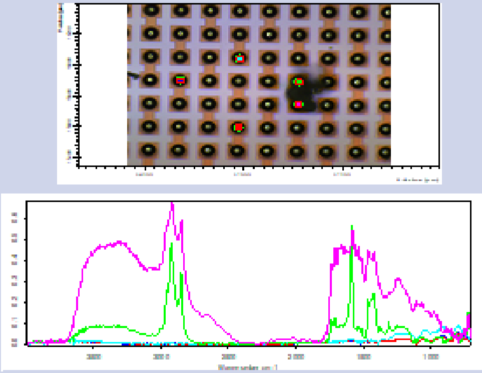
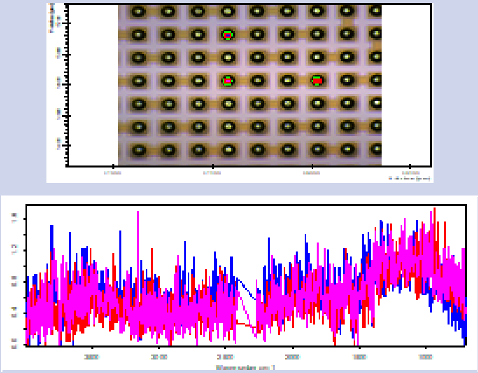
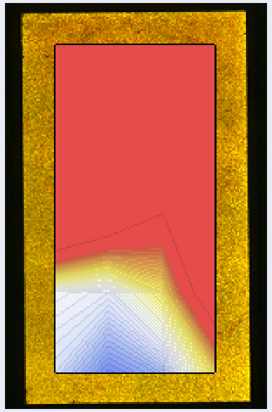
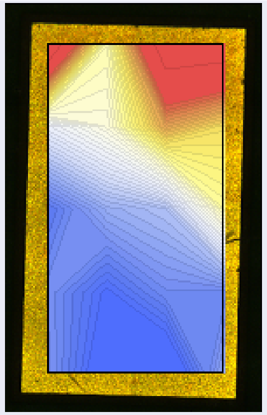
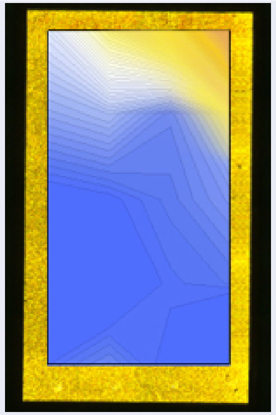
Au-pad



Heatmap calculated from integration.

- FTIR heat map indicates intensity of carbon/flux contamination. Red areas indicate high organic contamination and blue areas indicate very low to zero organic contamination

Reliability Test Results - FTIR Results

	Un-clean	De-ionized water at 2.0 fpm	Cleaning Agent at 3.0 fpm
Chip backside (bumps)			
Au-pad (mapping)			
Results	Significant amount of carbon/flux signals visible on bumps and Au-pad.	Carbon/flux signals visible around bumps and Au-pad	No detectable carbon/flux signals visible on bumps and very minor residues visible in upper right corner on Au-pad

Reliability Test Results

- SEM/EDS Results
  - **Substrates cleaned with DI-water:**
    - Showed presence of organic residues on both chip and Au-pad at 2.0 fpm
    - Significant amount of organic residues seen on both chip and Au-pad at 3.0 fpm
  - **Substrates cleaned with Cleaning Agent:**
    - Did not exhibit any organic residues at 2.0 fpm
    - Very minor amount of residues observed on Au-pad at 3.0 fpm
- FTIR Results
  - **Substrates cleaned with DI-water:**
    - Significant amount of residues observed on both bumps and Au-pad at 2.0 fpm
  - **Substrates cleaned with Cleaning Agent at 3.0 fpm**
    - Did not exhibit any carbon/flux signals on the bumps
    - Very minor residues observed on the Au-pad

Reliability Test Results - Overall Ion Chromatography Results

- Subjected to 10/90 v/v IPA/De-ionized water (as per IPC-TM-650 Method 2.3.28.)
- Bare substrates passed the IC test
  - All ionic species were **below** pass/fail limit
- Un-clean substrates having water-soluble tacky flux failed the IC test.
  - Significantly high levels of cations, anions and weak organic acids.
  - Anions (Formate, Chloride, Bromide, Nitrate, Sulfate) and WOAs **above** pass/fail limit
  - Cations: (Sodium, Ammonium, Potassium) **above** pass/fail limit
- Substrates cleaned with DI-water at 2.0 fpm
  - Formate ions **above** the pass/fail limit in 4 out of 5 substrates
    - Even though substrate #4 passed the IC test, the formate ion values very close to pass/fail limit
  - Chloride ions **above** the pass/fail limit in 3 out of 5 substrates.

Reliability Test Results - Overall Ion Chromatography Results

- Substrates cleaned with DI-water at 3.0 fpm
  - Significant failures observed for acetate, formate and chloride ions
  - Acetate ions **above** the pass/fail limit in 2 out of 5 substrates
  - Formate ions **above** the pass/fail limit on all 5 substrates
  - Chloride ions **above** the pass/fail limit on all 5 substrates

- Substrates cleaned with Cleaning Agent at 2.0 & 3.0 fpm
  - All the ions were **below** the pass/fail limits

Conclusions

- Cleaning with pure de-ionized water is challenging when it comes to removing flux residues underneath copper pillar packages with 150µm bump pitch and a 30µm pillar height

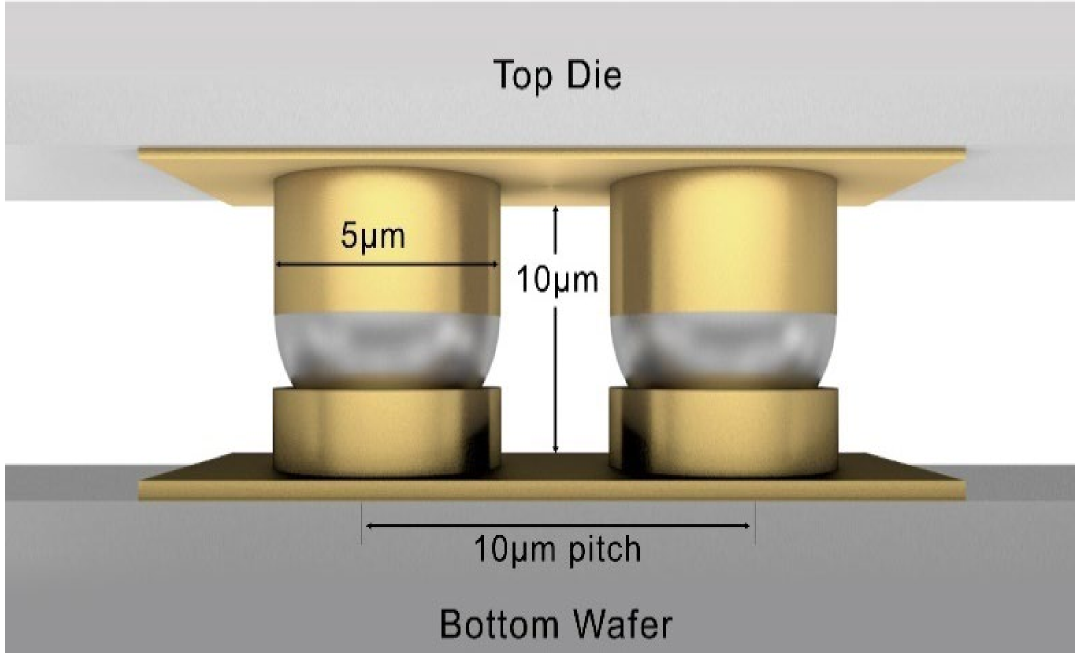
- Substrates cleaned with DI-water failed the TC, HTSL and MSL-3 test especially at faster belt speeds (3.0 fpm)
  - Exhibited presence of organic/carbon contamination via SEM/EDS/FTIR analysis
  - High levels of ionic species found via IC testing

- Substrates cleaned with Cleaning Agent passed the TC, HTSL and MSL-3 test especially at faster belt speeds (3.0 fpm)
  - Better cleaning performance under chip component as well as Au-pad
  - Very minor residue visible via SEM/EDS/FTIR analysis
  - Very low levels of ionic species found via IC testing

Cleaning agent at low concentration (5%) is completely able to remove lead-free water-soluble tacky flux residues at faster belt speed (3.0 fpm), compared to straight de-ionized water at slower belt speed (2.0 fpm)

Excerpts from Phase II study

- 8mm x 8mm die placed on a silicon wafer with 10µm fine pitch
- Gap height between the top die and bottom wafer is 10µm
- Total number of bumps > 150K



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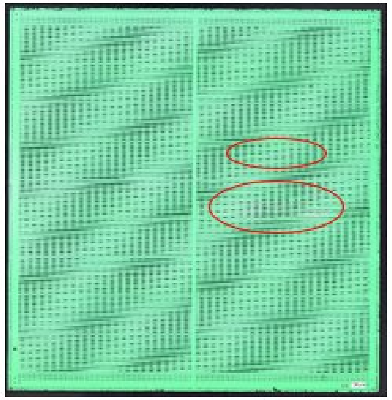
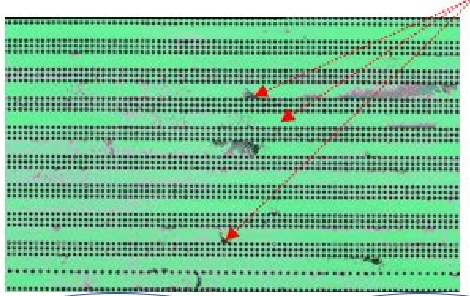
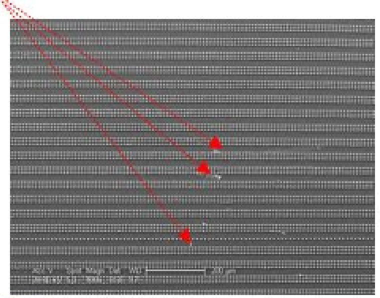
Results – Trial 2 (Low Conc., High Temp., Faster belt speed, 1X wash pass)

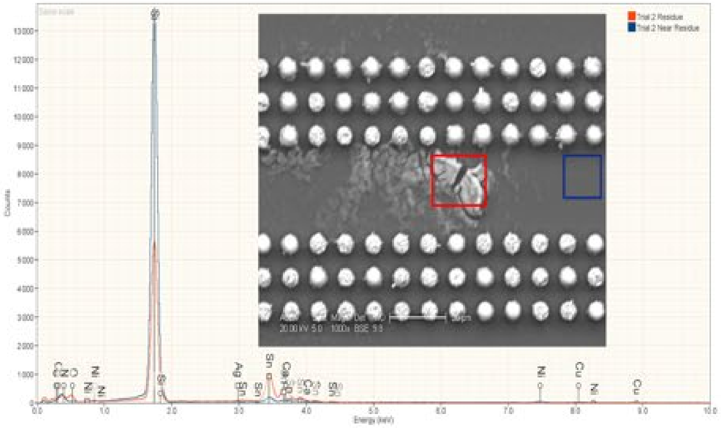


Visual Inspection

Residue observed

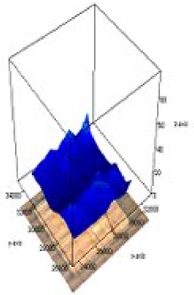


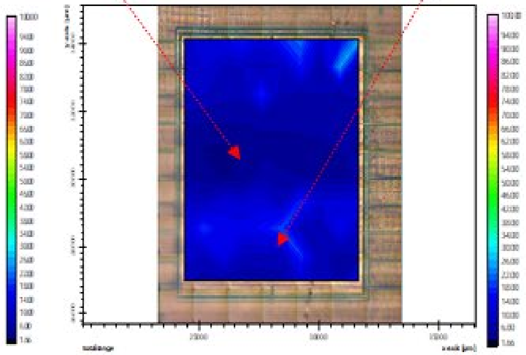




Dark blue color indicates no contamination

Lighter blue shade indicates slight presence of contamination

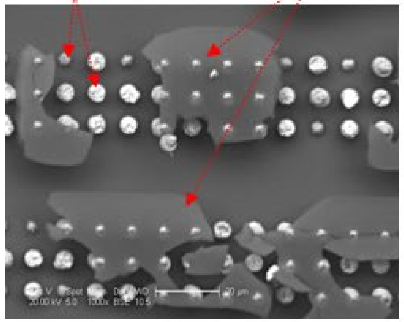




FTIR color mapping shows the presence of contamination: 3D plot (left) and 2D plot (right)

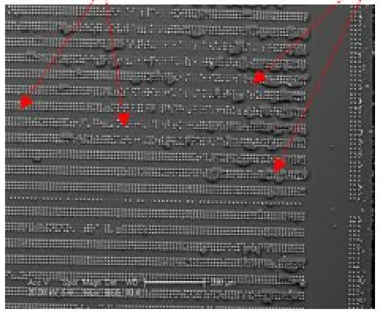
Solder bump broken at different depths

Substrate passivation



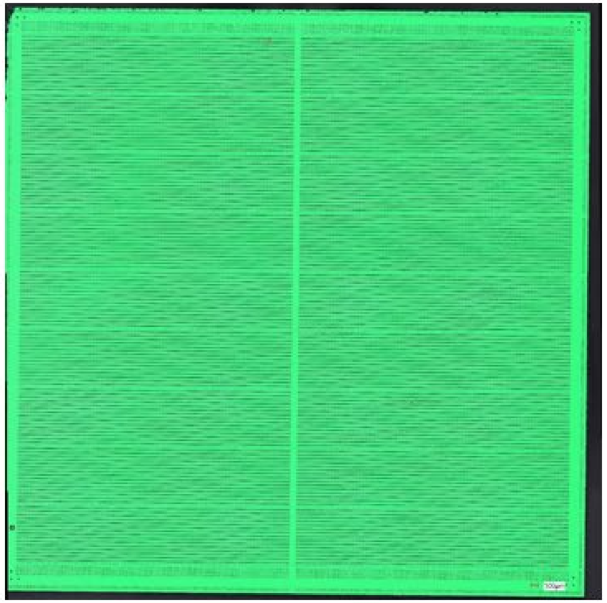
Solder bump broken at different depths

Substrate passivation

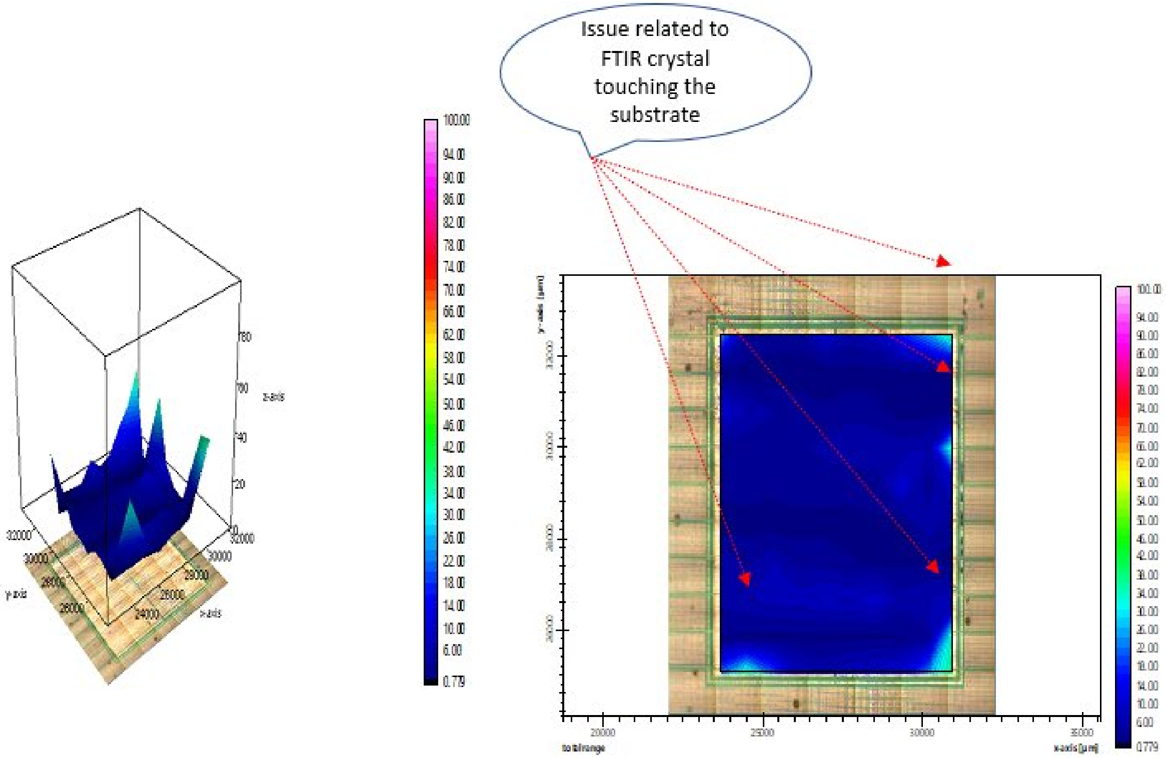


ZESTRON High Precision Cleaning

Results – Trial 5 (Low Conc., Low Temp., Faster belt speed, 2X wash pass)



Visual Inspection



FTIR color mapping shows the residue to be fully removed: 3D plot (left) and 2D plot (right)

Acknowledgement

- R&D of Dr. O.K. Wack Chemie GmbH for continued guidance
- Partner companies that assisted in conducting the study and performing reliability testing
  - ITW EAE (for providing specialized spray manifolds/nozzles)
  - Universal Instruments Advanced Process Lab (for perform detailed reliability analysis)

Thank You! Questions?

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Biography

Ravi Parthasarathy, M.S.Ch.E., is a Senior Application Engineer at ZESTRON Americas. As a long-standing member of IPC, SMTA, iNEMI and iMAPS, Ravi has presented numerous technical studies addressing critical cleaning challenges within the electronics manufacturing industry and is also actively involved in several IPC Task Groups.

Ravi has contributed to several case studies performed in collaboration with manufacturers of electronic assemblies, cleaning equipment providers, and solder paste suppliers. He has written and co-authored several technical articles in industry journals such as Circuits Assembly, SMT Magazine and Global SMT & Packaging. He has recently been appointed to SMTA Global Board of Directors beginning October 2022 and is also currently Vice-Chair for IPC 5-31J Cleaning Committee Task Group

Mr. Parthasarathy graduated with a Bachelor's Degree in Chemical Engineering from the University of Mumbai, India, and a Master's Degree in Chemical & Natural Gas Engineering from Texas A & M University. He has been with ZESTRON Americas since 2004.