Squaring Off with M-Series Fan-Out Technology

Cliff Sandstrom[1] – VP of Technology Development

Benedict San Jose[1], Tim Olson[1],

Jen-Kuang Fang[2], Ping-Feng Yang[2], Sheng Feng-Huang[2], Ping-Ching Shen[2]

[1] Deca Technologies, Tempe, Az

[2] ASE Group, Kaohsiung, Taiwan

Outline

1. Introduction
2. Challenges in HI
3. Large Panel Solutions
4. 2D Scaling
5. Conclusion

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2. Challenges in HI
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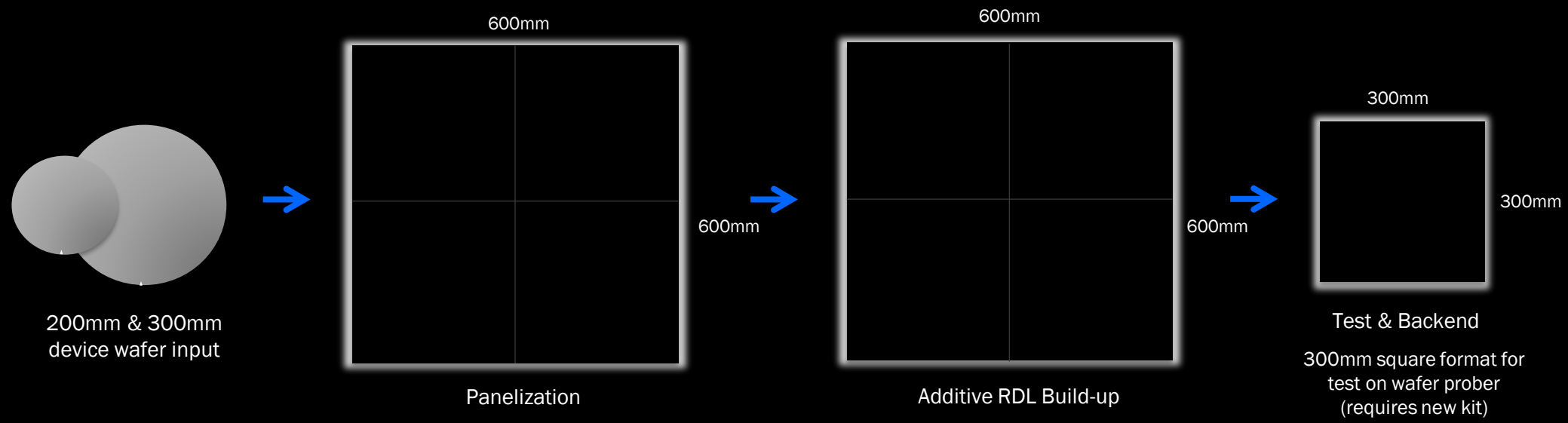
Introduction

- The integration of processors, memory, communication devices, and other functions together with passive components drives HI towards larger package sizes
- As HI module package sizes increase, barriers to continued size growth need to be addressed with innovative solutions
- PLP provides a format to address the cost and feasibility of creating large packages



Outline

1. Introduction
2. Challenges in HI
   - A. Body Size, Cost, and Active Area Utilization
   - B. Reticle Size Limitations
   - C. Die Shift
3. Large Panel Solutions
4. 2D Scaling
5. Conclusion

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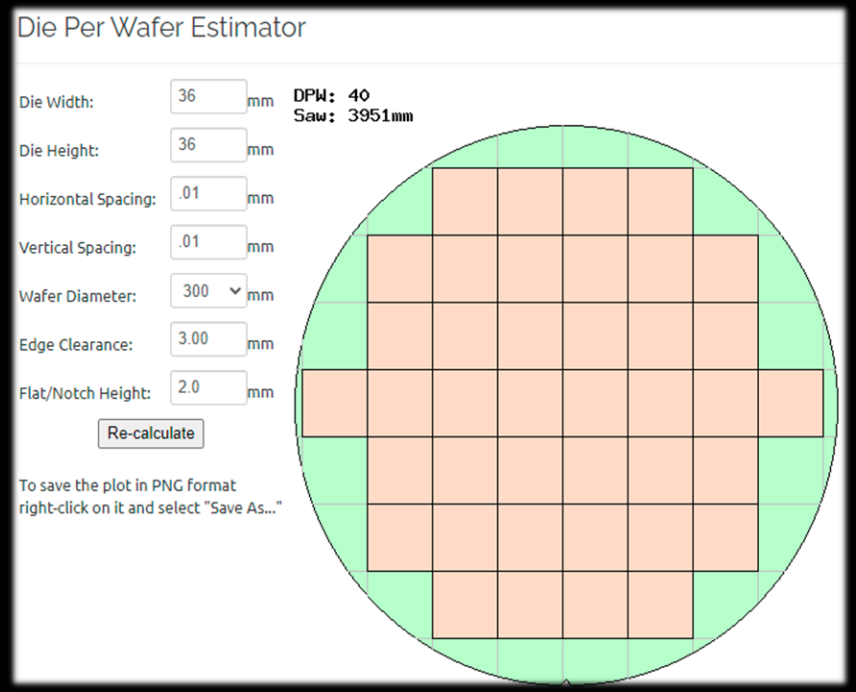
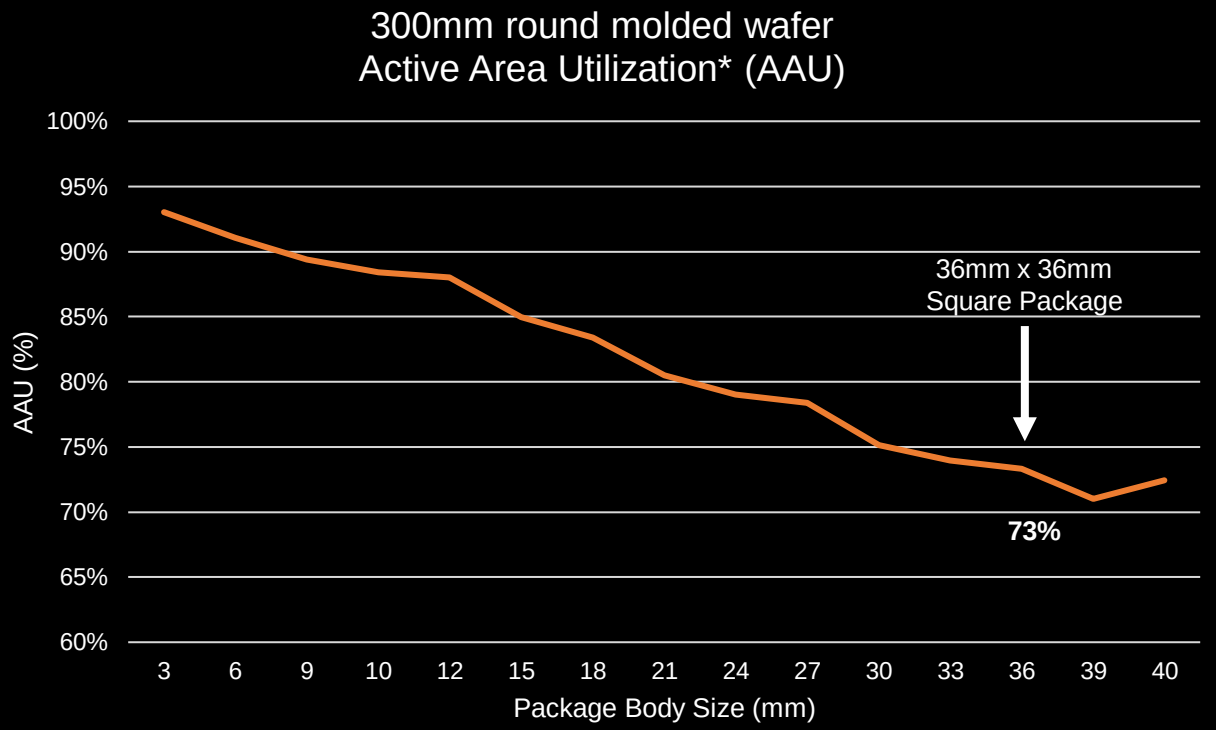
A. Body Size, Cost, and Active Area Utilization

As Heterogenous Integration is moving towards larger packages,
Active Area Utilization (AAU) decreases for 300mm round molded wafers



http://www.silicon-edge.co.uk/j/index.php/resources/die-per-wafer



*Active Area Utilization = potential good packages per panel ÷ total useable panel area (assumes square packages)

27% of active area lost

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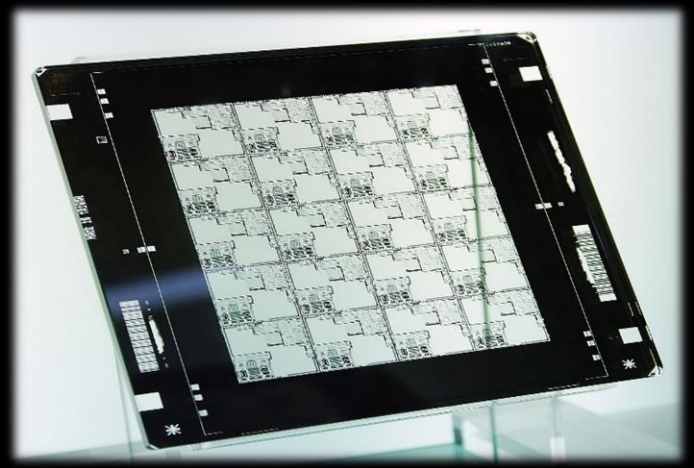
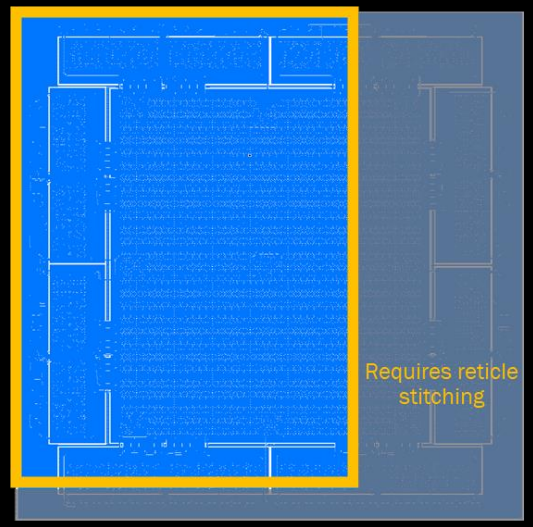
B. Reticle Size Limitations

- Conventional stepper mask-based lithography requires the use of glass reticles
- Complex processor + HBM memory integration exceeding reticle limit, typically around 850 mm^2
- Customers asking for 36 x 36 mm (1,296 mm^2) to 85 x 85mm (7,225 mm^2)
- Stepper throughput loss & reticle stitching

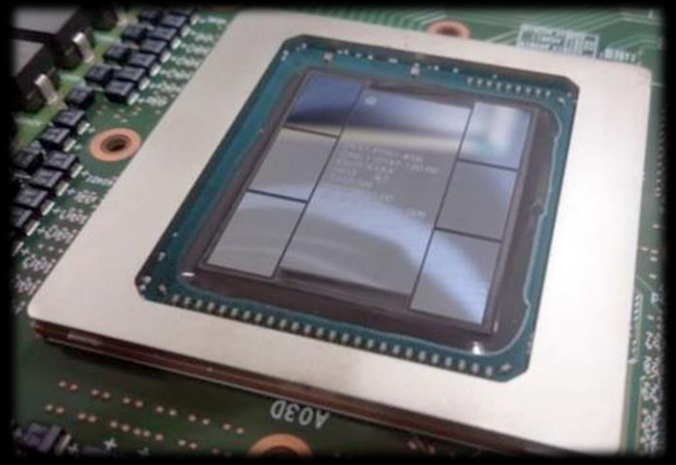


wikipedia.org/wiki/Photomask



36 × 36 mm Device

Single Device - Beyond Reticle Size



https://www.anandtech.com/show/16036/2023-interposers-tsmc-hints-at-2000mm2-12x-hbm-in-one-package

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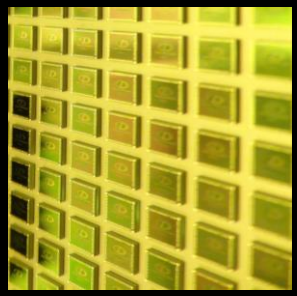
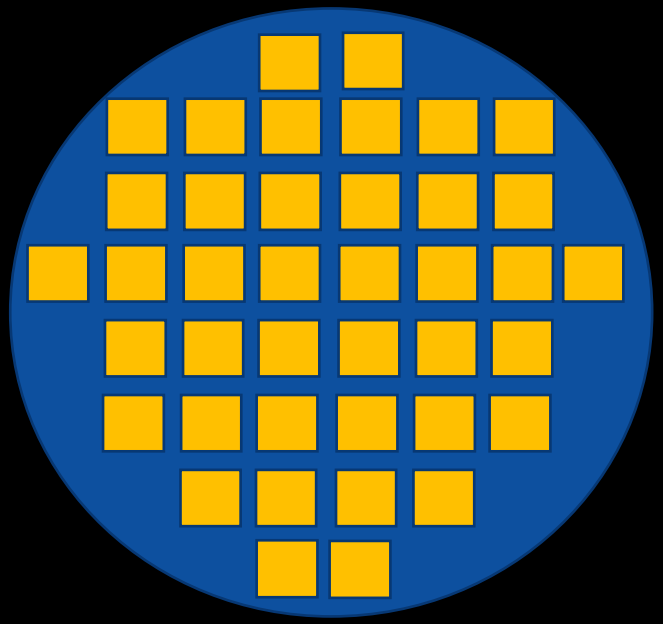
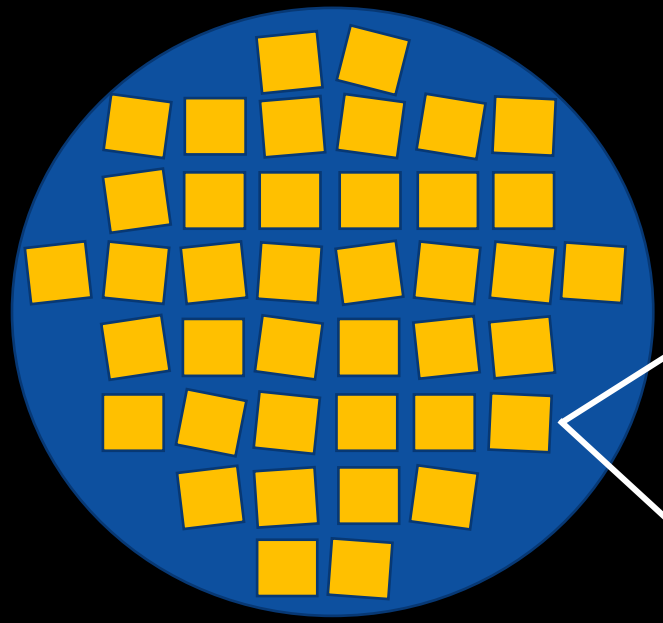
C. Die Shift

- In a stepper, each field as small as a package is aligned and then exposed
- Die by die alignment decreases through-put and multi-die packages are difficult to manage
- Some systems use area alignment, sacrificing accuracy

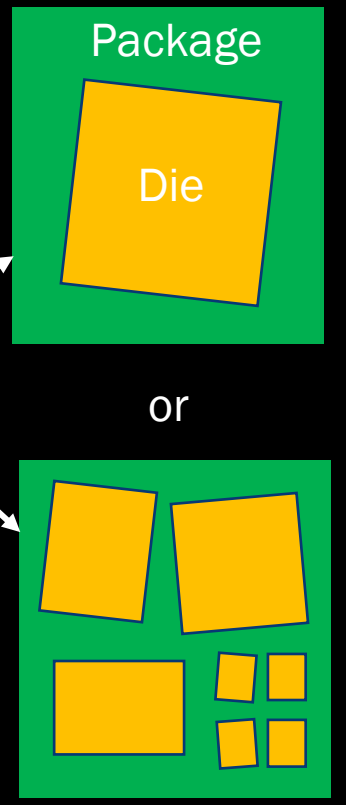




Designed die locations on reconstituted wafer



Actual die locations after die attach and mold



Stepper = each package is an exposure aligned to the die offset

Multi-die or chiplets become difficult to manage

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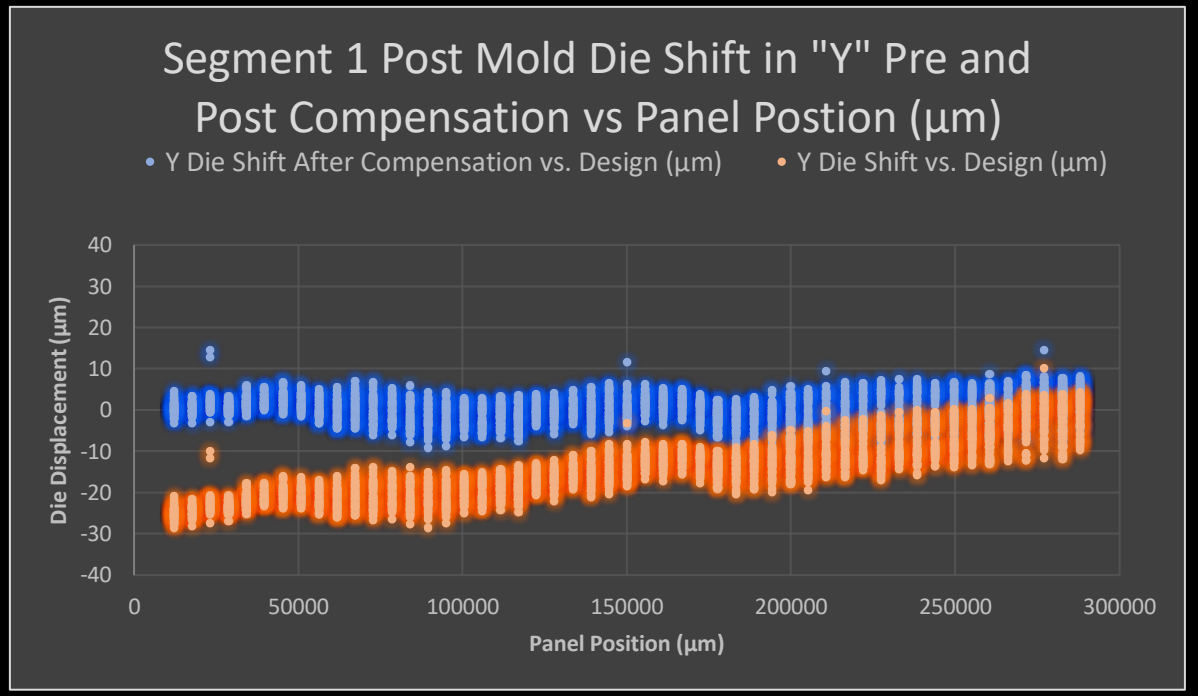
Die Shift Compensation (ASE Data on 600mm)

- The slopes and intercepts were calculated for each segment showing a correlation to panel position
- Uncompensated data is shown in orange vs. the compensated data shown in blue
- With this correlation to panel position, the die placements can be compensated using a simple linear fit



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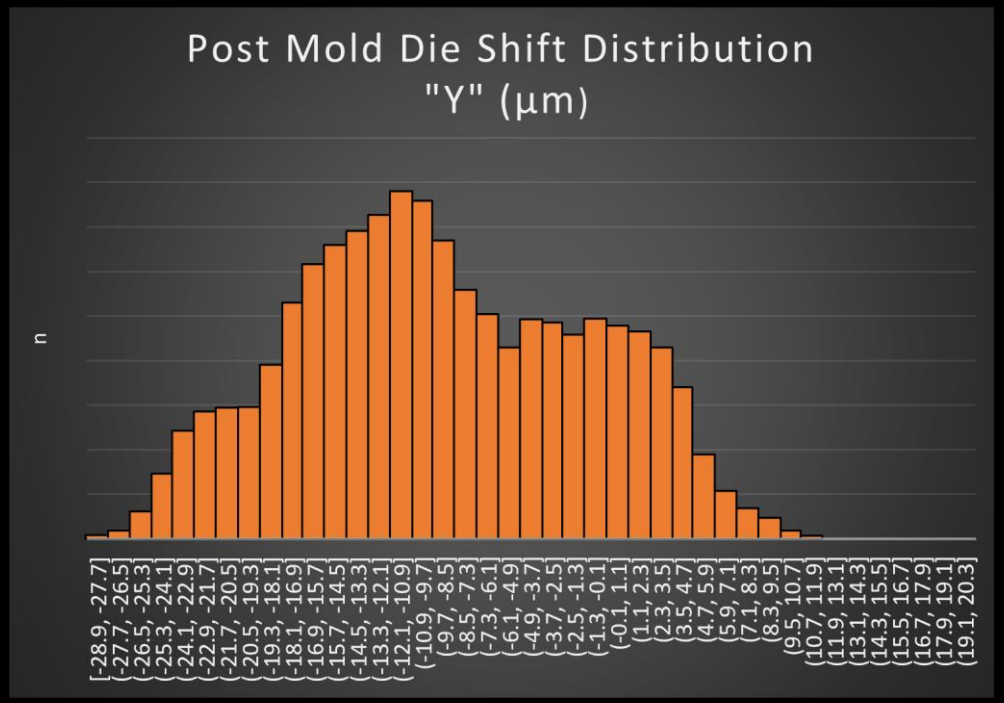
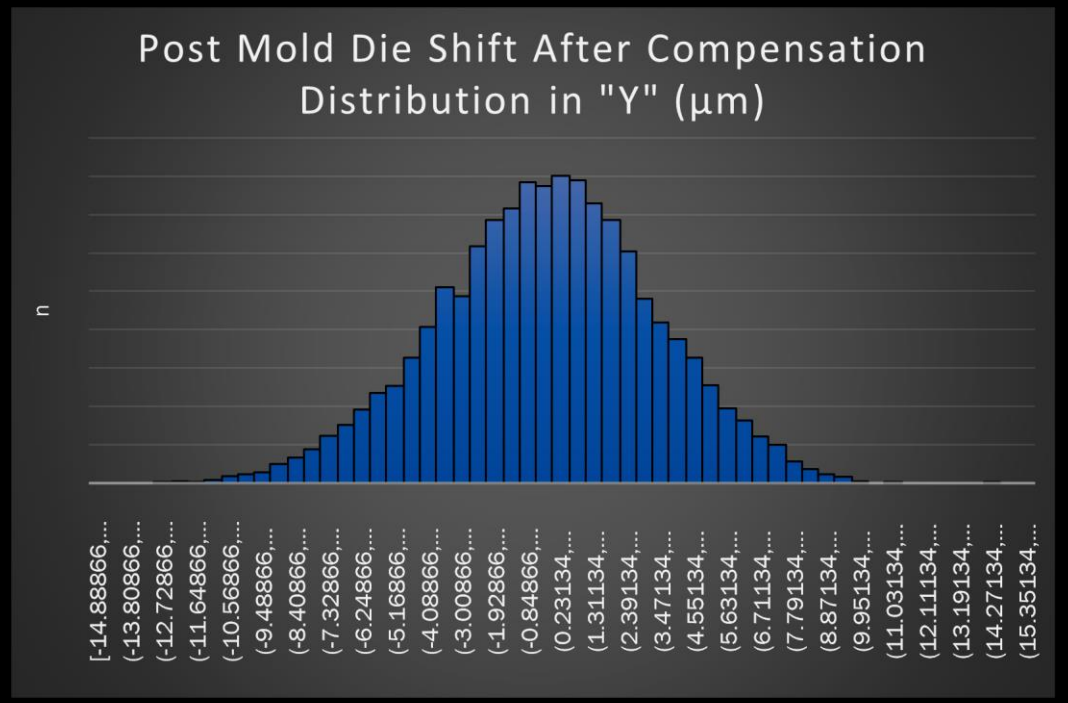
Die Shift Compensation (ASE Data on 600mm)

Initial “Y” Displacement (µm)



Compensated “Y” Displacement (µm)



Before chip attach compensation range of -29 µm to +10 µm centered at -9 µm

After compensation range from -10 µm to +10 µm centered at 0 (with a normal distribution)

Chip attach compensation improves distribution, however, die shift distribution still significant

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    - A. Employ 600mm Square Panel Format
    - B. Laser Direct Imaging
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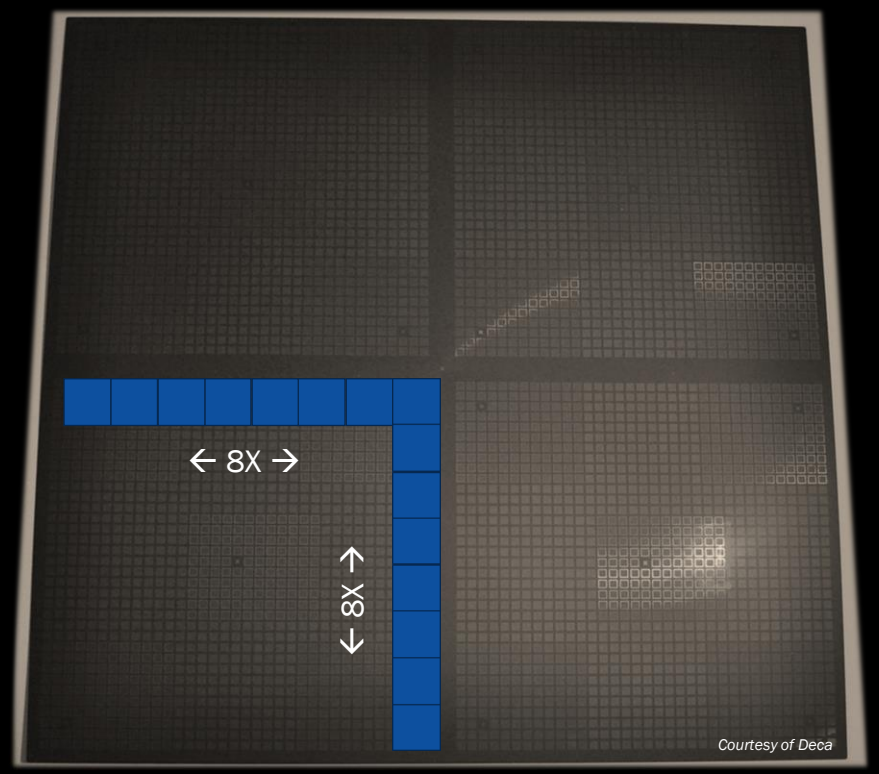
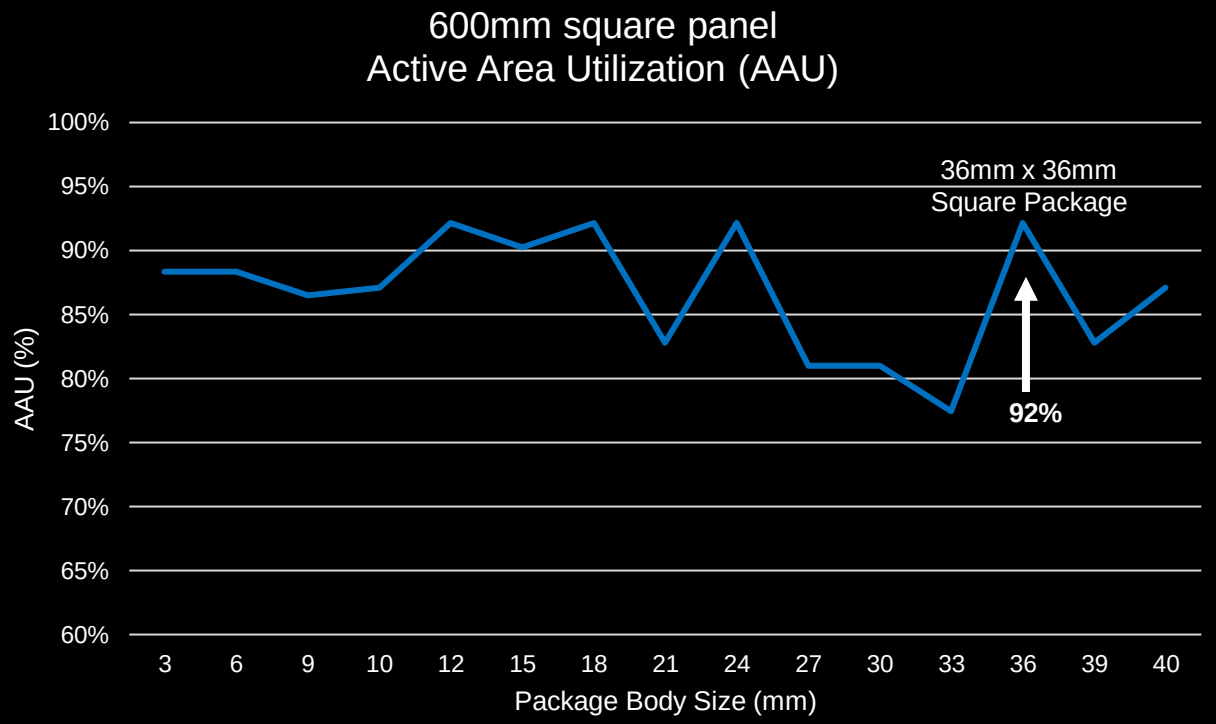
600mm square panel format – AAU and Cost

For a 36 x 36mm HI package, AAU is 92% for 600mm square panels

6.4x increase in package count vs. 300mm round wafers (256 vs 40)





*Active Area Utilization = potential good packages per panel ÷ total useable panel area (assumes square packages)

Only 8% loss on large panel format

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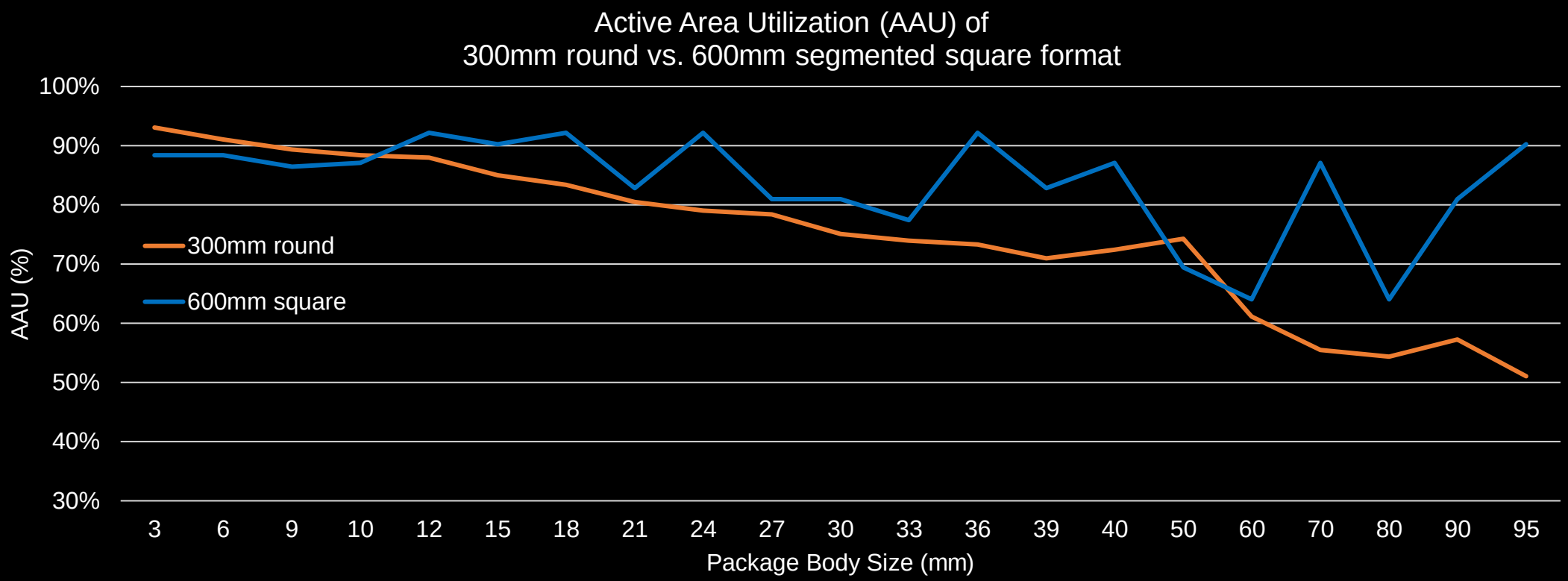
AAU and Material Cost Impact



- 600mm leads to less material wastage, especially for laminate films like die attach tape, mold release tape, and dry film resist)
- For a square 36mm package on 300mm, this is 2,560mm^2 of film consumed vs 1,502mm^2 on 600mm:

  41% reduction in cost on a per package basis across three or more laminates
- Comparing a square 95mm package where the AAU difference is significant, a 59% reduction on a cost per package basis is achieved

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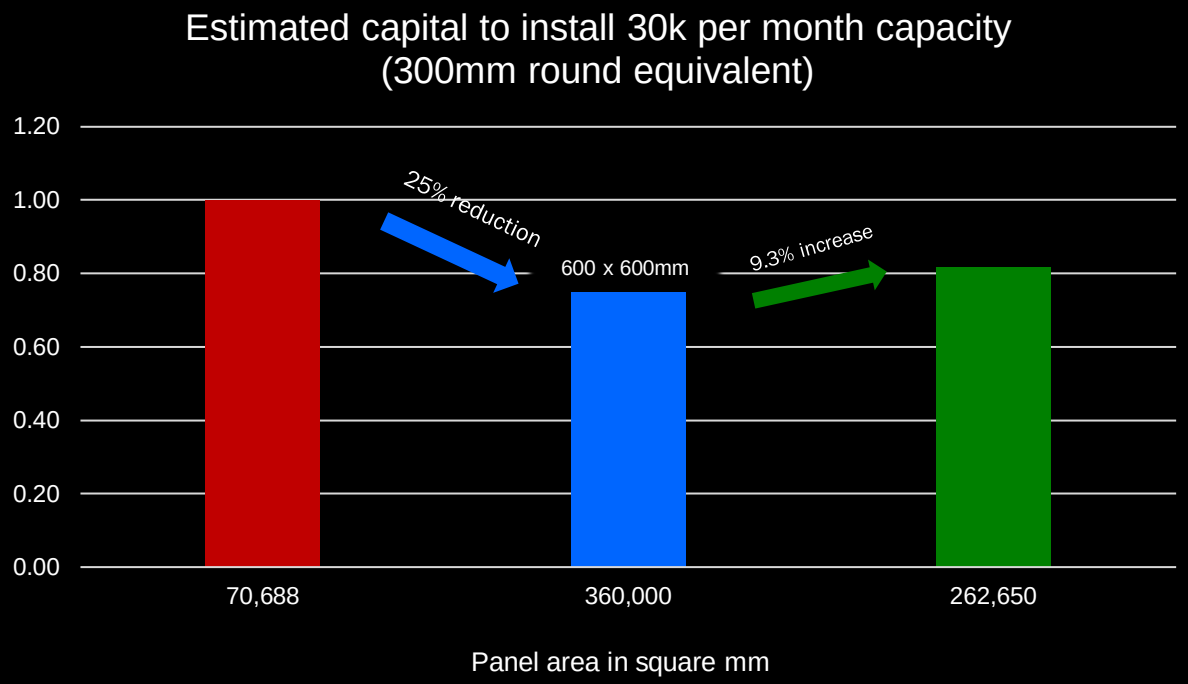
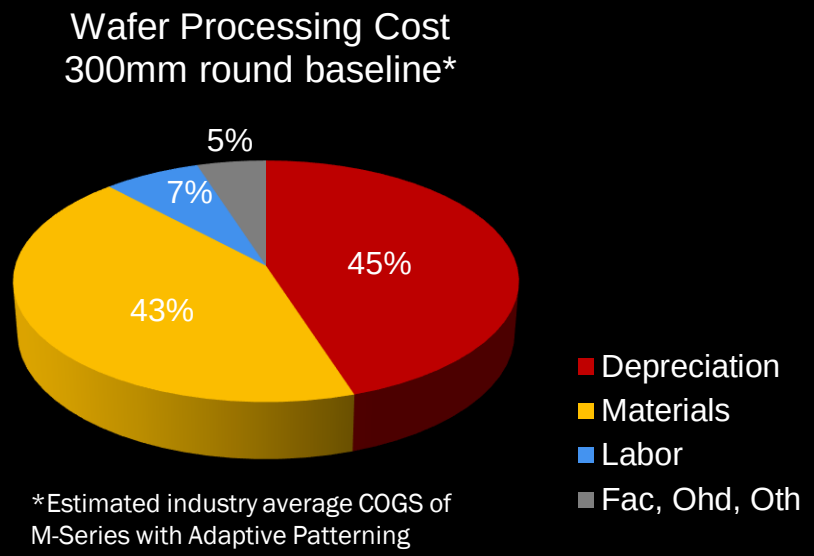
Impact on Capex and Material Cost





Significant cost reduction potential with 600mm large panel format

- Capital productivity – more throughput per CapEx dollar
- Roughly 20% increase in tool cost with half the through-put but with 5-6x more die

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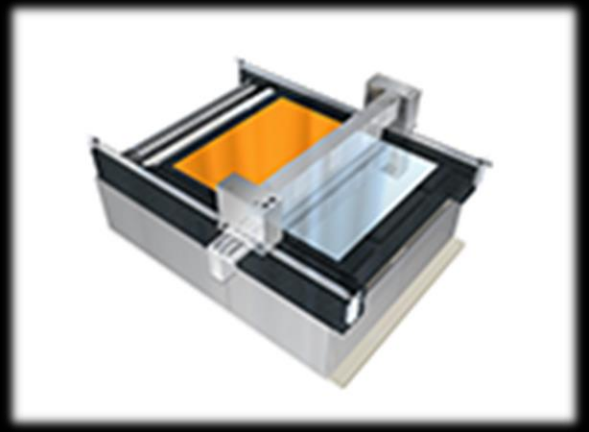
Material Cost - 600mm Slot Coat Example

- Slit or Slot die coating using polyimide with the following attributes:
    1. 600mm x 600mm format
    2. Polyimide diluted by 30% over current 300mm material
    3. Slot coated to 12µm thickness followed by a vacuum dry and bake
- Was able to coat using 22ml of polyimide vs 8ml on 300mm format
- Uniformity across a 600mm panel <3% (see right)
- Example: for a standard high runner M-Series production fan-out part, there are 12,648 candidates on a 600mm panel and 2,567 candidates on 300mm (4.5mm square package)
- For 300mm, this is 0.00312ml per die and for 600mm 0.00174ml per die or 44% reduction in cost on a per die basis
- For our 36mm package, 256 die per panel at 22mm vs 40 die per wafer at 8ml

  is a 57% reduction (0.086ml per die vs 0.2ml per die)



Edge cut 10mm	Grid Measurement	
Max.	12.18	um
Min.	11.49	um
Range	0.69	um
Ave.	11.93	um
Uniformity	2.87	±%

Uniformity = (Range/(2XAve.))X100

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Material Cost - 600mm Laminated Film Example

- Lamination rolls for 300mm in current fab are 320mm wide with a 20mm panel to panel dead zone
- Lamination rolls for 600mm are 620mm wide with the same 20mm panel to panel dead zone
- Films use in the M-Series flow include:

    1. Die attach tape
    2. Mold release tape
    3. Backside laminate used for warpage control
    4. Photoresist dry films for RDL and UBM (two or more)

- For our square 4.5mm package on 300mm, this is 39.9 square mm per die and for 600mm 30.4 square mm per die or 24% reduction in cost on a per die basis across five or more laminates due to wastage from using a round format
- For our square 36mm package on 300mm, this is 2560 square mm per die and for 600mm 1502 square mm per die or 41% reduction in cost on a per die basis

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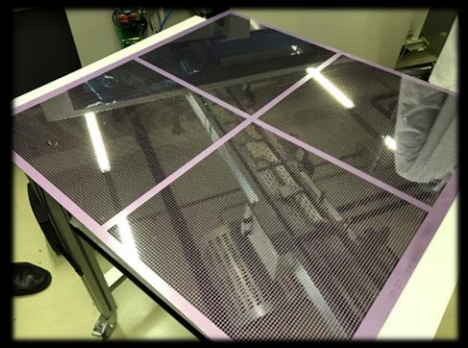
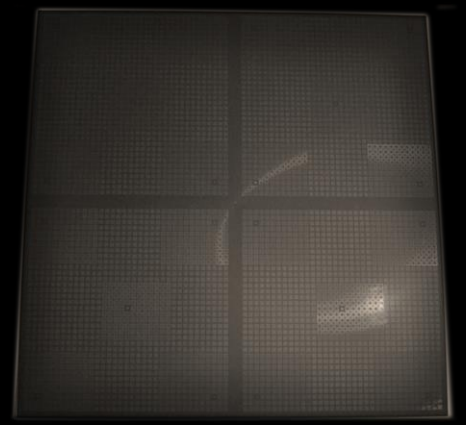
600mm square panel – Molding and Front Planarization results



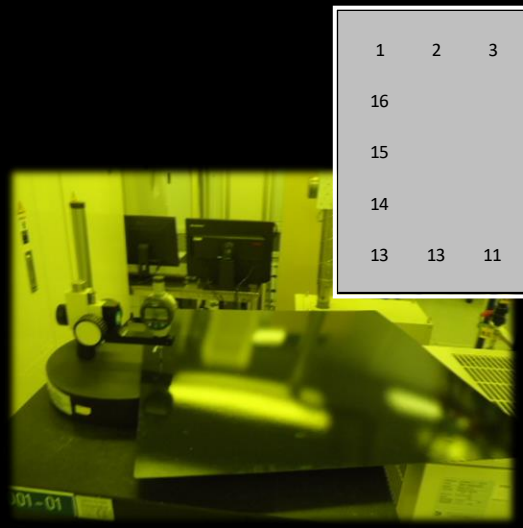
After Die Attach



After Panelization

Samples	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
Carrier Type					
Locations					
1	581	568	578	578	730
2	583	571	579	574	728
3	589	574	581	570	730
4	592	563	578	562	742
5	598	557	588	576	729
6	593	570	581	571	722
7	585	574	579	564	715
8	580	562	571	565	708
9	564	563	576	579	702
10	576	567	578	578	698
11	570	566	573	582	689
12	568	562	565	589	703
13	568	551	568	600	700
14	568	567	563	586	697
15	575	572	568	570	707
16	575	577	569	581	728
Target (um)	575 , ±35 um, TTV: 70 um				700 , ±35 um, TTV:
Ave	579.06	566.50	574.69	576.56	714.25
Stdev	10.31	6.75	6.82	9.93	15.69
TTV	34	26	25	38	53
RESULT	Passed	Passed	Passed	Passed	Passed

Post Mold Thickness TTV



Post Mold Thickness Measurement

Post Mold Thickness
- Actual: TTV < 60 µm

Post Frontgrind TTV
- TTV: < 5 µm
- Ra: < 0.1 µm

1	2	3	4	5	24	25	Avg.	TTV		Target	Delta
6	7	8	9	10	594.6	611.3	572.2	102.6			
11	12	13	14	15	520.9	522.1	522.0	4.6		525.0	3.0
16	17	18	19	20	587.0	625.5	576.8	155.1			
21	22	23	24	25	448.7	449.9	449.4	3.5		450.0	0.6
					582.0	585.3	581.9	51.8			
					523.2	525.0	524.6	3.9		525.0	0.4
					605.7	622.8	582.4	100.1			
					522.9	524.8	524.3	4.0		525.0	0.7
							TTV Avg	Pre	102.4	Delta Avg	1.2
								Post	4.0		

Post Front TTV

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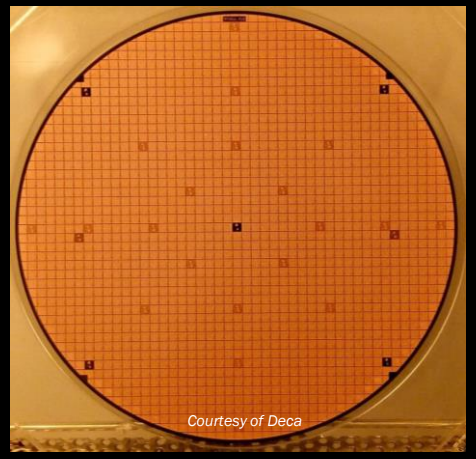
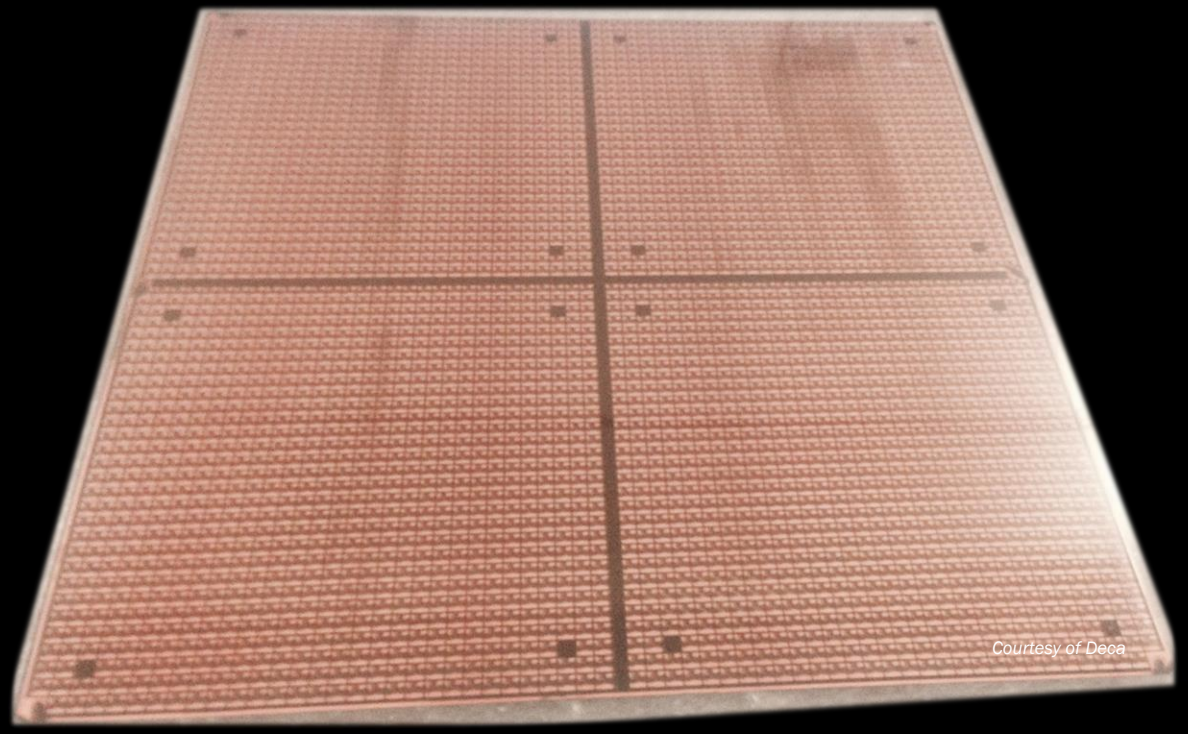
M-Series Fan-out Production Formats

M-Series – After RDL

300mm Wafer Production



Large Panel Production



600mm x 600mm square panel

600mm delivers

- *Lower cost of capital per unit output*
- *Estimated 15% reduction in the cost of materials (higher utilization of PI & PR)*
- *Projected 25% overall cost reduction vs. 300mm round*

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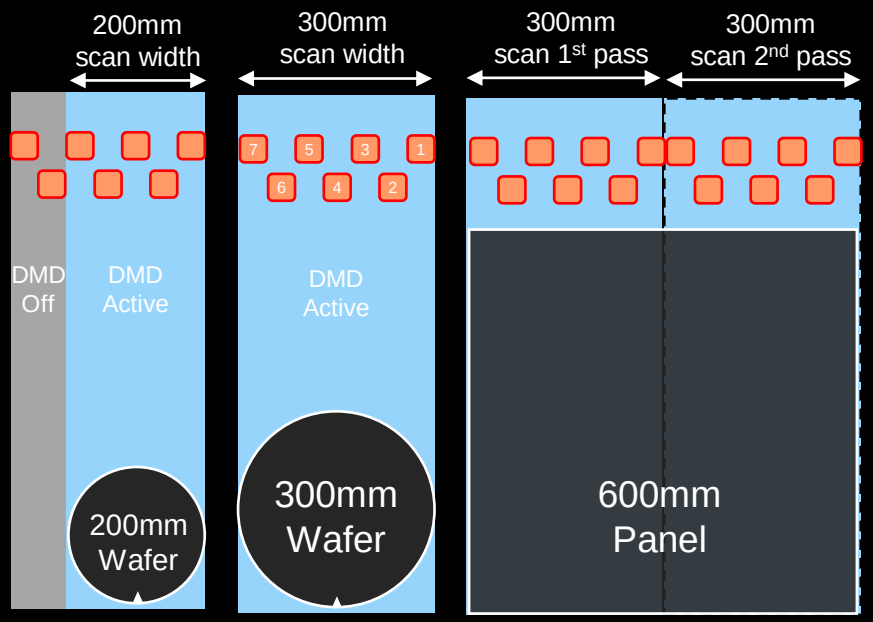
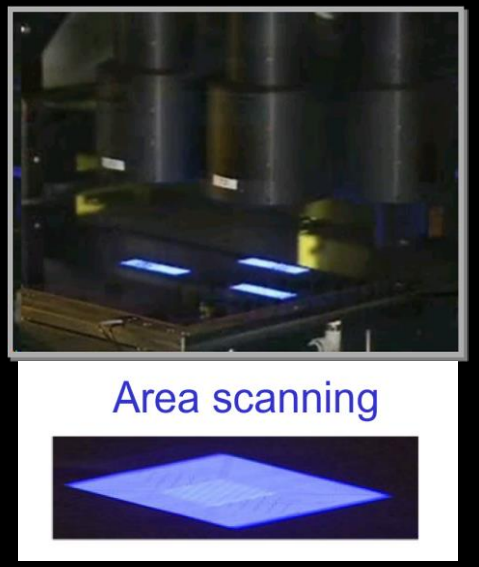
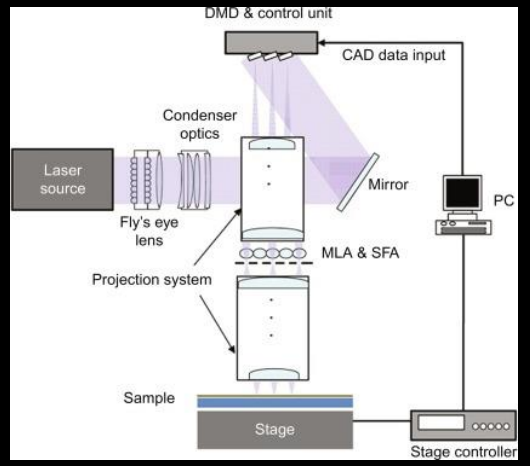
B. Eliminate Reticle using Laser Direct Imaging (LDI)

- LDI has no glass photomask and therefore no reticle size limits (ideal for large chiplet integration)
- Opens the possibility to utilize Adaptive Patterning (enables real time design-during-manufacturing)
- Supports formats of 200 mm, and 300 mm round wafers, and up to 600 mm square panels
- Multiple exposure engines using a solid-state laser (single scan 300 mm, dual 600 mm)







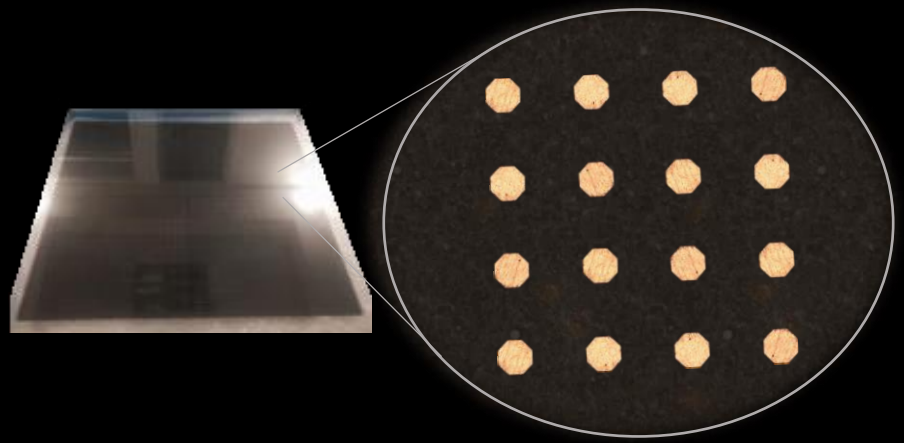
Schematic of DMD based Laser Direct Imaging platform*

*Source: Martinez-Chapa, S., et.al. In *Micro and Nano Technologies*, 2020

C. Solving Die Shift with Adaptive Patterning*

a. Measure actual die positions using high-speed optical scanner

Embedded die



High-speed optical scanner

Measured position per die

-112480	4.452	-75300	11.505	-0.07094
-112480	10.433	-60240	-5.664	0.076578
-112480	33.628	-45180	56.964	0.220956
-112480	17.823	-30120	-4.514	-0.06077
-112480	-0.121	-15060	7.748	0.148717
-112480	9.098	0	-2.332	0.159489
-112480	1.766	15060	1.994	0.042713
-112480	7.599	30120	9.588	0.051493
-112480	-2.226	45180	24.771	-0.01267
-112480	-1.291	60240	-13.819	0.046882
-112480	5.439	75300	-0.659	0.130947
-98420	0.127	-90360	7.939	-0.03352
-98420	3.053	-60240	-4.68	-0.01368

b. Generate unique lithography patterns for polyimide & photoresist layers during manufacturing (every device, every panel)

Measured position per die

-112480	4.452	-75300	11.505	-0.07094
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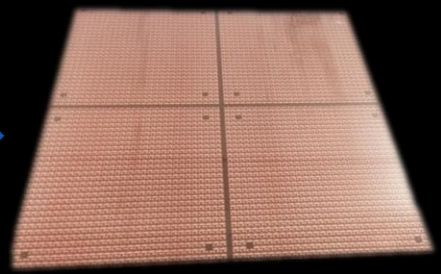
Real-time design-during-manufacturing

ENGINE

Lithography pattern for the whole panel is dynamically generated

Mask-less LDI lithography system

Unique lithography pattern per panel



Entire panel is one GDSII file

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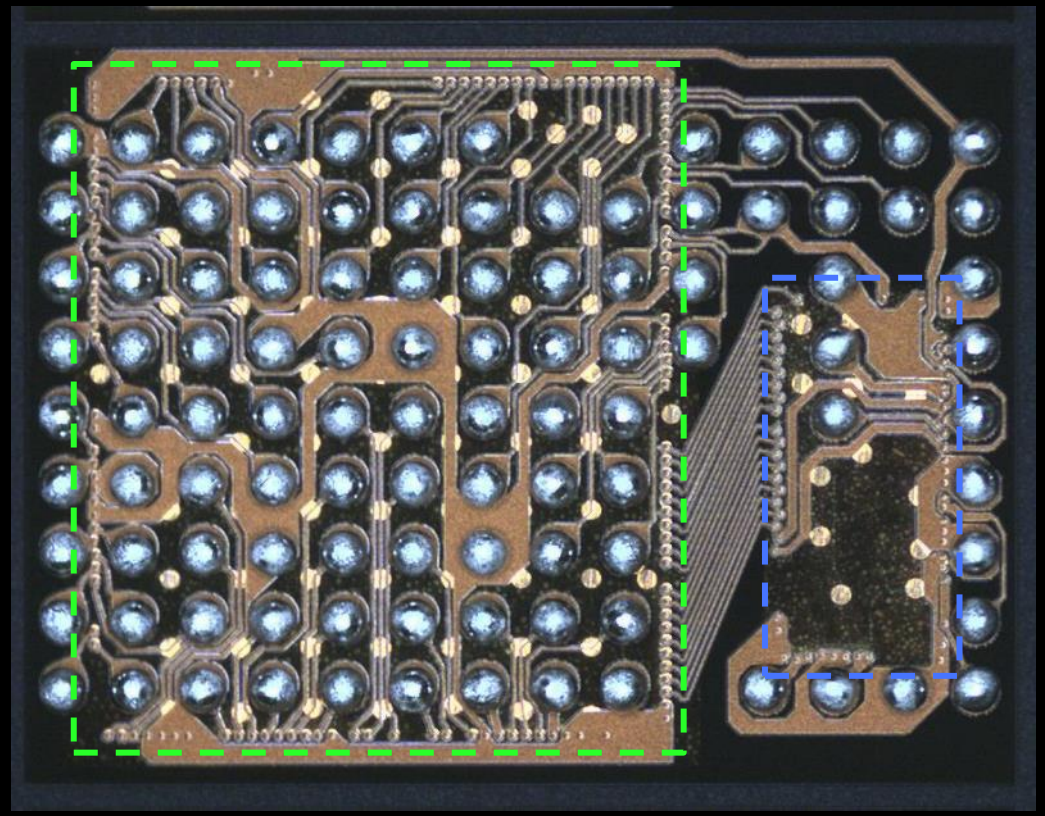
Multi-mode Adaptive Patterning

IoT Module – 2 chips

- High performance MCU – 40nm
- Bluetooth radio – 55nm



<u>Package 5.0 x 3.8 mm</u>

104 IO, 0.4mm pitch

Die 1: 3.7 x 3.2 mm

Die 2: 1.0 x 2.0 mm

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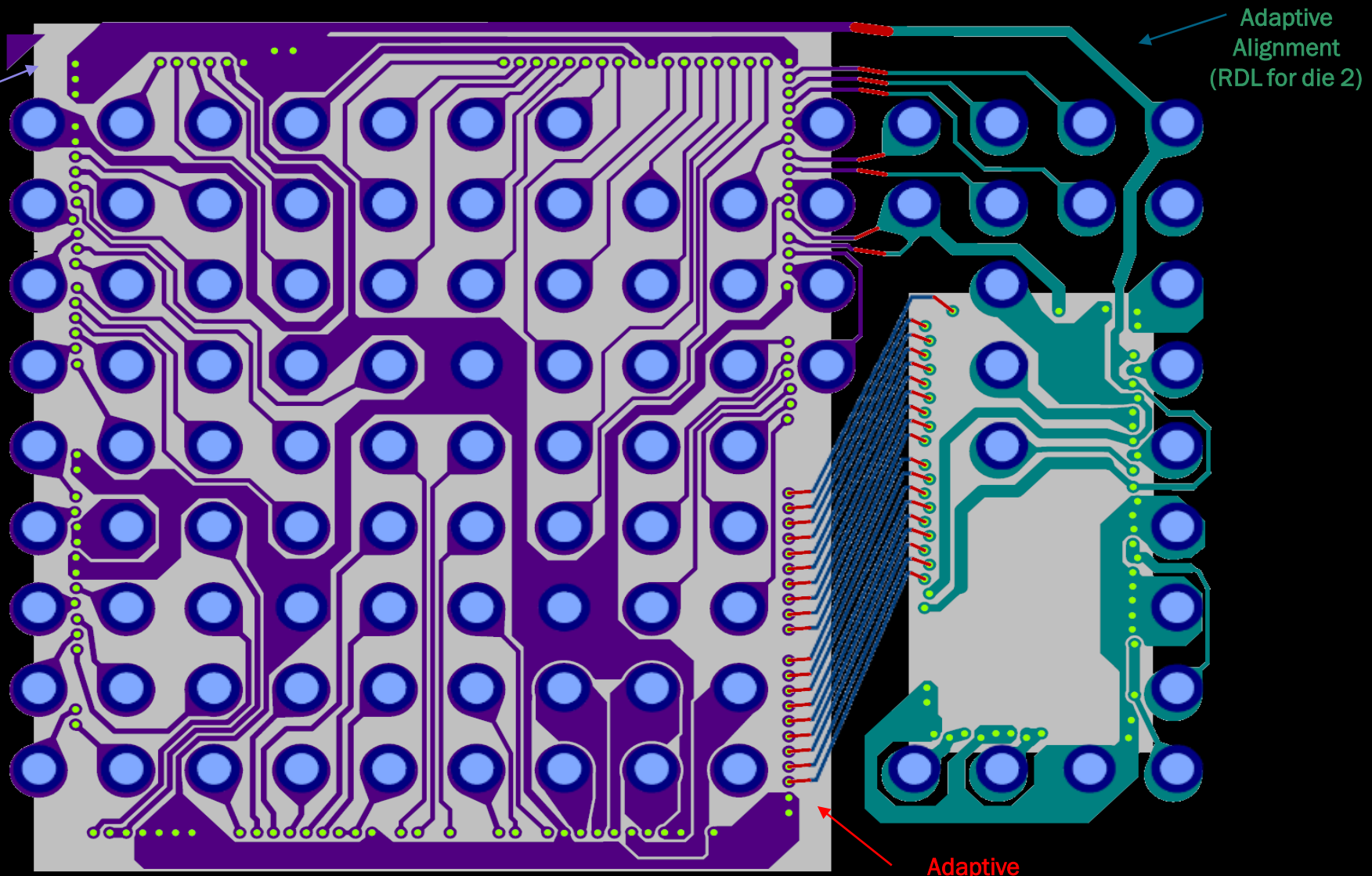
Multi-mode Adaptive Patterning



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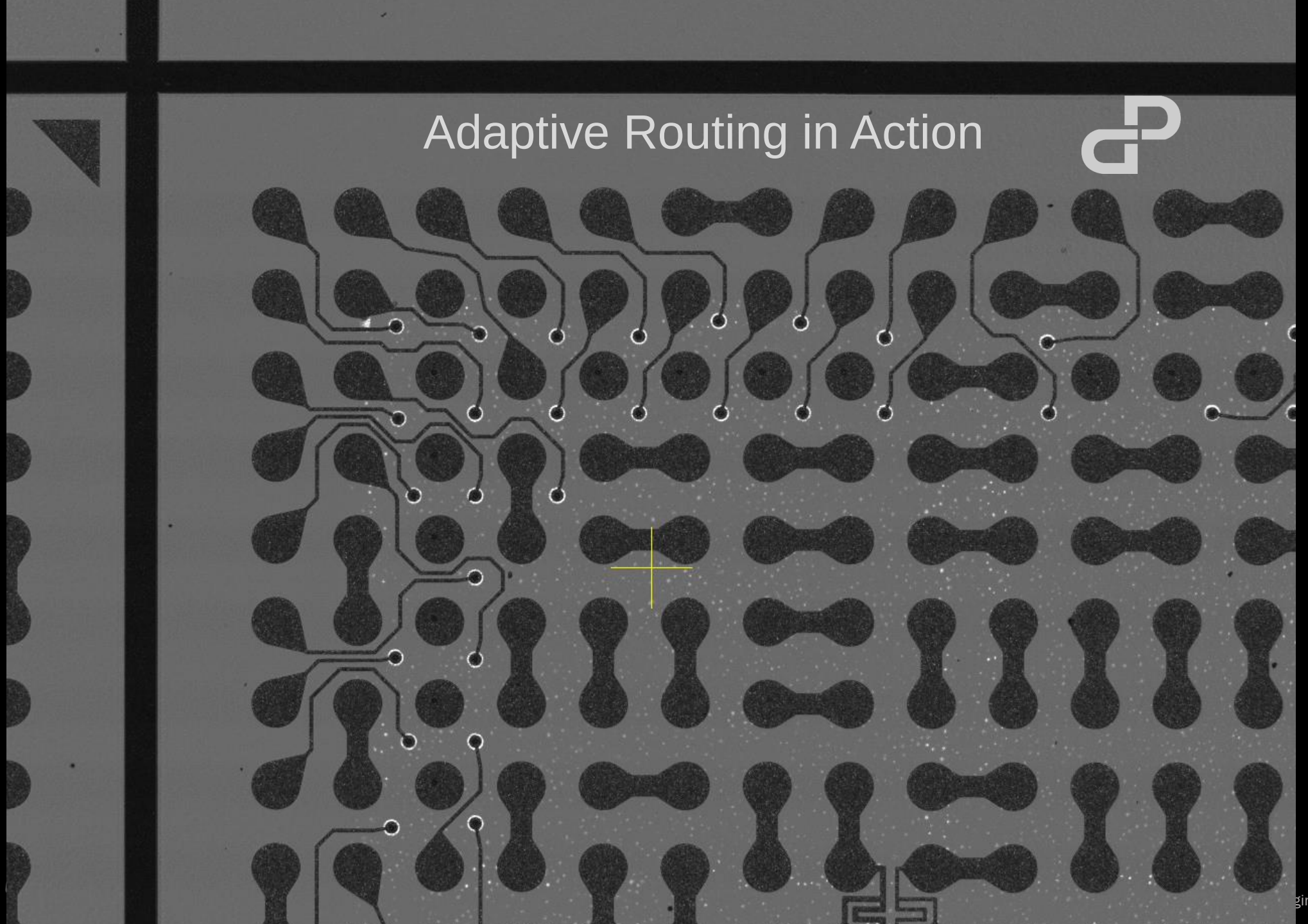
Adaptive Routing in Action



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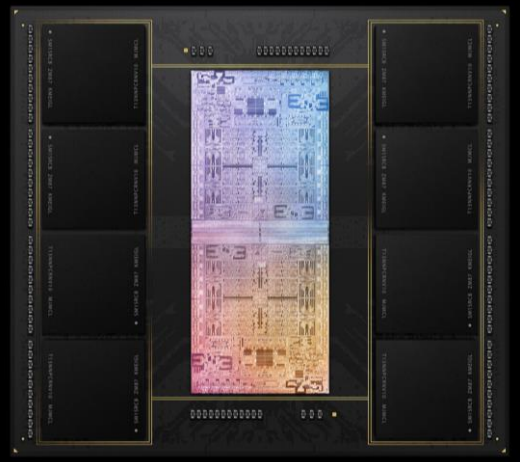
Apple Mac Studio with M1 Ultra Processor – March 2022

M1 Ultra Processor

(Created with advanced packaging)



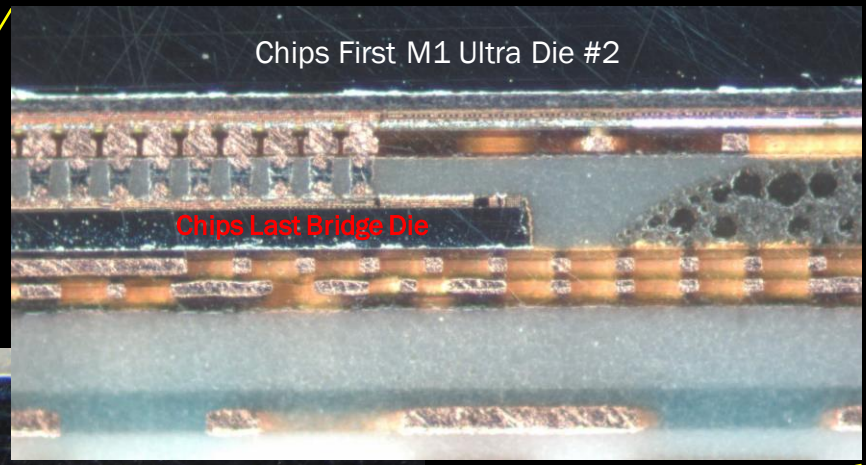
- Two 5nm M1 Max die, 840mm2 (total both die)
- 16 high-performance CPU cores
- 4 high-efficiency CPU cores
- 64 GPU cores
- 32 Neural Engine cores
- 2 Thunderbolt 4 or USB 4 controllers
- 64 or 128GB DRAM (total in 8 packages)

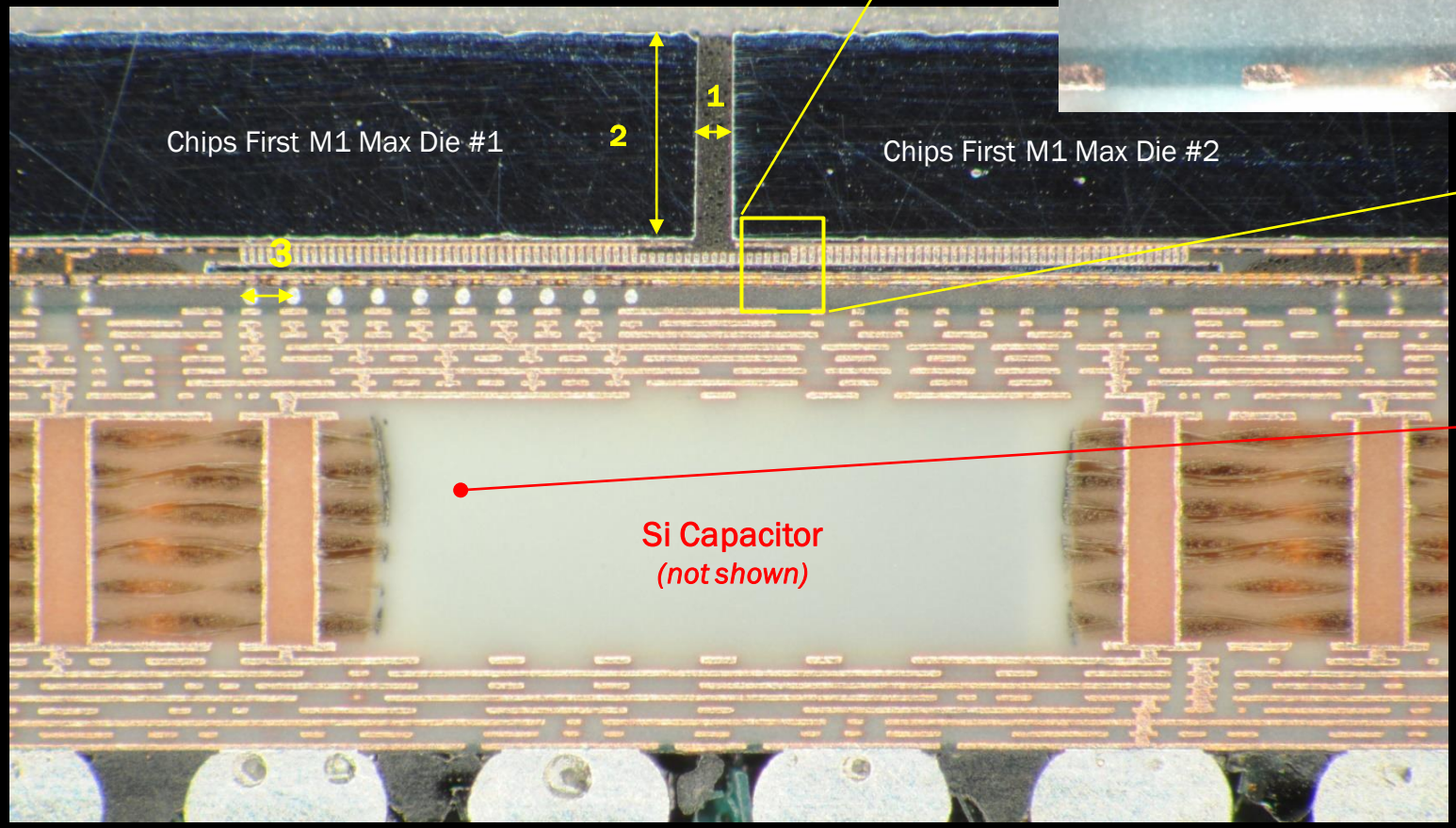
The world's most powerful personal computer, over 22 trillion operations per second

DECA

A Look Inside the Apple M1 Ultra

1. M1 Max die-to-die spacing: 110µm
2. M1 Max die A thickness: 587µm
3. InFo-L ball pitch: Variable 100-150µm





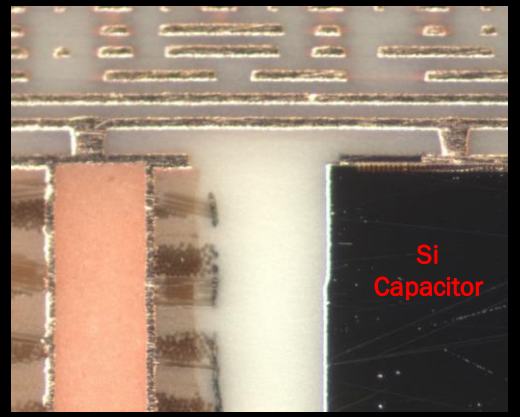


Photo source: Prismark/Binghamton University

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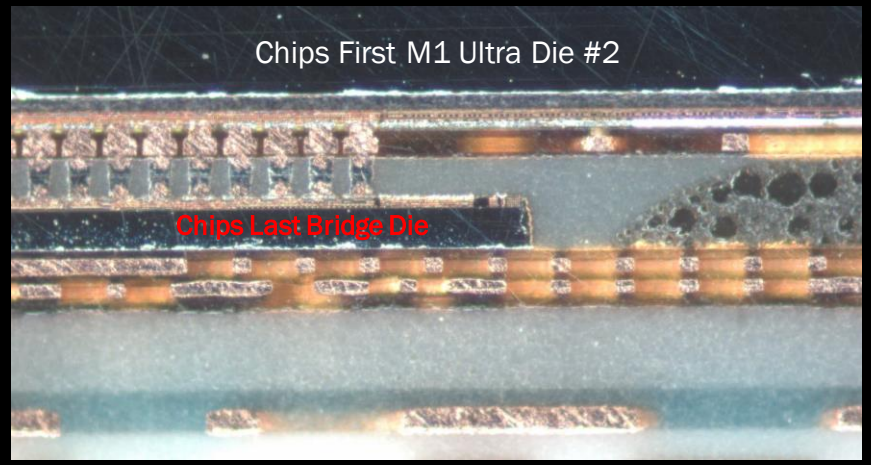
A Look Inside the Apple M1 Ultra



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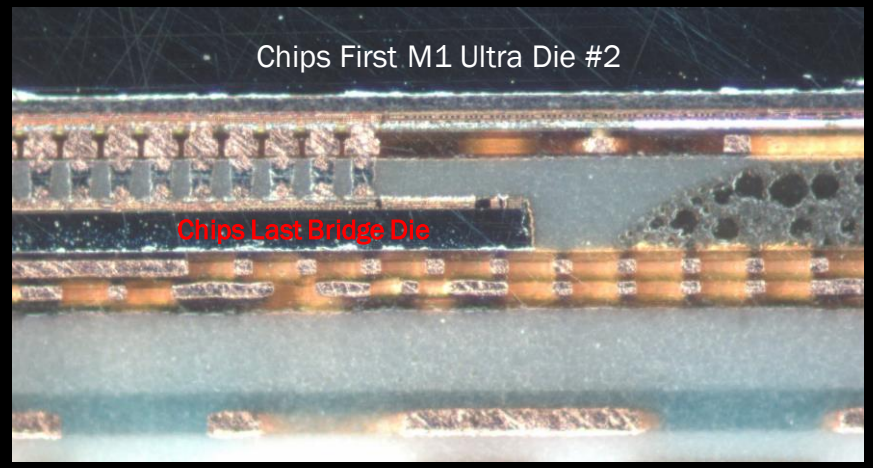
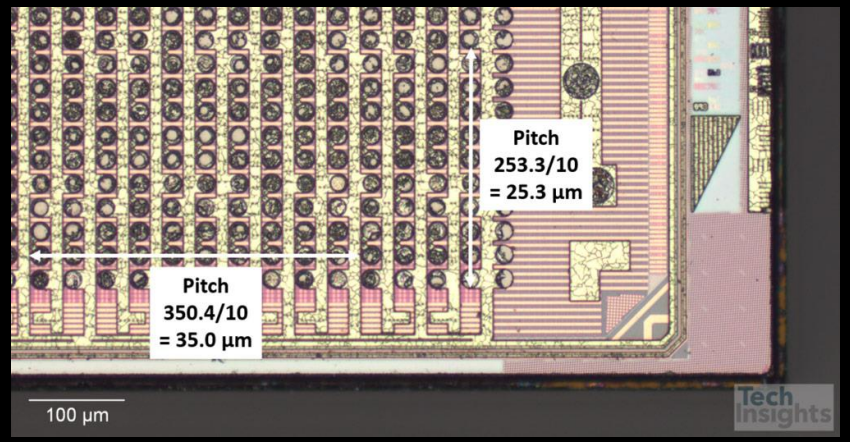
A Look Inside the Apple M1 Ultra

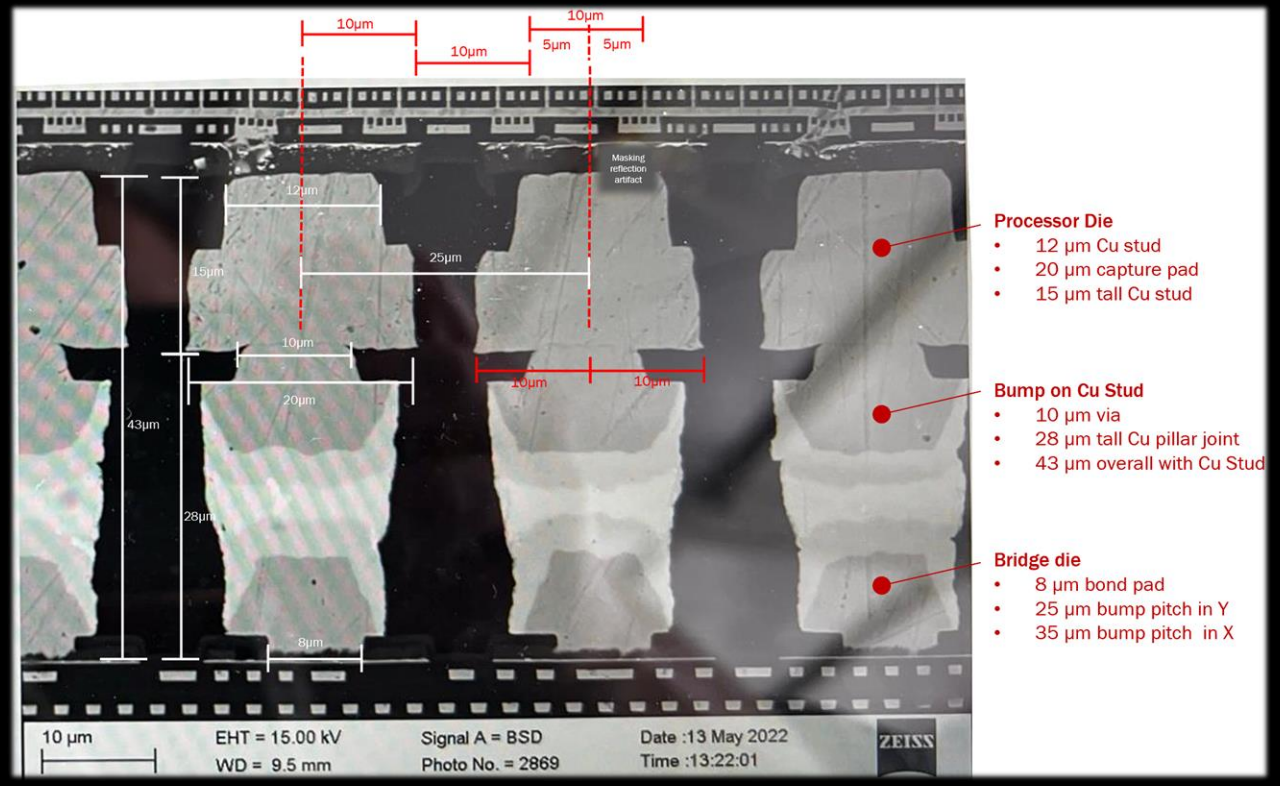




https://www.techinsights.com/blog/apple-joins-3d-fabric-portfolio-m1-ultra

Semiconductor Industry's Most Advanced Packaging (1st half of 2022)

- Ultra fine pitch Cu pillar flip chip bridge die (25µm x 35µm)
- 10,000 bond pads per die for bridge (leading density when introduced)
- **2.5 TB/s estimated bandwidth**



65x72mm TSMC InFO-L fan-out on substrate

- Chips up chips first M1 Max die (2 die)

Major challenge in manufacturing with < 4µm die shift required (x, y & θ after chip attach & mold)

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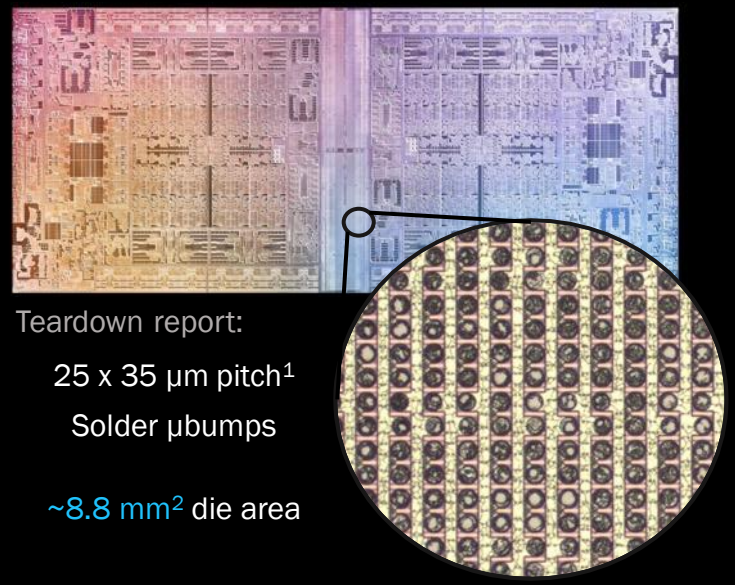
Industry Leading Die-to-Die Bandwidth (M-Series™ with Adaptive Patterning®)

- Industry's most advanced die-to-die interconnect density as of today
- Integrates two M1 Max die
- > 10,000 die-to-die connections

Silicon Bridge



Teardown report:

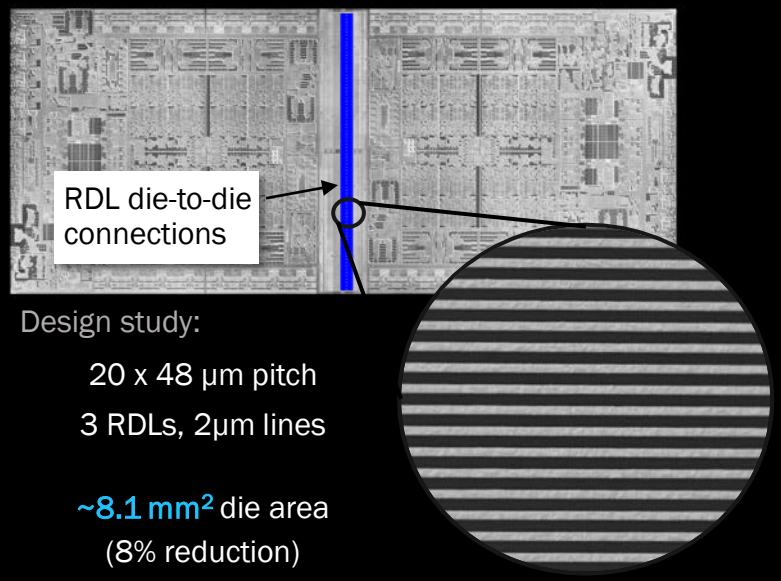
25 x 35 µm pitch[1]

Solder µbumps

~8.8 mm² die area

[1]Techsearch International Inc.

M-Series Gen 2



Design study:

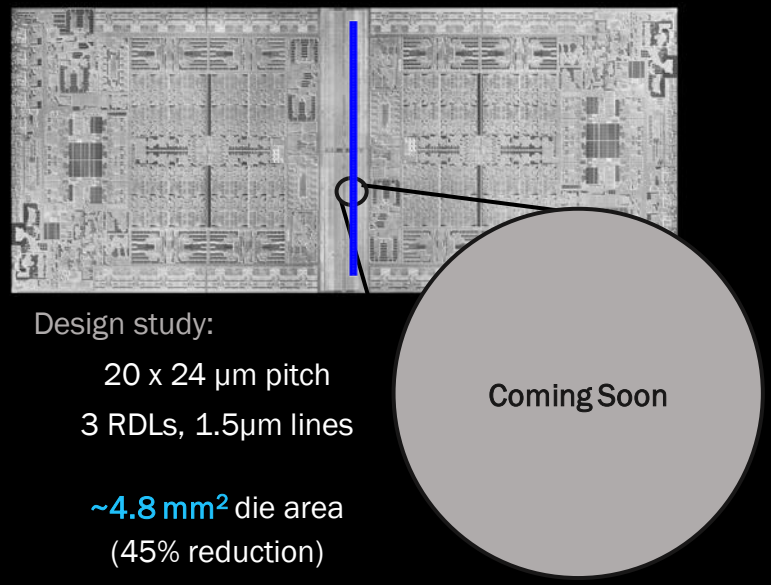
20 x 48 µm pitch

3 RDLs, 2µm lines

~8.1 mm² die area

(8% reduction)

M-Series Direct - MDx



Design study:

20 x 24 µm pitch

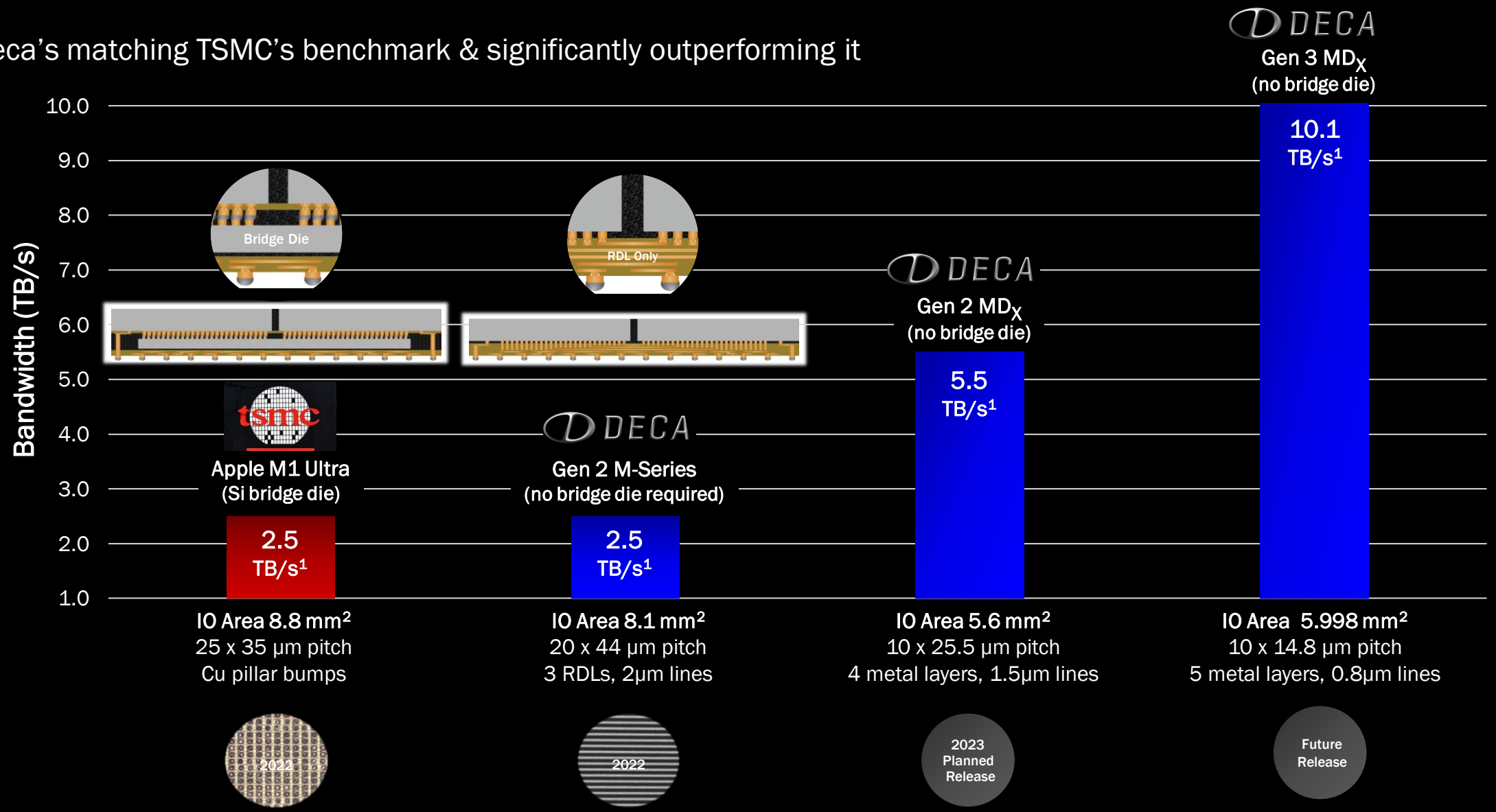
3 RDLs, 1.5µm lines

~4.8 mm² die area

(45% reduction)

Industry Leading Die-to-Die Bandwidth (M-Series™ with Adaptive Patterning®)

Deca's matching TSMC's benchmark & significantly outperforming it



[1] Assumes 20mm beachfront with the same per-wire bandwidth (Gbps) for all cases
[2] Estimated IO area includes signal bumps for one die; ground bumps and guard traces vary depending on implementation

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High-end Gaming PCs with AMD RDNA3 – August 2022

AMD

RDNA 3 GPU

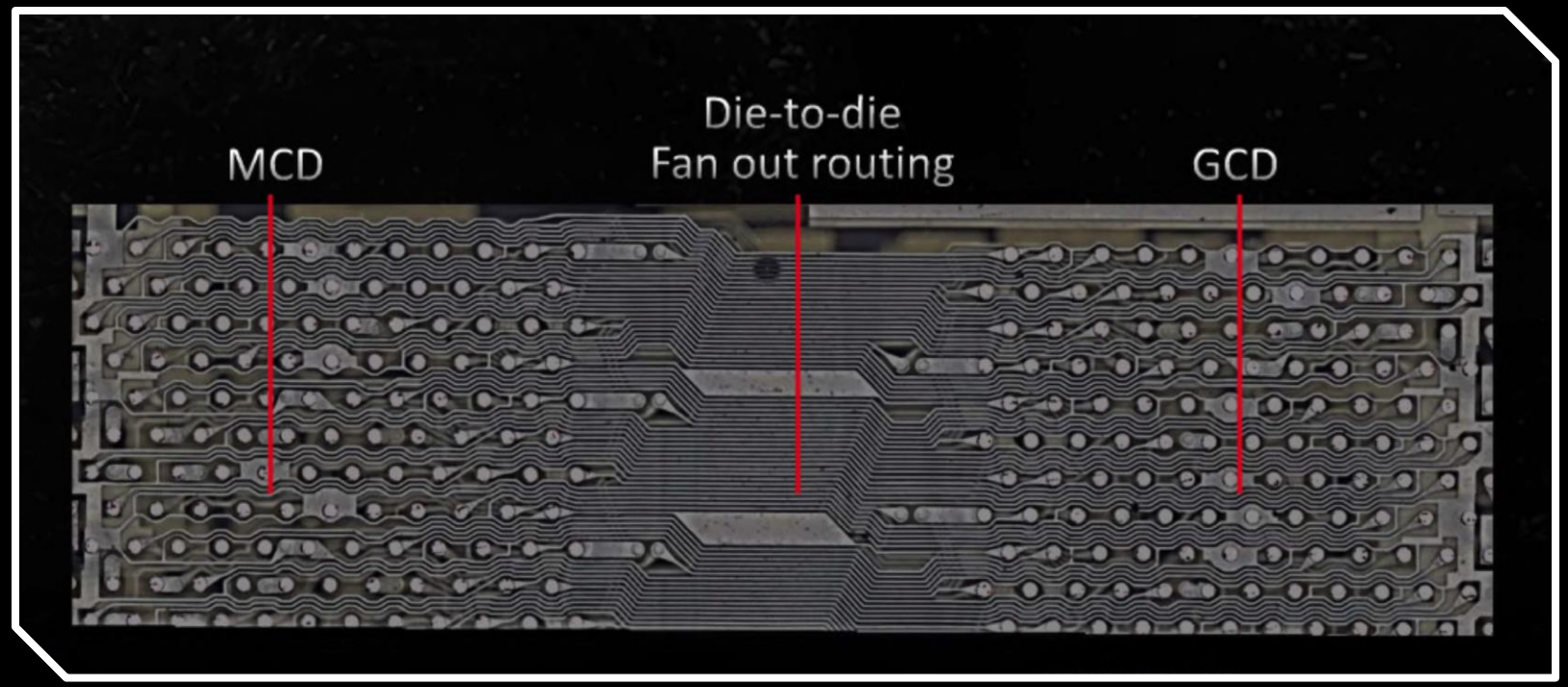
The world's most powerful gaming computers, over 28 teraflops of performance

DECA

A Look Inside AMD's RDNA3

The New Most Advanced Packaging as of August 2022

- Very fine pitch 35µm pitch die bond pads
- 4 layers of RDL – no complicated bridge die required (RDL only)
- **5.3 TB/s spec performance (double the Apple A1 of six months earlier)**

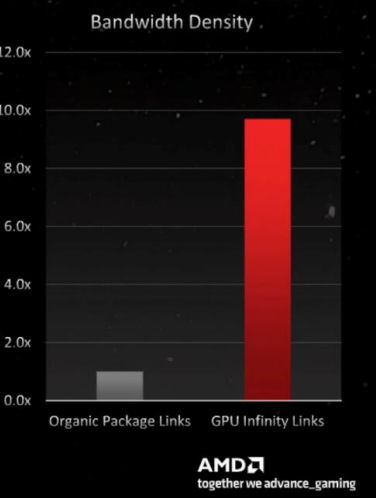


8µm via & 13µm capture pads

- Again, like the M1, < 4µm total die shift required (x, y & Θ after chip attach & mold)
- Significant manufacturing challenge

Can this approach scale in next generation to 25 µm or 20 µm pitch?

RDNA 3 GPU



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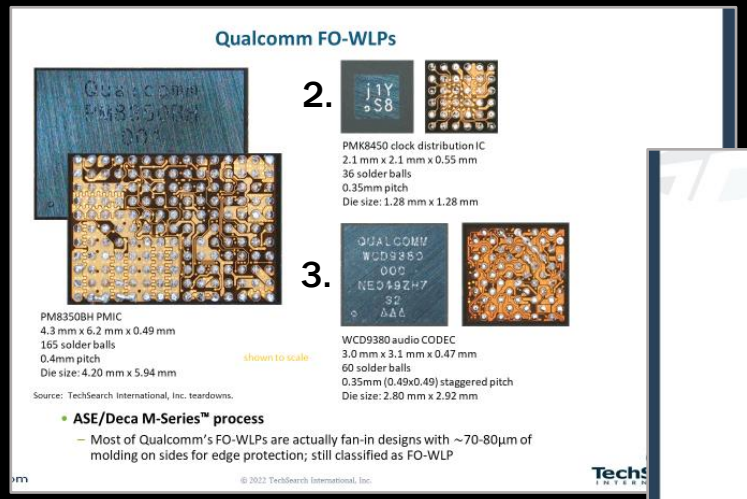
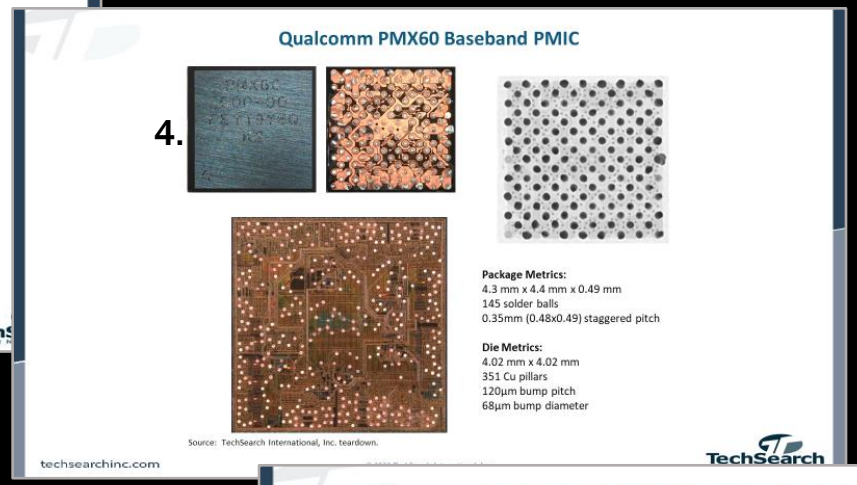
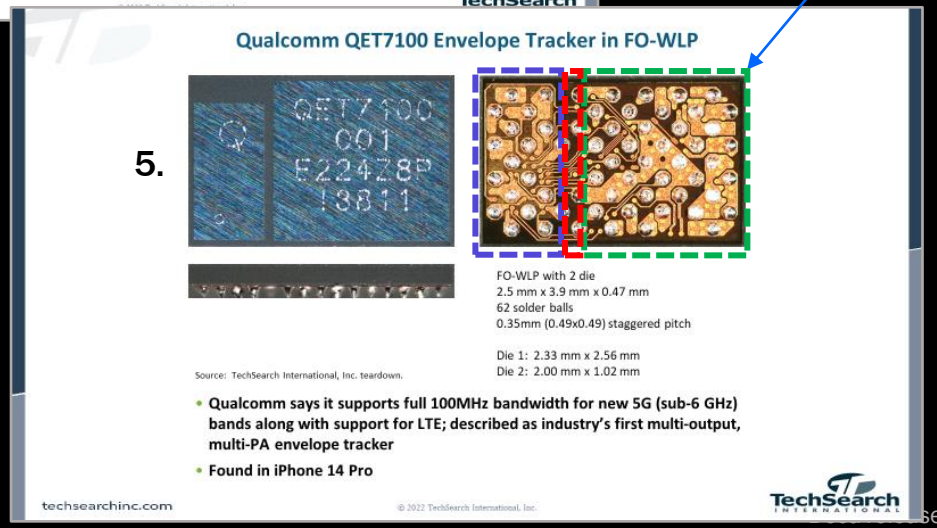
A Look Inside the Apple iPhone 14 Pro Max

5 M-Series devices with Deca's M-Series & Adaptive Patterning inside iPhone 14

1.







Multi-mode Adaptive Patterning® in the iPhone

(Adaptive Alignment + Adaptive Routing)

- Die 1 – Adaptive Alignment
- Die 2 – Adaptive Alignment
- Adaptive Routing Region

iPhone 14 teardown by TechSearch

(M-Series fan-out & protected fan-in)

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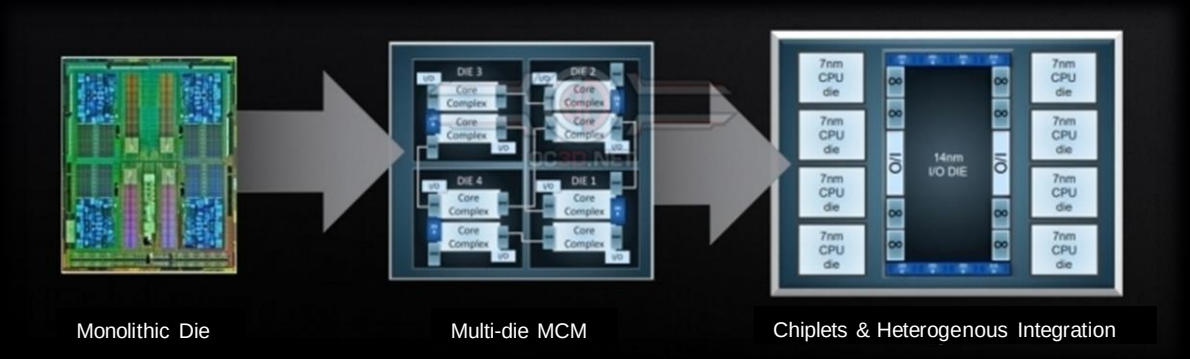
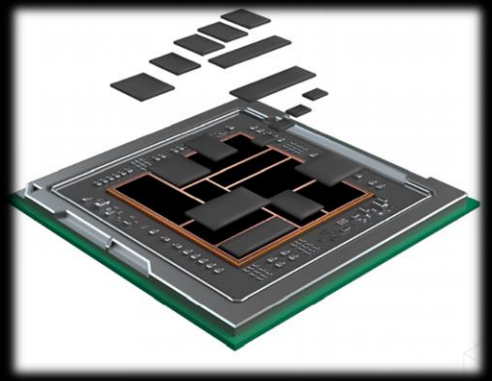
Outline

1. Introduction
2. Challenges in HI
3. Large Panel Solutions
4. 2D Scaling
5. Conclusion

Conclusion

- Chiplets & heterogeneous integration are happening





- Key challenges must be overcome
- Large panel fan-out offers compelling solutions
- Roadmap for continued scaling
- LDI technology coupled with Adaptive Patterning provides the industry with breakthrough scaling capability to 20µm die pad pitch for ultra high-density HI and beyond

Thank you.

Cliff Sandstrom

cliff.sandstrom@thinkdeca.com

Who are we?

Jen-Kuang Fang – Vice President of ASE Corporate R&D Center

- Mr. Steve Fang (Jen-Kuang Fang) is ASE Group's Vice President of Flip Chip, Package Substrate, SESUB (Semiconductor Embedded in Substrate), FOPLP (Fan-Out Panel Level Packaging) and ABF/BT substrate material fields. He is more than 200-patent inventor and has published dozens of journals discussed about packaging technologies. Steve also represents ASE to receive "2011 Taiwan National Invention and Creation Award" and "2012 Taiwan National Industry Innovation Award".
- Since joining ASE in 1992, Steve has played a successful role in delivering each of ASE's innovation IC-package products to customer. He spent 20 years to establish ASE's first plant for flip chip, bumping, 2.5D, SiP (system in package), 5G mmWave, IC-package substrate products, which he led manufacturing and distribution functions for supply chain CSR (corporate social responsibility) management in Taiwan and China fields.
- In scientific research, Steve cooperated with Professor Konstantin Novoselov (Nobel Prize in Physics) of the University of Manchester in the application of graphene in IC-package materials. Steve's team has an excellent track record of building and strengthening world-class packaging technologies that meet and exceed the high expectations of ASE's customers.
- Steve is PhD of DBA (Doctor of Business Administration) from NSYSU (National Sun Yat-sen University), where he is an expert of CSR innovation, and his master degree earned in EMBA (Executive Master of Business Administration) from NSYSU

Ping-Feng Yang – Director of ASE Corporate R&D Center

- Jeffrey Yang (Ping-Feng Yang) is Director CRD of ASE and leading of Project Management of Panel Level Package Development, ASE(ASE Group), where he is currently in charge of new technical development for advanced panel level fan out packaging, He has over 19 years of research focusing on advanced packaging solution (fan-out, embedded packaging, SiP, Adv. FO, 2.5DIC), project management to coordinate end customer and cross function team, including APQP phase management, new product DFMEA & PFMEA & risk assessment control, NPD & NPI phase in, customer engineering total solution of hetero-generous for module & material issue, roadmap alignment and analysis, packaging reliability issues, failed root cause definition, DOEs CZ, design rule and manufacturing process innovations of advanced packaging integration.
- PhD Yang has over 160 technical publications of SCI journal papers and international conference papers, and also is the inventor of more than 22 patents in US, China and Taiwan..

ASE GROUP 日月光集團

Who are we?

Cliff Sandstrom – VP of Technology

- 12 years at Deca
- Over 22 years front-end experience at Cypress Semiconductor
  - Manufacuring
  - R+D
  - Integration

Benedict San Jose, PhD – Principal Materials, Process, and Integration Engineer

- 7 years at Deca
- Doctorate in Materials Science – expertise in Polymer Chemistry
- Over 17 years of Materials Science and Engineering experience in various fields
  - Semiconductor packaging
  - Solar cell fabrication
  - Functional polymer design and synthesis

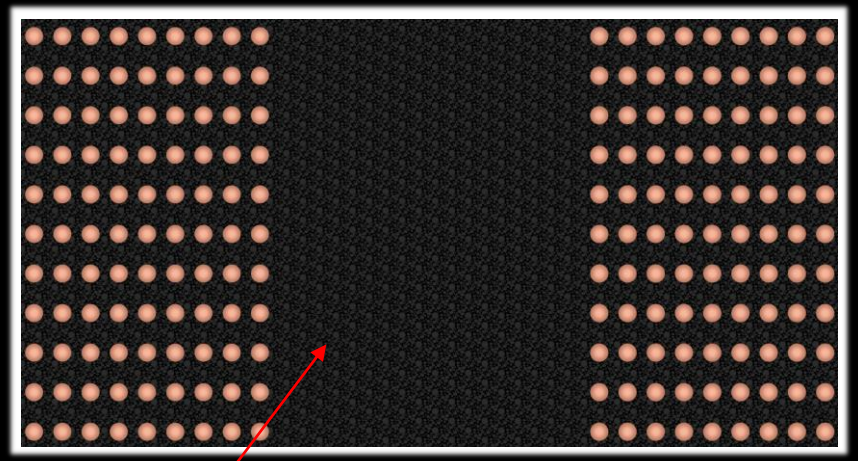
Tim Olson – CEO

- Founder and Director of Deca Technologies
- 37 years of R&D and semiconductor experience at Deca, Amkor, and Motorola
- Prev. Sr. VP of R&D and Emerging Technologies at Amkor Technology

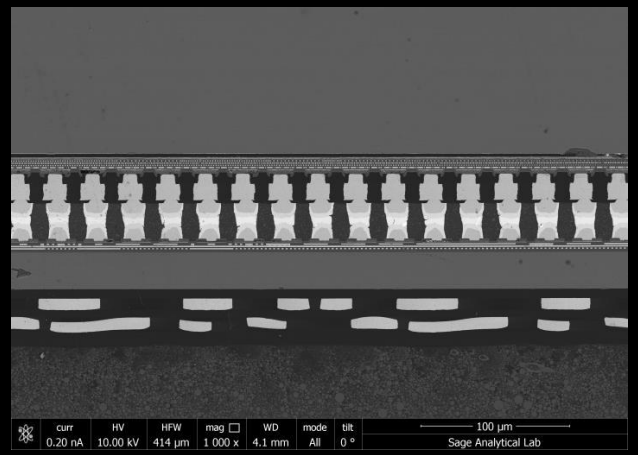
Industry Leading Die-to-Die Bandwidth (M-Series™ with Adaptive Patterning®)

Matching TSMC's Apple M1 Ultra benchmark & significantly outperforming it

1. TSMC InFO Bridge Die Solution



Die-to-Die requires bridge die
15.8 µm UBM pad
25 x 35 µm pitch

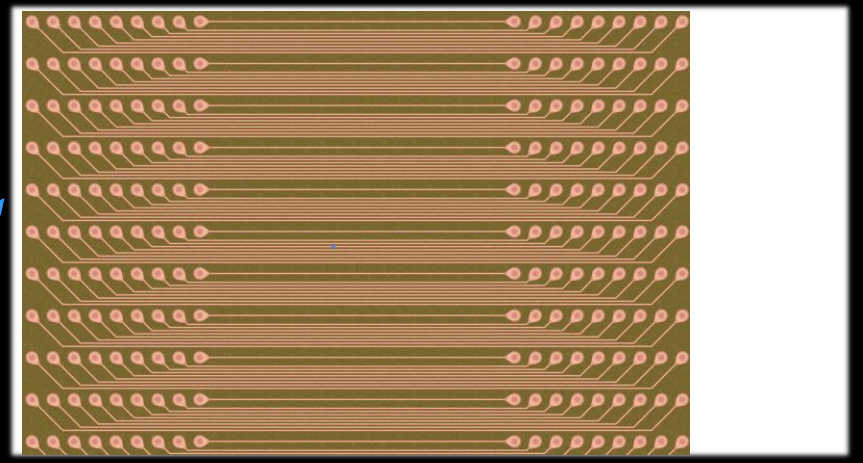


TSMC requires bridge die with challenging flip chip attach

All drawings to scale

Deca solutions much simpler with RDL-only

2. Deca M-Series Gen 2C (to scale)



White box = TSMC M1 Size

Die-to-Die interconnect in RDL
1.5 µm line & space, 14um capture pad
20 x 40 µm pitch

3. Deca Gen 2 MDx (M-Series Direct with no capture pads)

MDx interface size
(image under NDA)

DECA