Tektronix
Component Solutions

Validating Flip Chip package models through experimental deflection measurements

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Tektronix is advancing its simulation capabilities to improve product reliability, reduce costs, and speed up time-to-market.

Research Objective:
To validate model accuracy through correlation to real-world results

Outline

- Project Introduction and goals
- Simulation Model
- Experimental warpage methods
- Warpage Measurement Correlation
- Experimental strain methods
- Strain Measurement Correlation
- Closing Remarks

Validating Flip Chip package models through experimental deflection measurements

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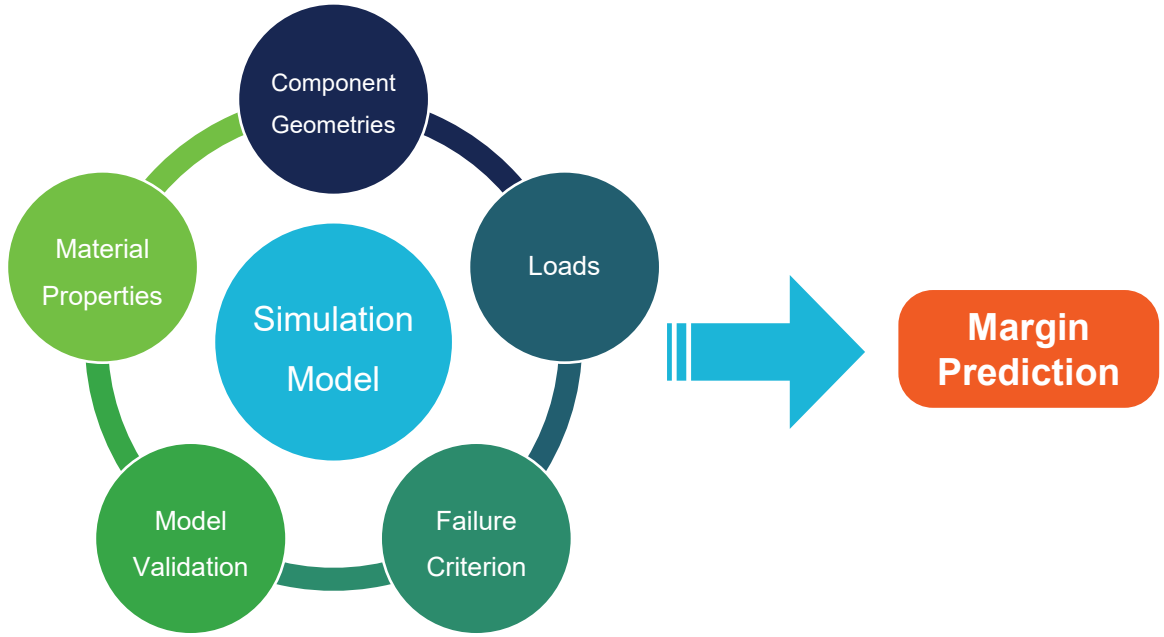
Project Goals

Primary Goal

Improve Design optimization and failure prediction

- Validate simulation models based on physical package measurements



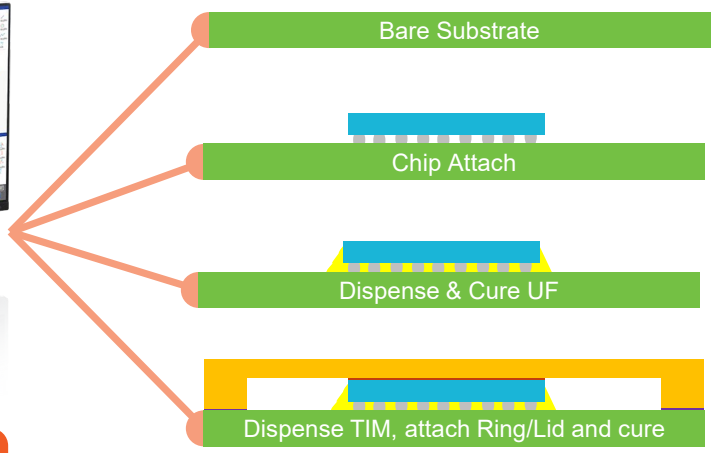
Long-term:

Increase yield and package reliability

- Integrate warpage measurements as part of fabrication process

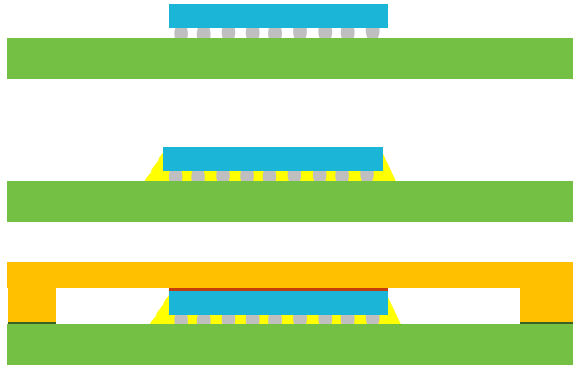
Measurements after each step

Flip-Chip packaging process



Evaluate Warpage during Flip-Chip Package Process

Physical Assembly



Flip-Chip Attach

Dispense & Cure Underfill

Dispense TIM, Attach Lid and cure

Thermal Loading

Reflow C4 bumps (solidification at 220C)

Underfill Cure temperature

TIM and Lid adhesive cure temperature(s)

Deformations & Stresses arise from:

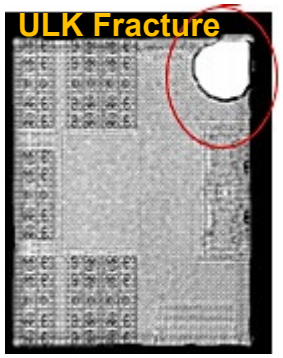
- Addition of new components
- Differences between component CTE
- Magnitude of Temperature change

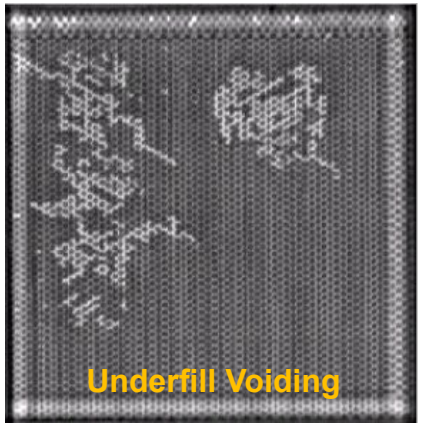
They are functions of:

- Component stiffness
- Temperature ramp rate
- Dwell time

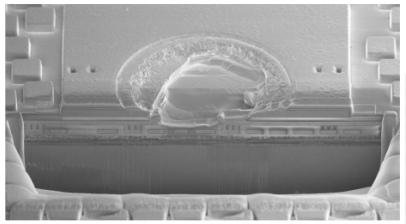
Failure modes during fabrication

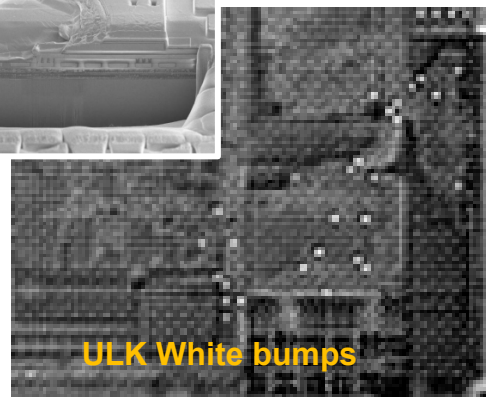
- Component fractures and delamination
  - Die ULK
  - Adhesive delamination
- Adhesive voids and non-wetted regions
- Solder bump reflow problems
- Excessive warpage
- Tolerance stack-up
- Uneven bond lines

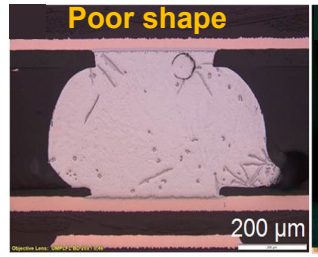


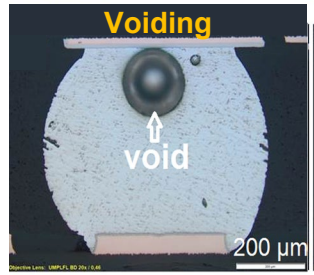


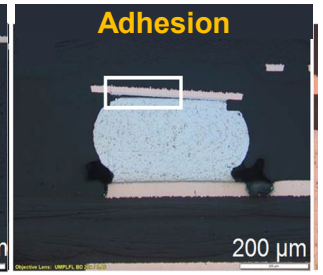
[Wang, 2006]







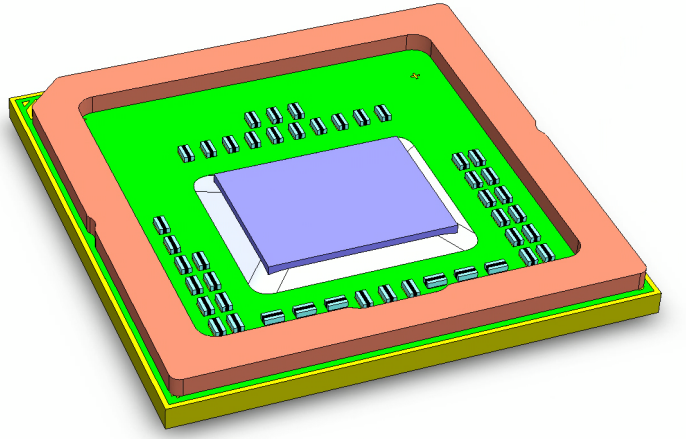


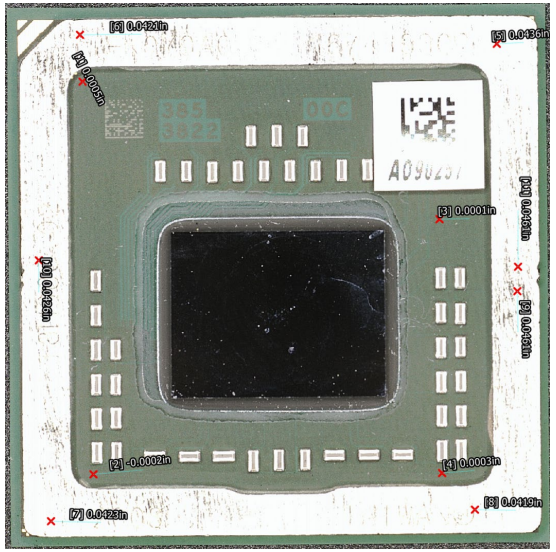


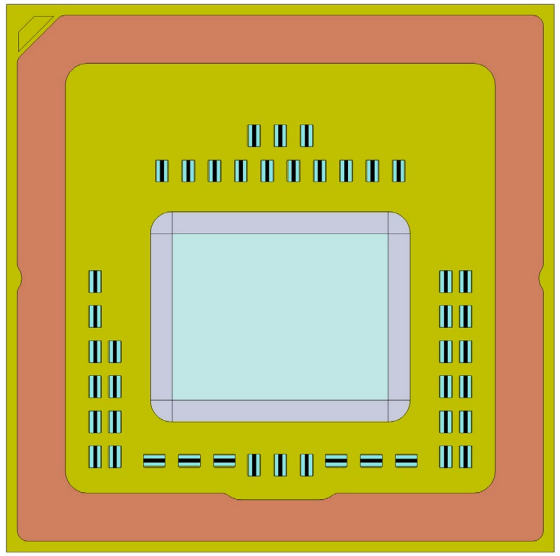
[Grosshardt, 2019]

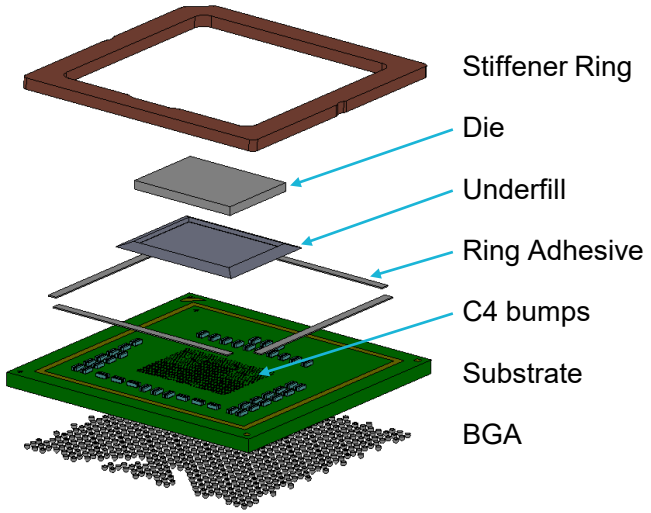
Details of Flip Chip Package

- In-house designed advanced node CMOS Flip Chip
- 10 x 8 mm IC with 180-micron bump pitch
- 25 x 25 mm organic substrate with 800-micron BGA pitch
- Stiffener ring
- Package height 2.68 mm





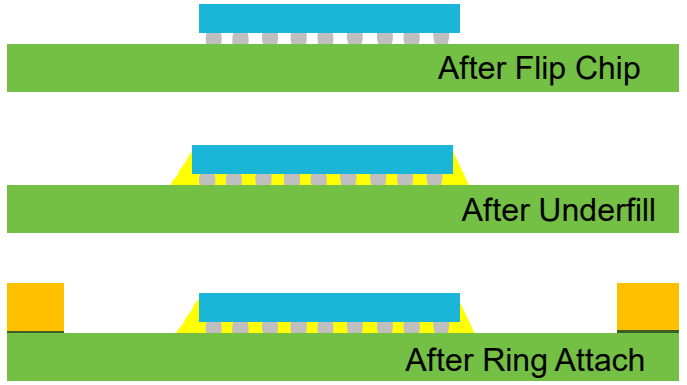


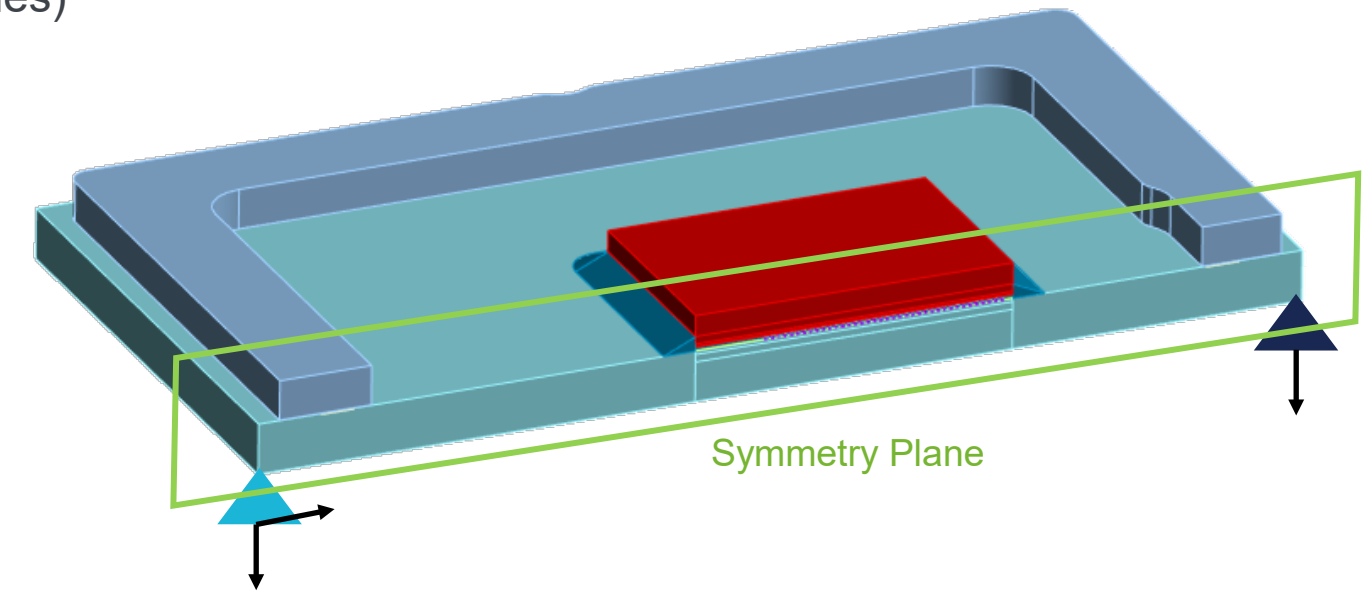


Simulate with Finite Element Method

Goal: simulate package assembly and extract results to correlate to experimental measurements

- Solver:
  - Ansys Mechanical 2022
  - Multi-step, large deformation
  - Quadratic elements (134k elements, 698k nodes)
- Geometry and Boundary Conditions
  - SMT not included
  - ½ symmetry conditions
  - BCs at substrate corners
- Outputs:
  - Warpage
  - C4 bump strain



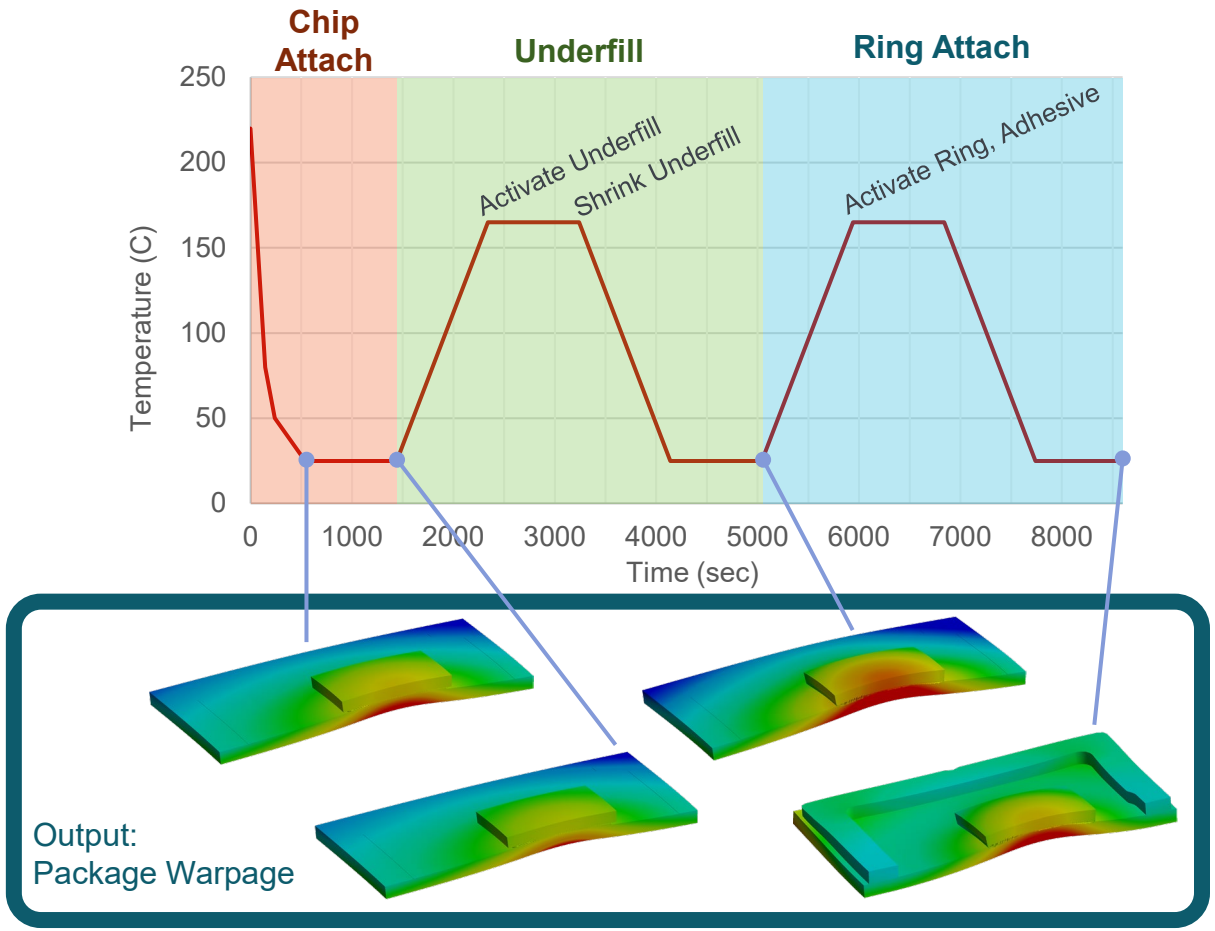


Finite Element Simulation

Components and Materials

Component	Material	Key Properties	Source
Die (bulk)	Silicon	Orth. Modulus, CTE, *v*	Literature
Die Active Layers	Composite	Orth. Modulus & CTE, *v*	Calculated/Literature
Die C4 Pad	Copper	Bilinear Modulus, CTE, *v*	Literature
Solder Bumps	Solder	Viscoplasticity, CTE, *v*	Literature (Anand)
Underfill	Adhesive	Viscoelasticity, CTE, *v*	**Lab Test**
Subs. Solder Mask	Elastomer	Modulus, CTE, *v*	Literature
Substrate	Composite	Viscoelasticity, CTE, *v*	**Lab Test**
Stiffener ring	Metal	Modulus, CTE, *v*	Literature
Ring Adhesive	Adhesive	Viscoelasticity, CTE, *v*	**Lab Test**

Assembly and Load Steps



Experimental Warpage Measurement Plan

3D Optical Scanning – Can this tool be integrated in process flow?

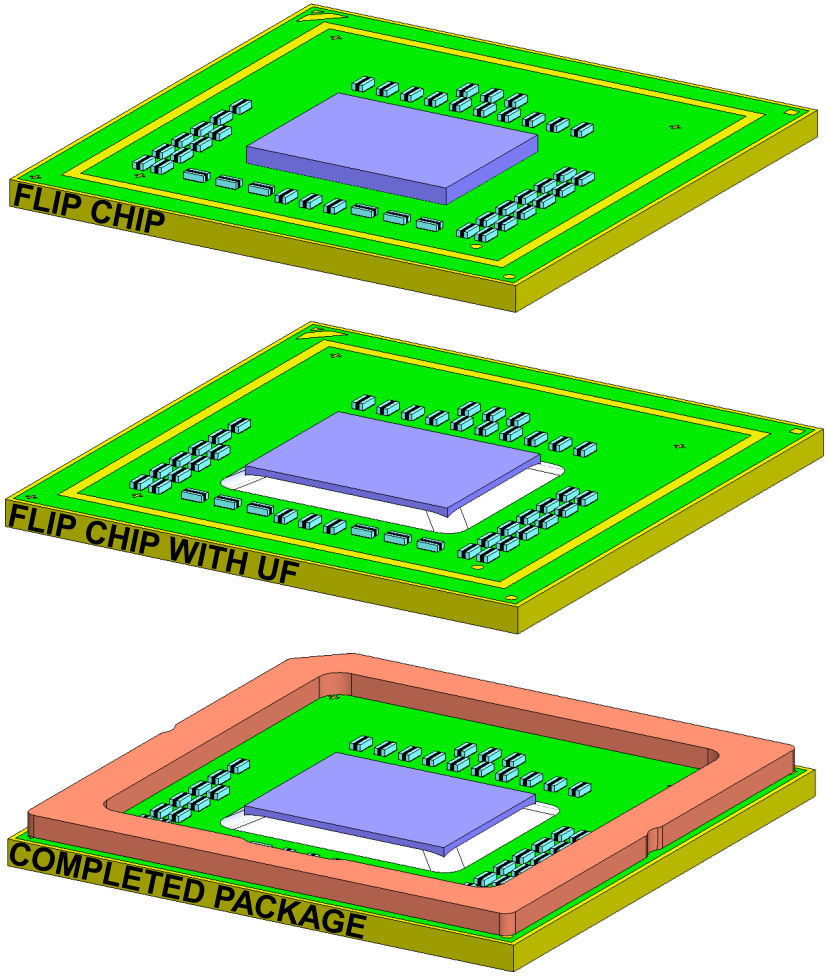
Entry level: Fast, Small footprint, easy integration in process flow

- Keyence VR-5000
- Accuracy of 2.5 µm
- Room temperature only
- Measure Warpage as a function of process step
  - **6 packages were measured after each assembly step**

Thermal Projection Moiré – Industry standard tool

High-end: high accuracy with thermal control

- Accuracy of 1 µm
- Measure Warpage as a function of process step
  - **3 packages were assembled to different assembly steps and measured**
  - **Thermal load applied to each (partial) assembly and warpage measured**

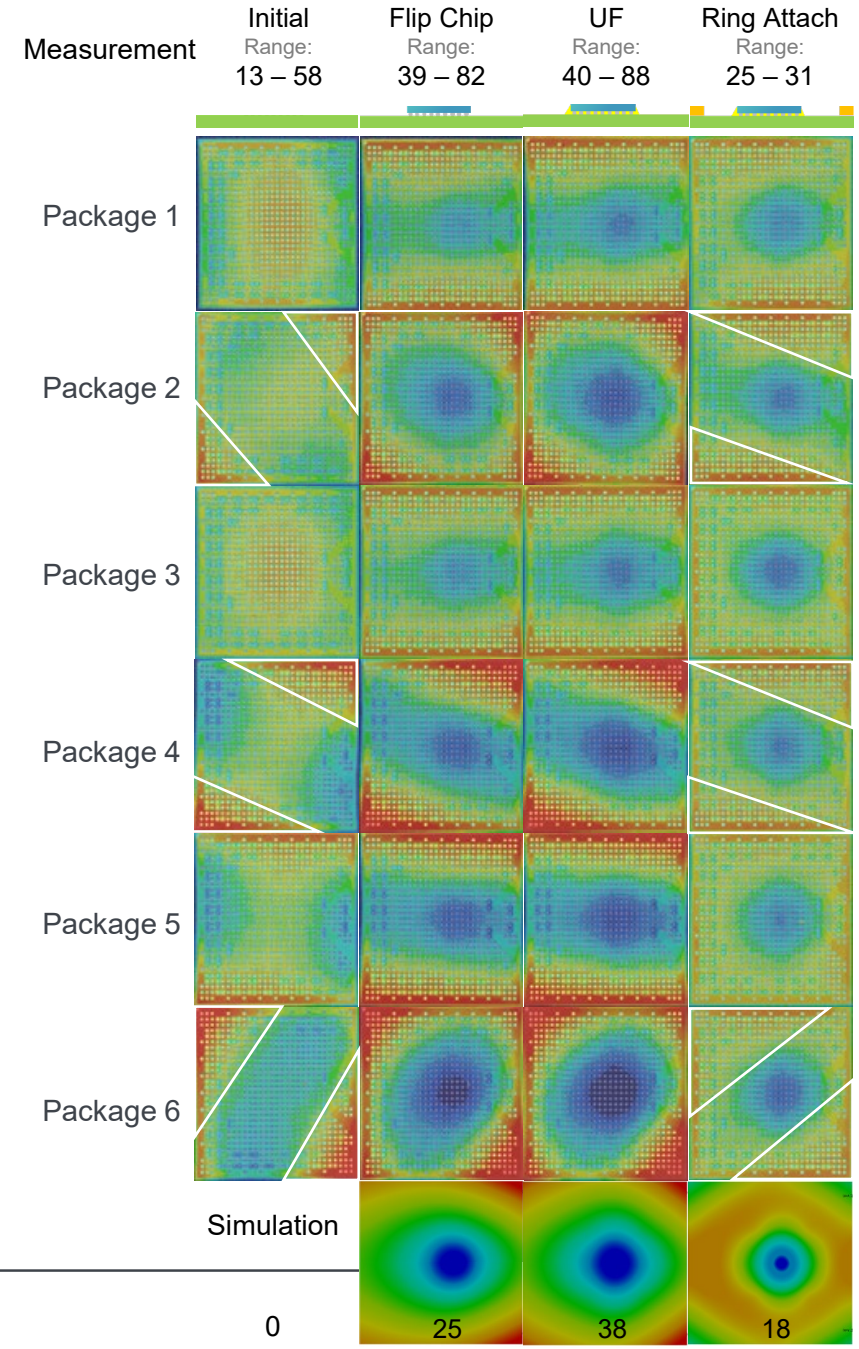


3D Optical Scan Results

Can this tool be integrated in process flow?

- Die measurements were unsuccessful (high reflectivity)
- Substrate measurements were successful
- Significant pre-warpage in substrate influenced results
  - Design Spec: Flatness < 100 microns
  - Still visible in complete package
- Simulations assumed flat substrates (no pre-warp)
  - Captured correct warpage direction and shape
- Pre-warpage of Ring was not investigated
- Further work is needed to for the 3D Optical Scanning system
  - Improve die opacifying method
  - Account for component pre-warpage (in simulation)

- The tool has the capability for warpage measurements
- Substrate is a difficult component to use for simulation warpage correlation because of pre-warpage



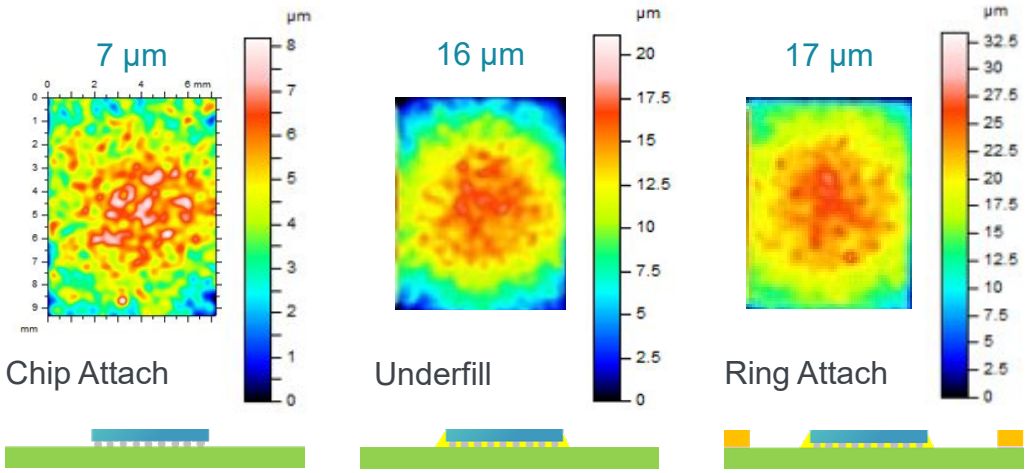
Projection Moiré Results

Method 1

Measure warpage from processing steps

- Measurements on 3 individual packages
- The substrate in each package had its own unique pre-warp
- Die surface was the most relevant for correlation to the simulation
  - Opacifying spray influence can be seen in results

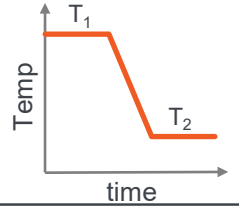
Die warpage:



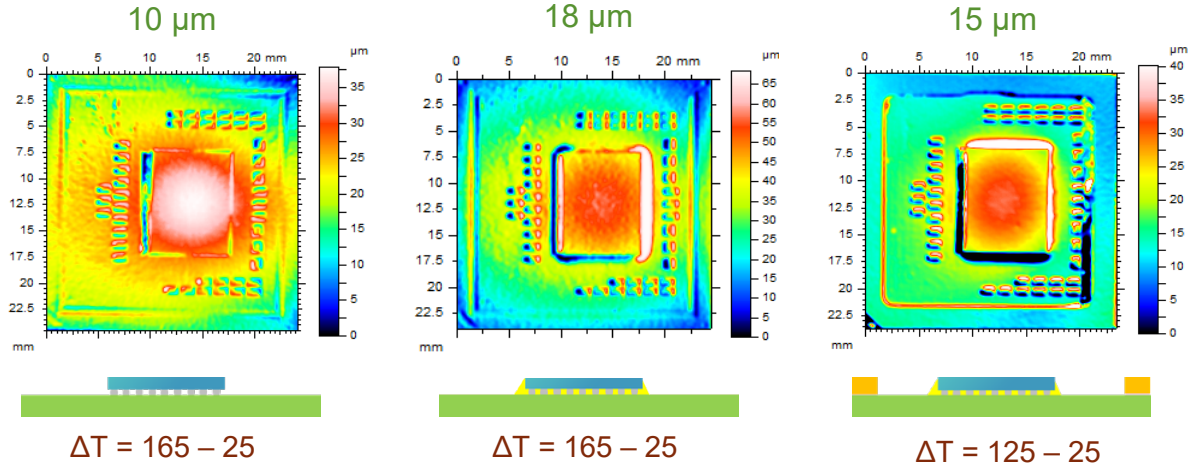
Method 2

Measure warpage change from thermal load (delta T)

- Measurement performed on each (partial) package
- Eliminates variation between package builds inherent to Method 1
- Die surface was the most relevant for correlation to the simulation



Die warpage:

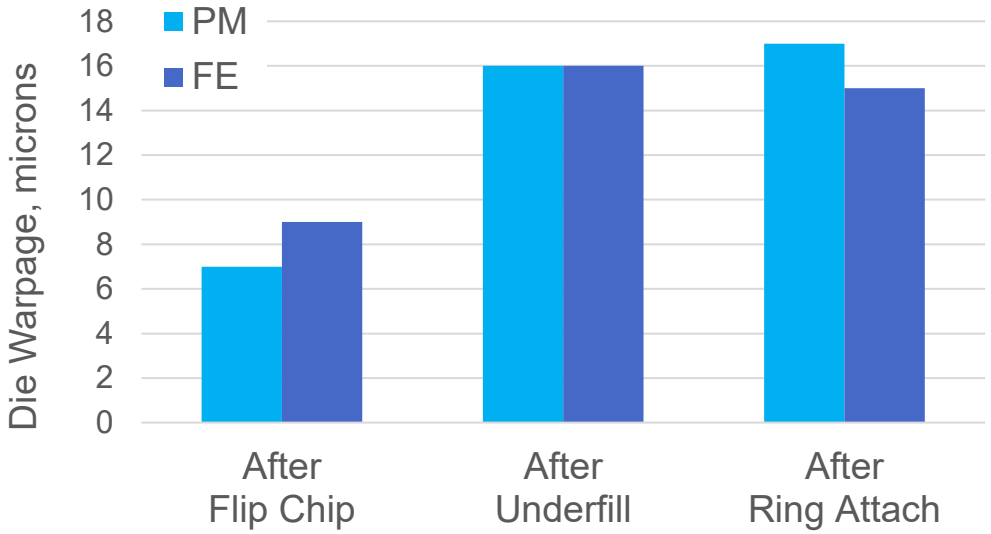


Warpage Correlation: Sim vs Projection Moiré

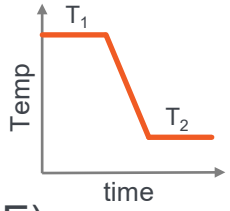
Method 1:

Die warpage during package assembly

Projection Moiré (PM) versus Simulation (FE)

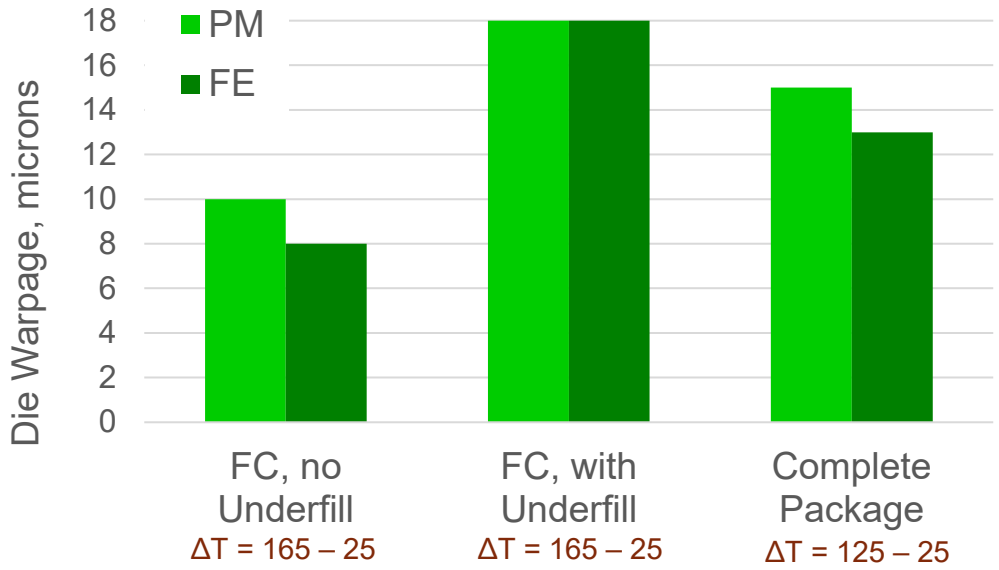


Method 2:



Die warpage during thermal load

Projection Moiré (PM) versus Simulation (FE)



Conclusion: **Excellent correlation – within 2 microns at each assembly step and thermal load**

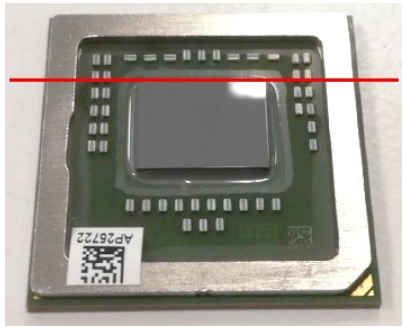
This is the result from extensive materials characterization and model refinement

Package Strain measurement methods

Digital Image Correlation (DIC) or Deformation mapping

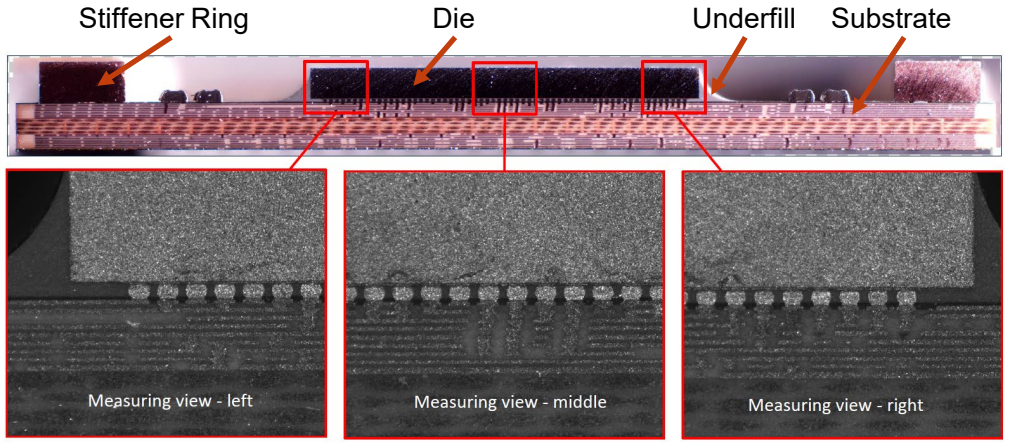
VEDDAC 7 — Chemnitzer Werkstoffmechanik GmbH

- Instrument: 5.1 MPx camera with VEDDAC 7 DIC software
- Surface Preparation not required
- Tracks displacement of surface contrast/specular makers
- Strains calculated as a function of load (temperature change)



C4 bump deformation measurement approach

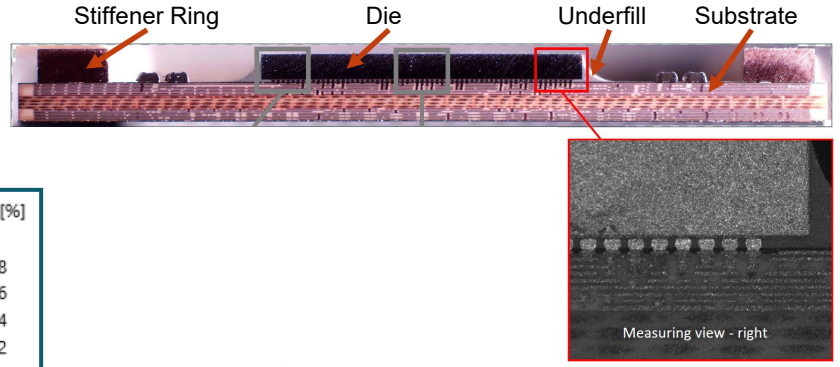
1. Cross-section package
2. Clamp package in thermal chamber
3. Focus camera to region(s) of interest
4. Thermally load package



Study of C4 bumps requires cross-sectioning, adding uncertainties

- Cutting operation
- Creation of “free surfaces”
- Removal of parts and features from the package
- Fixture clamping

C4 Bump Strain correlation



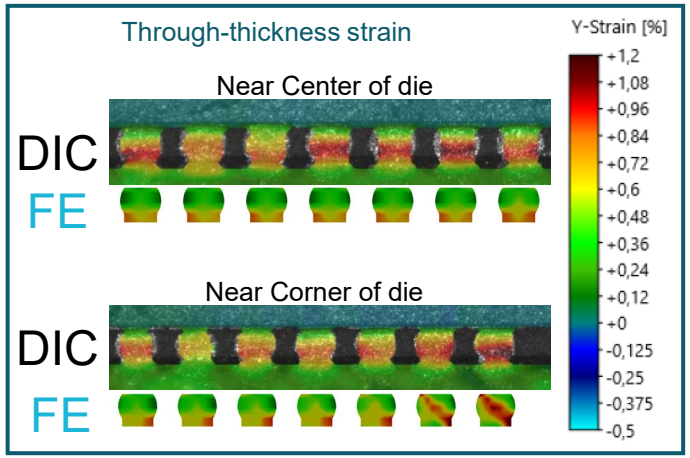
Thermal Ramp: 25 – 125C

total strain = thermal + elastic + plastic

Results:

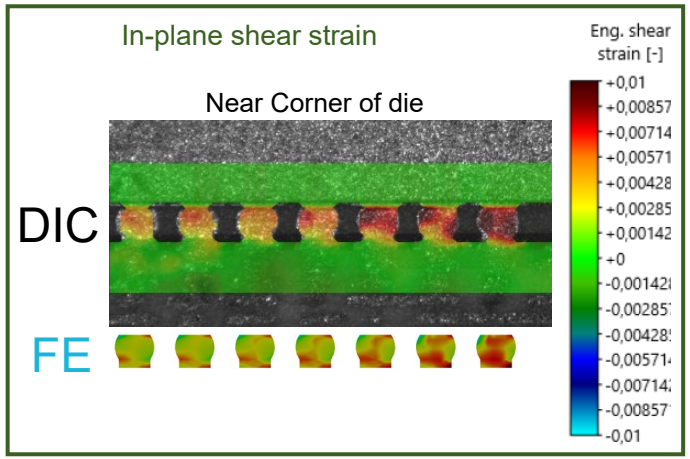
Through-thickness strain

- Magnitude: good correlation, ~1 – 1.2% max
- Distribution: some correlation
  - Within Bump (yes), Die location (no)



Shear strain

- Magnitude: good correlation, ~0.8 – 1.0% max
- Distribution: some correlation
  - Die location (yes), Within bump (no)



Key differences/model limitations:

- Simulation model not cross-sectioned
  - Removal of parts and features
  - Local influence of cutting operation
  - Creation of free surfaces
- No Interaction between bumps and UF
- No Substrate vias or copper traces
- Not clamped like DIC setup:

Conclusions:

Reasonable correlation of strain magnitude.

Further modelling work is needed to match physical strain distributions

Future Work

Primary Focus: Modelling

Apply methods to more advanced packages

C4 strain correlation for local (bump) stresses

Incorporate pre-warped substrate

Include post-processing steps

- BGA reflow
- Bake-out
- Test fixture loads

Long-term focus: Measurements

3D Optical Scanning

- Reduce die reflectivity
- Measure warpage of each component before and after assembly
- Build component/package warpage database

Thermal Projection Moiré

- Continue use as standard model validation tool

DIC

- Use to further define C4 bump strain “target” in sim

Summary

- Simulation warpages were compared to physical measurements after Chip attach, after Underfill, and after stiffener ring attach
- DIC was performed to characterize C4 bump strains during thermal load
- Simulation produced excellent correlation with experimental warpages and good correlation with C4 strain magnitudes
- Considered 3D Optical Scanning: non-contact, repeatable, easily integrated into flow
  - Tool has the capability but struggled with reflectivity
- Component pre-warpages are important to measure and need to be considered in simulation model

Thank you

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Component Solutions

QUESTIONS

Validating Flip Chip package models through experimental deflection measurements

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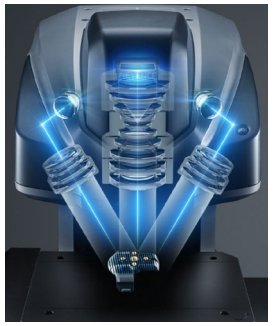
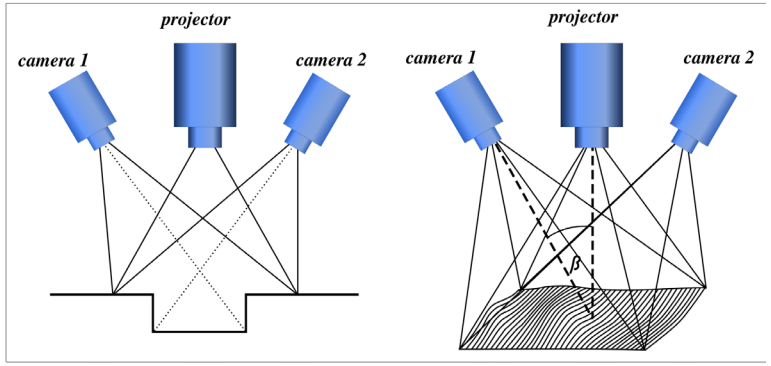
Package Warpage Measurement methods

3D Optical Scanner (Structured light) performed in-house

Entry level: Fast, Small footprint, easy integration in process flow

- Instrument: Keyence VR-5000 3D optical scanner
- Accuracy of 2.5 µm
- Room temperature only
- **Measure Warpage as a function of process step**

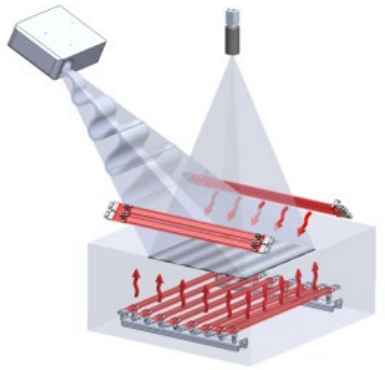




Thermal Moiré (Fringe Projection) performed by external lab

High-end: high accuracy with thermal control

- Instrument: TDM Compact 3 – 12MPx
- Accuracy of 1 µm
- Can be used over full temperature range
- **Measure warpage as a function of process step and thermal load**



Both methods use similar measurement approach

1. Structured light projected onto package
2. Lens(es) detect light which appears bent based on topography of surface
3. Triangulation to calculate and measure surface height