Toward Thinner and Higher Heat Dissipation Advanced Chip Embedded Power Supply Module Packaging

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AOI ELECTRONCS CO., LTD.

Outline

- Background
- Introduction of Our Coreless Chip Embedded Technology
- Trial production and evaluations for a Prototype
  - Manufacturing flow
  - Process flow
  - Package structure
  - Prototyped package
  - Package warpage
- Summary

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Background

■ Applications : Power Supply System

Source : NTT Corporation

Source : TOYOTA corporation

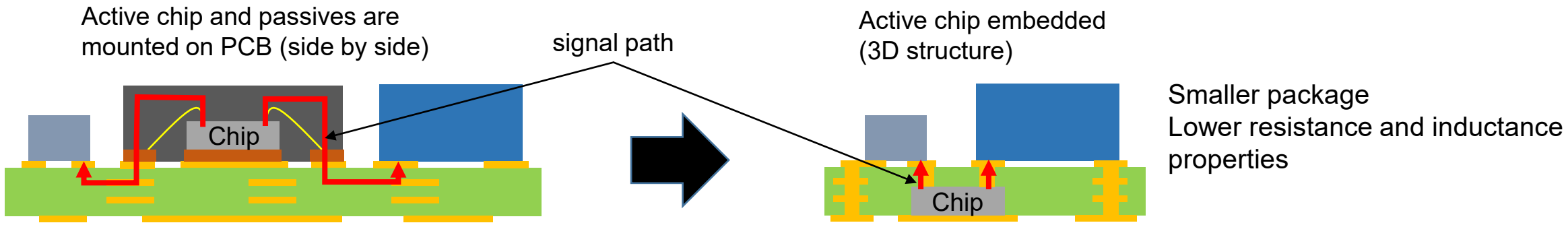
- ✓ Data centers and various power supply equipment shift from 12V to 48V systems.
- ✓ As power supply output current increasing, wiring resistance is a big issue about power distribution loss.
- ✓ Placing the power supply near the processor (CPU/GPU) will be an important for power integrity.
- ✓ Chip-embedded packages (PoP/CoP/3D-SiP) can shrink size and increase current density.

According to Texas Instruments 's white paper, they have brought an average module size reduction of 25 percent annually.

Source : U. Chaudhry et al, SiP Power Modules White Paper “Powerful solutions come in small packages”, Texas Instruments, page2

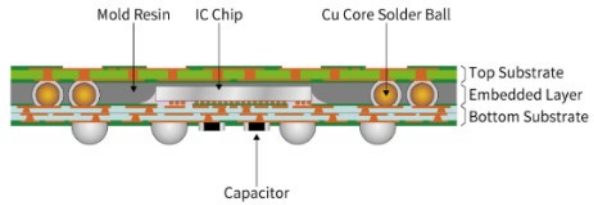
Background

■ Packaging Technologies



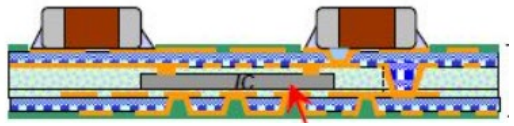
Chip Embedded package trends of each company

MCeP



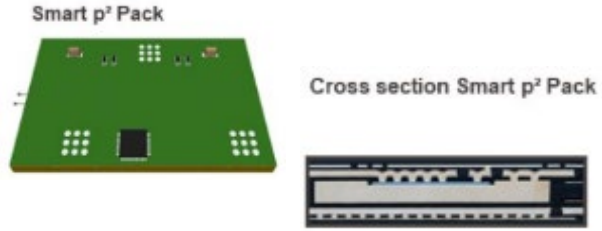
Source : SHINKO Corporation

SESUB



Source : TDK Corporation

Smart P2 Pack



Source : Schweizer Corporation

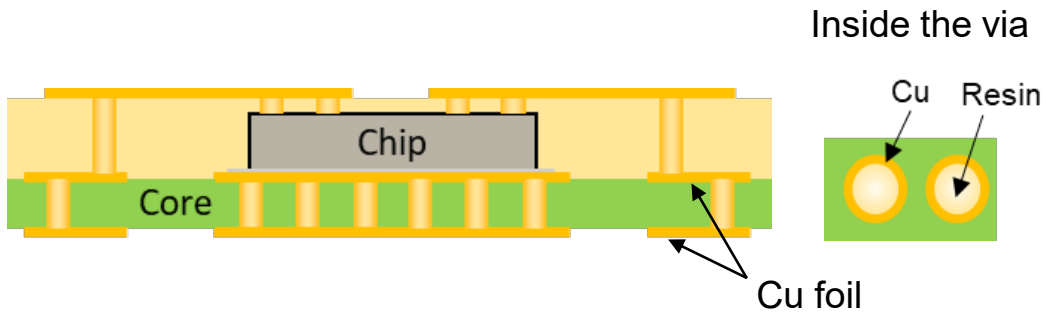
Recently, several chip-embedded packages have been proposed.
We want to propose a new thinner and higher heat dissipation coreless package structure.

Background

■ Concerns about reducing thermal resistance with PCB prepreg substrates

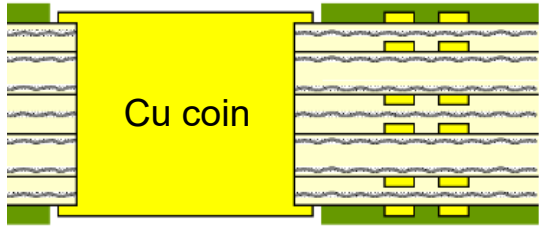
✓ Cu foil + core material

Difficult to form large vias due to glass cloth as disturbance.
Also difficult to fill with Cu in the via due to thick plating requirement.
Thinning down is limited due to thick core material.



✓ Cu inlay／coin

Cu coins are large in size and thick, so difficult to make smaller and thinner.
And, there are also layout design restrictions.
Built-in process has difficulty affecting productivity and cost.



Source : ELNA PRINTED CIRCUITS corporation

Source : FINECS corporation

For power applications, PCBs based structure size/thickness, heat dissipation properties, and cost are still non-negligible issues and consequently necessitate the development of further concepts.

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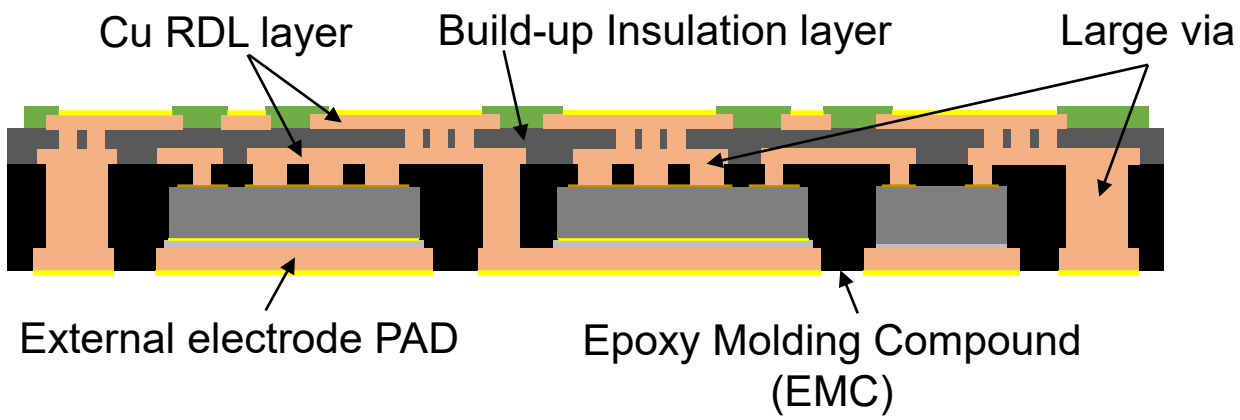
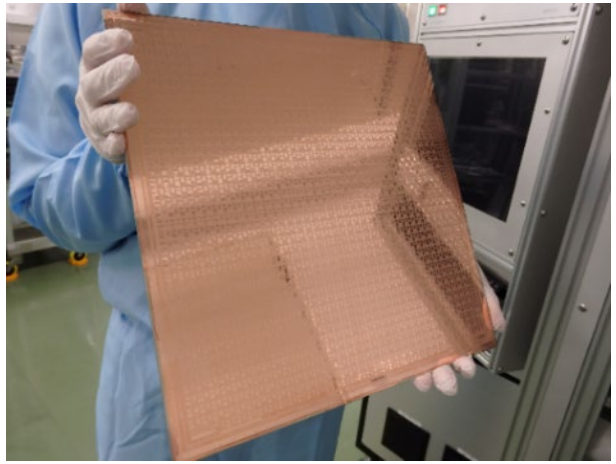
Introduction of Our Coreless Chip Embedded Technology

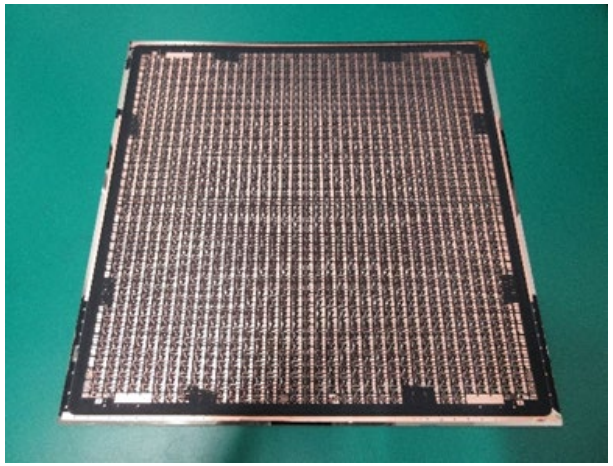
AOI's new approach of ***Ultra thinner, Higher heat dissipation*** chip embedded technology in analog and power solutions.





Features of this concept

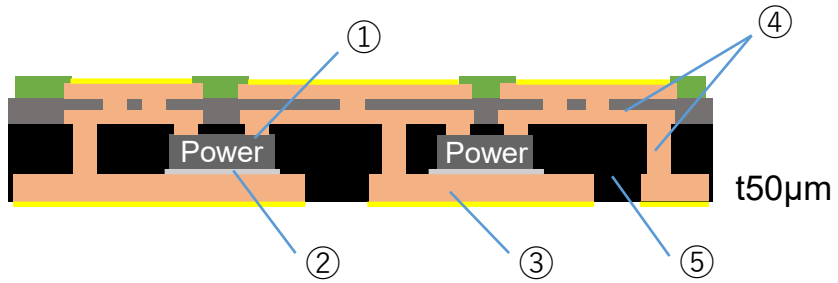
- Unique Coreless structure with all-Cu plating embedding method, using power customized fan-out processes
- Panel form of 300 mm square with cost benefit
- Smaller and Ultra thinner module package with coreless structure
- Excellent thermal property with large electrode pad and large via filling
- High reliability and short TAT with one stop solution (from panel substrates to package assembly in-house)



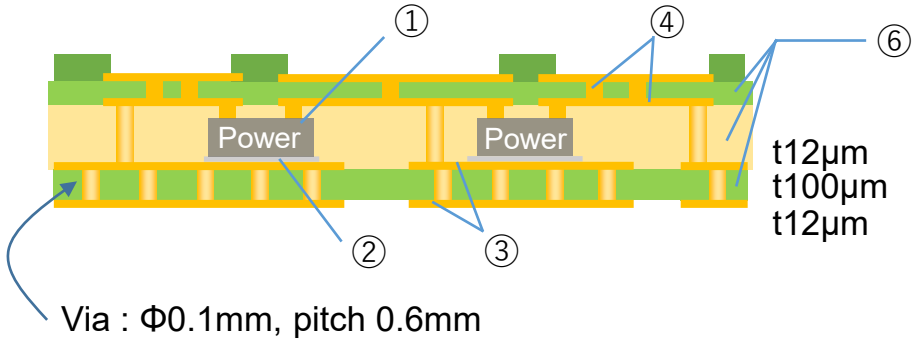
Thermal Resistance Simulation with Our Concept Package

■ Simulation conditions and structures

Our concept package



Conventional Prepreg package (assumption)



Analysis conditions

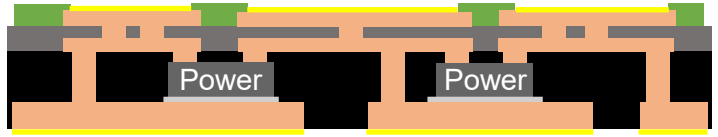
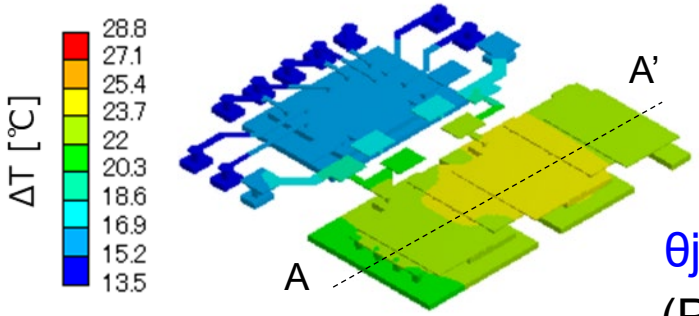
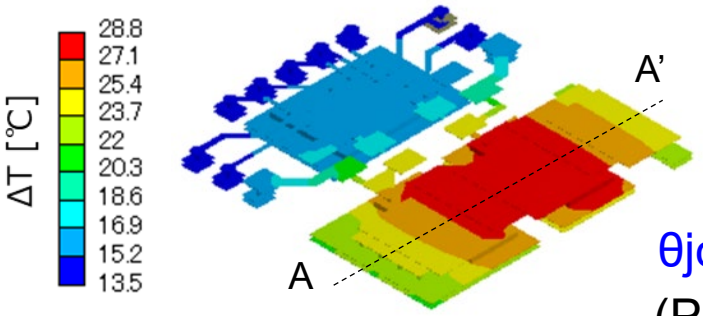
Analysis software	ANSYS
Analysis type	Steady heat transfer
Heat transfer coefficient	10W/(m²℃) assuming natural air cooling
Chip Power	Total 1.0W 0.5W/power chip

Material properties

Parts	Thermal conductivity [W/(m.℃)]
①Chip	124
②Ag sinter	100
③Electrode PAD	360
④RDL, VIA	360
⑤EMC	1.0
⑥Prepreg	0.7
⑦Solder resist	1.0

Thermal Resistance Simulation with Our Concept Package

■ Simulation result

	Our Concept package	Prepreg package (assumption)
Structure	 t50μm	 t12μm t100μm t12μm Via : φ0.1mm, pitch 0.6mm
Thermal simulation result	Inside the Package image  θjc : 0.5 [℃/W] (Package only) Cross-section A - A' 	Inside the Package image  θjc : 3.7 [℃/W] (Package only) Cross-section A - A' 

The thermal resistance of our concept package is very low, and it has the advantage of quickly dissipating heat to the substrate side.

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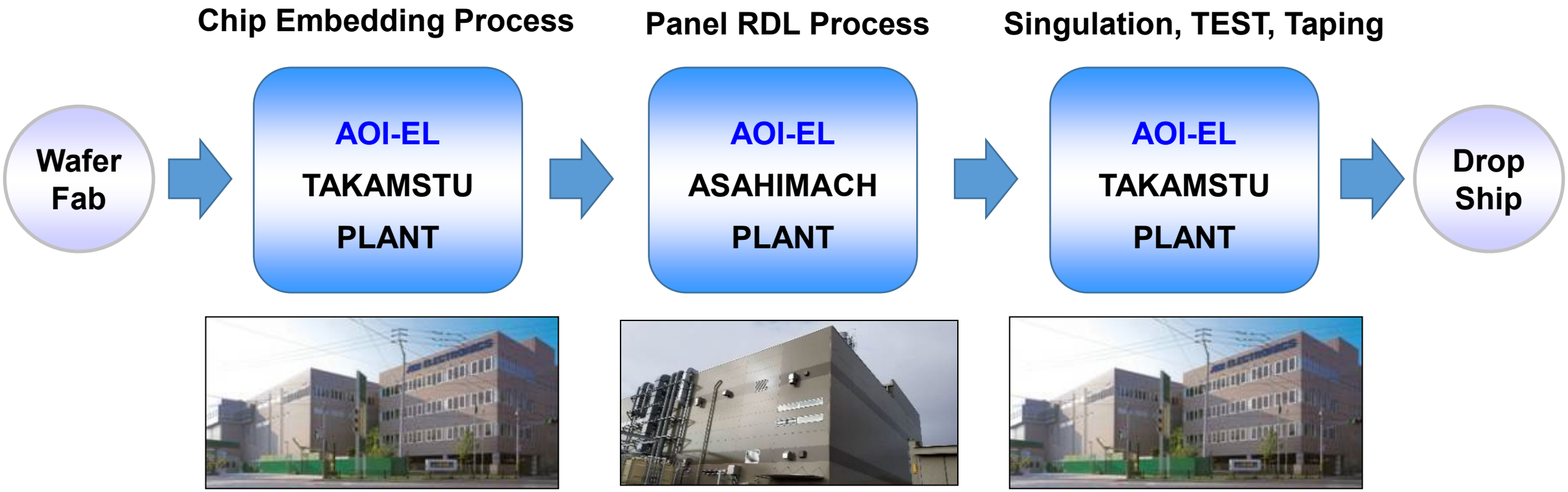
Trial production and evaluations for a Prototype

■ Panel level package manufacturing flow

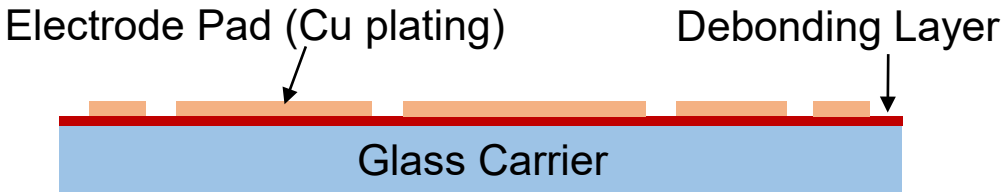


We can perform one-stop production in-house, from panel substrates to chip embedding process, panel RDL process and package assembly.

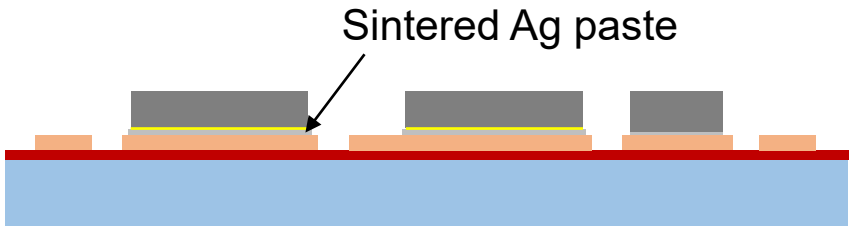
Trial production and evaluations for a Prototype

■ Process flow (1)

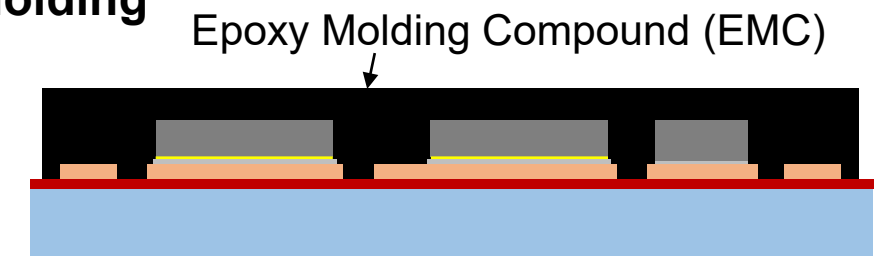
1. Electrode Pads Formation on Glass Carrier



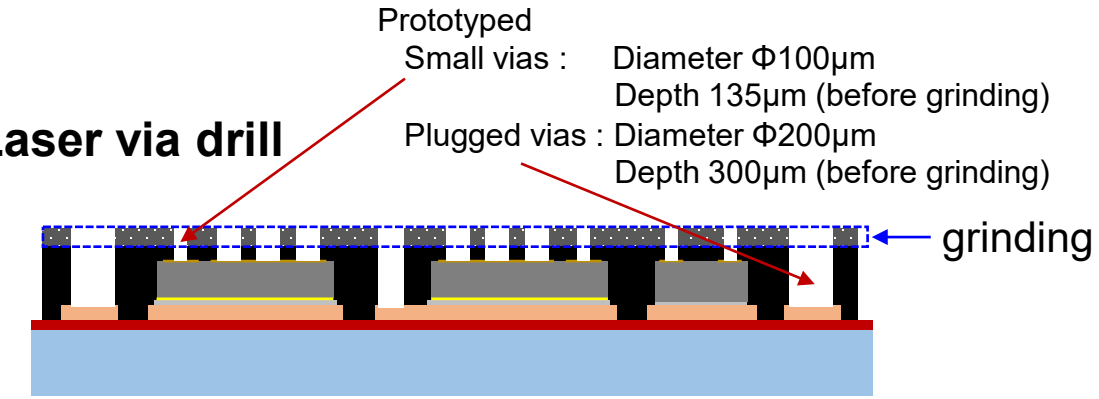
2. Controller and Power Chips Bonding



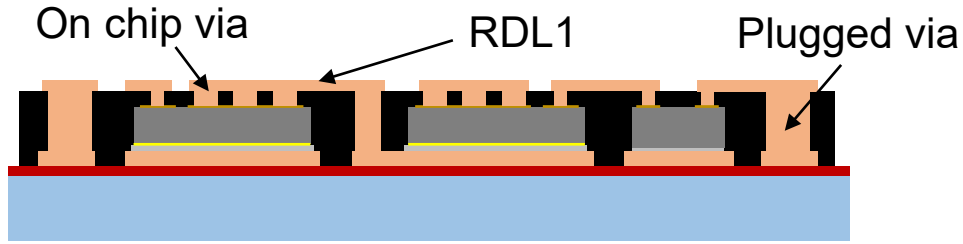
3. Molding



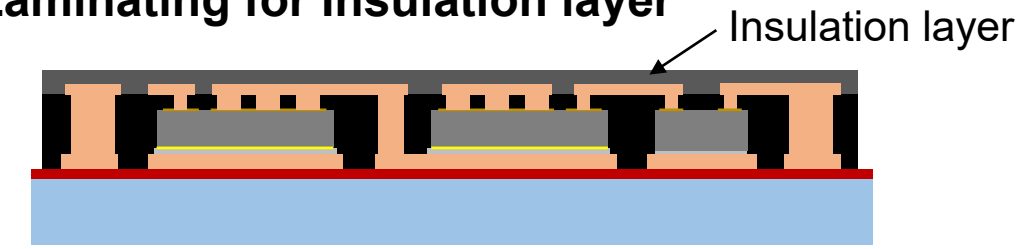
4. Laser via drill



5. Cu plating for Via-filling and RDL1



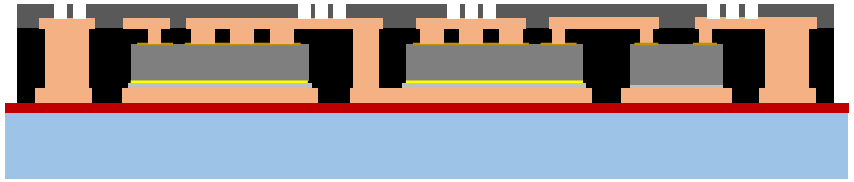
6. Laminating for Insulation layer



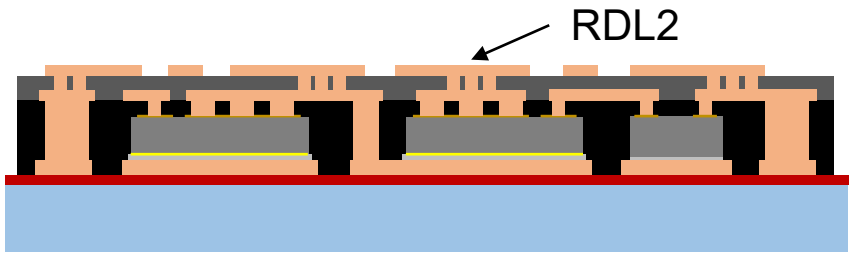
Trial production and evaluations for a Prototype

■ Process flow (2)

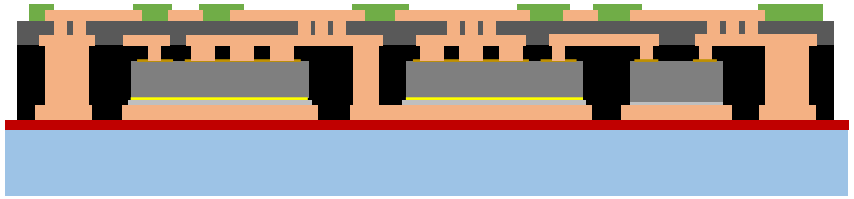
7. Laser via drill



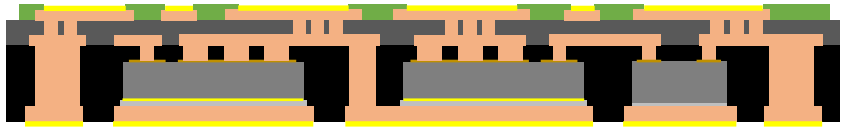
8. Cu plating for Via-filling and RDL2



9. Solder resist formation



10. Glass Carrier Debonding / Terminal plating / Singulation



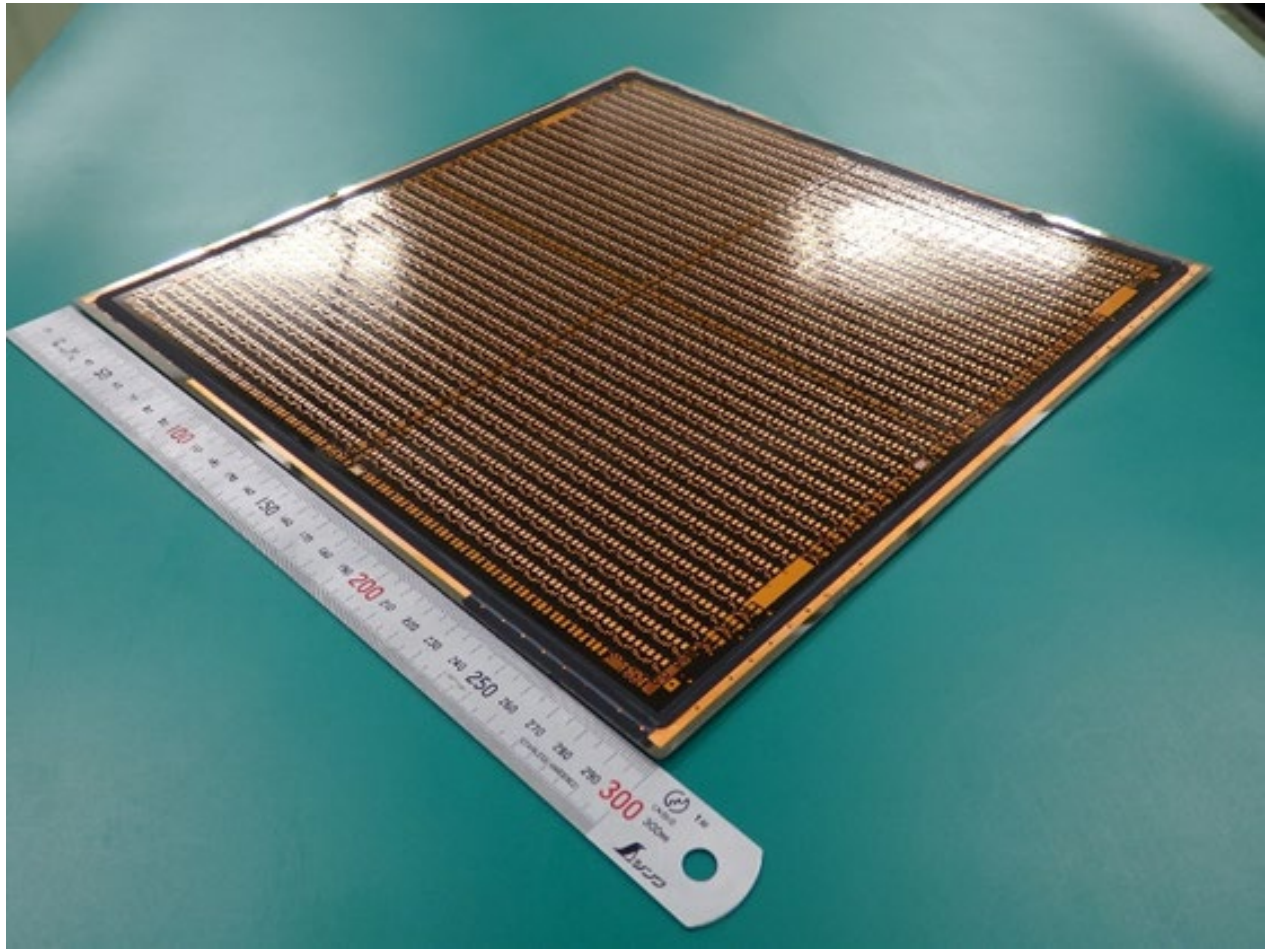
Our usual inspection or test

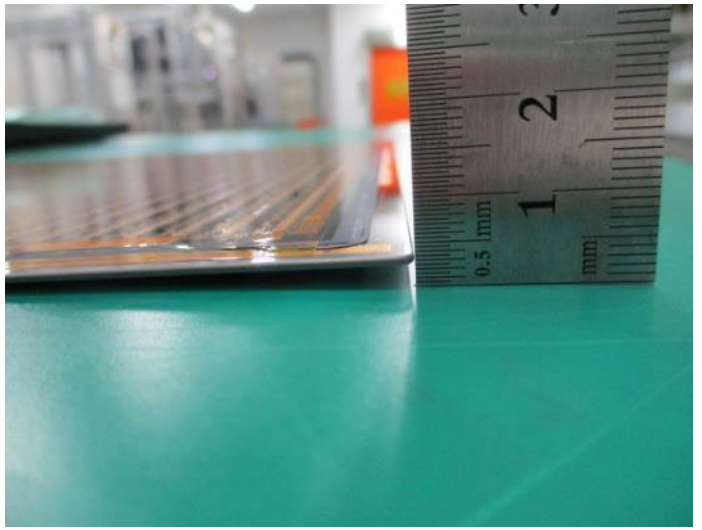
- Pattern inspection for each process
- Open/short test for checking internal connection
- Optional function test

Trial production and evaluations for a Prototype

- 300 mm square Panel-level photo

Warpage Before singulation (with Glass Carrier)





Panel warpage : 2mm Maximum

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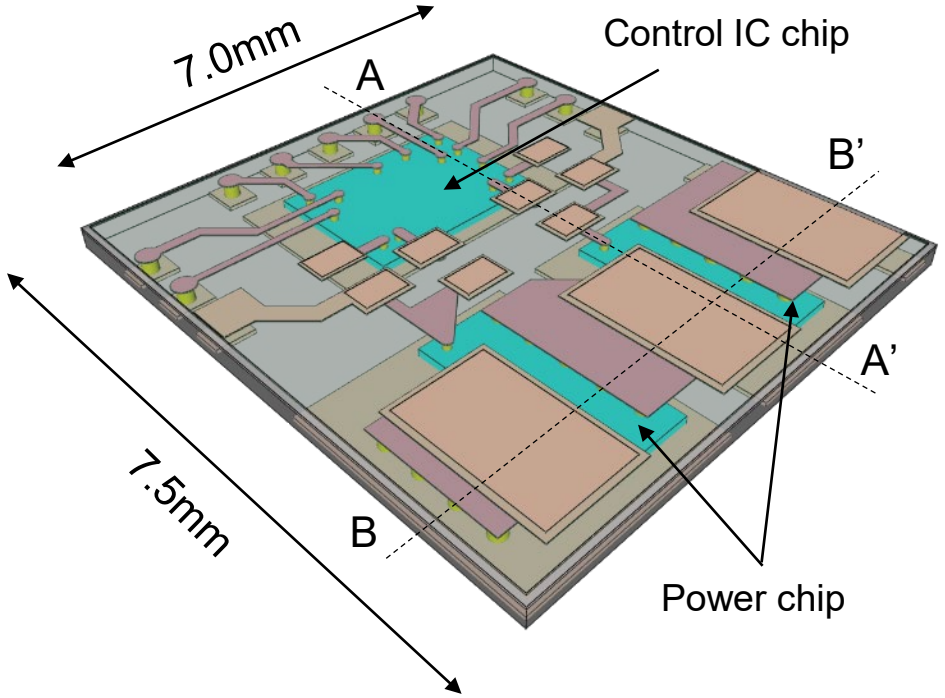
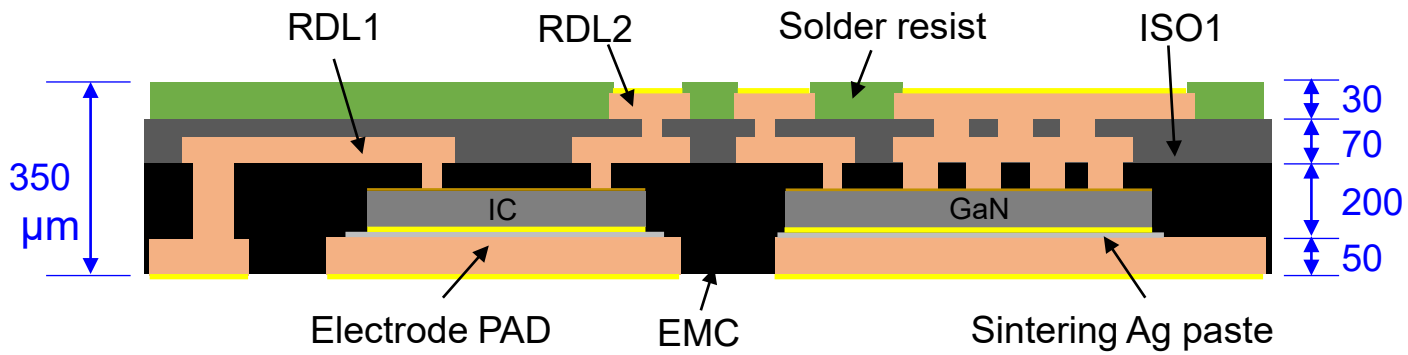
Trial production and evaluations for a Prototype

■ Prototype package structure

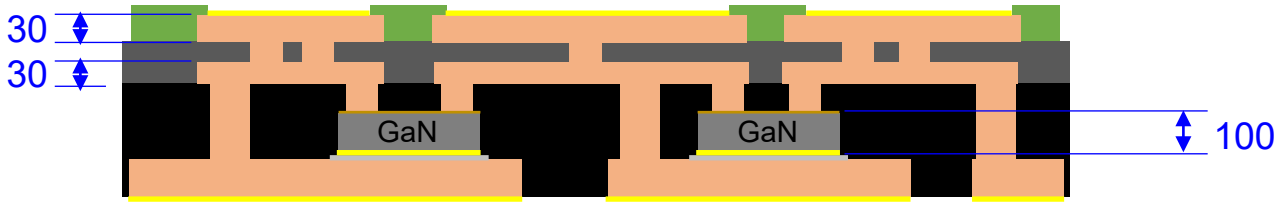
Design value /unit : μm



Control IC chip × 1, Power chip × 2



Cross-section A-A'



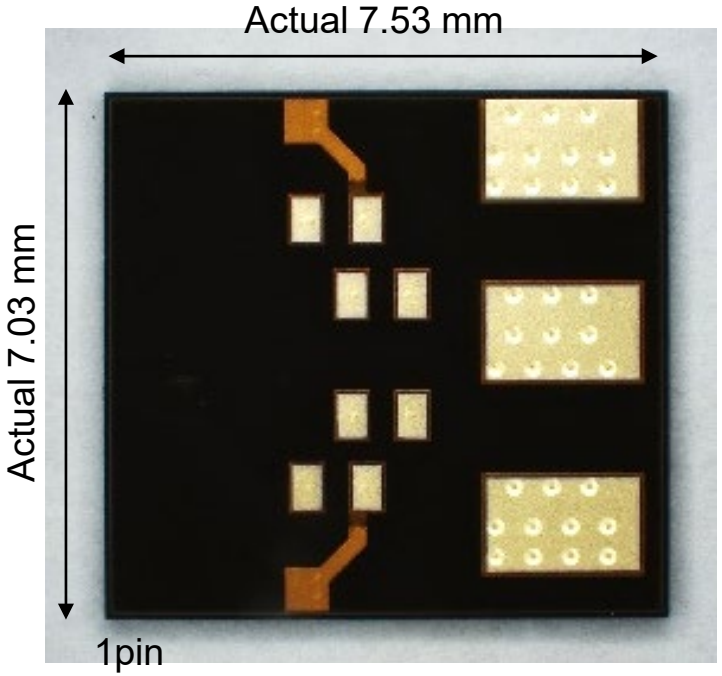
Cross-section B-B'

- Ultra-thin & high heat dissipation module with DC-DC half-bridge structure.
- Motif of GaN HEMT for power and high-speed switching.

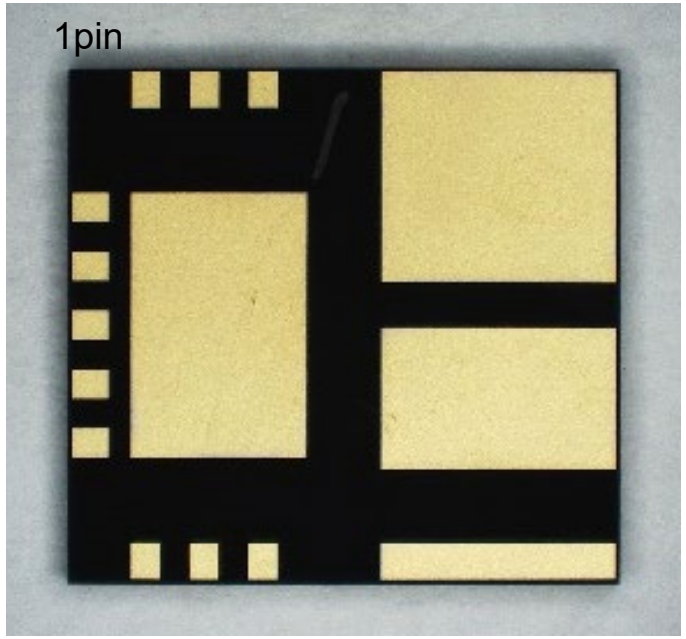
Trial production and evaluations for a Prototype

■ Prototyped package

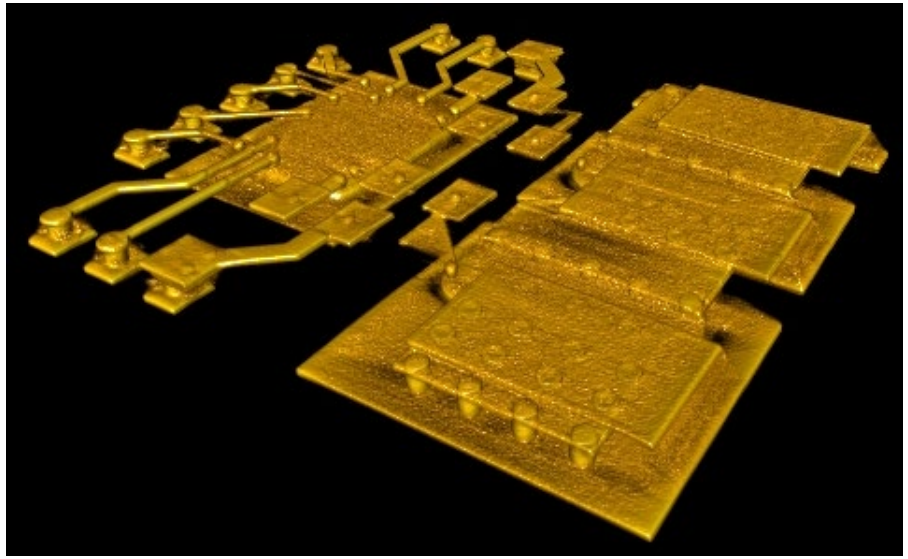
Top side



Bottom side
(Board mounting side)



X-ray CT 3D image
(Internal structure)



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Trial production and evaluations for a Prototype

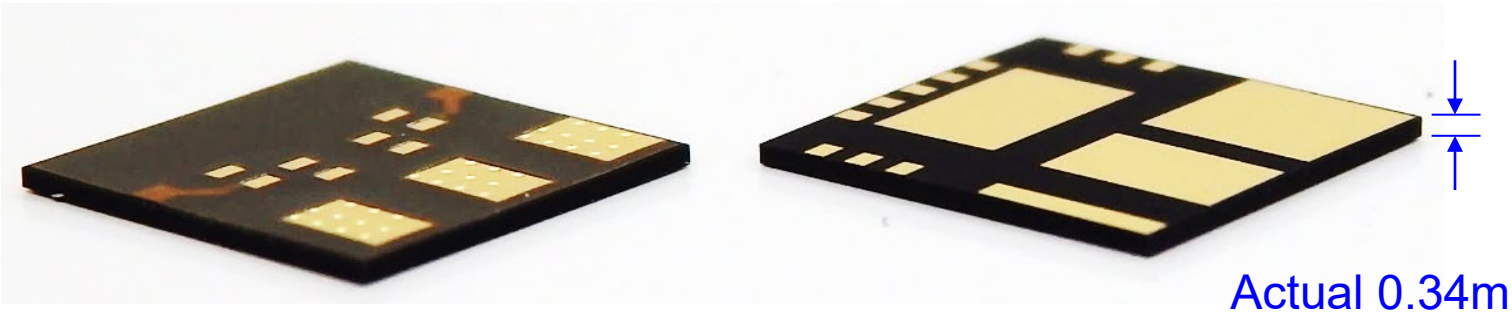
■ Prototyped package

Package thickness comparison

New Coreless chip embedded module package

Top side

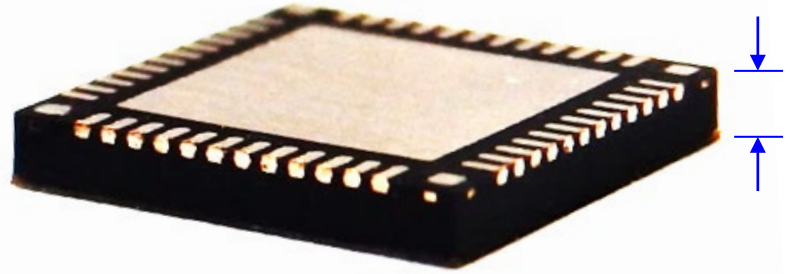
Bottom side



Actual 0.34mm

Package size : 7.0×7.5mm

Conventional Power QFN



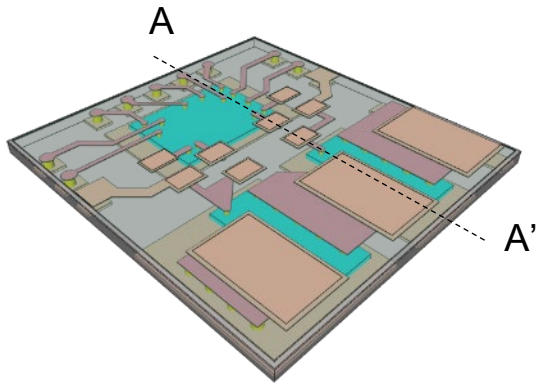
Actual 1.10mm

Package size : 8.0×8.0mm

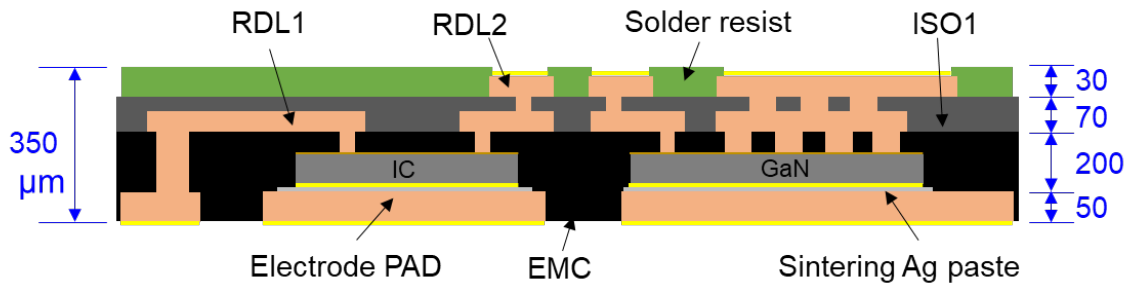
Our proposed new Coreless chip embedded package thickness is actual 0.34mm.
It is very thin compared to conventional power QFN.
Very thin SoC-like analog and power module package such as heterogeneous chip bonding can also be realized.

Trial production and evaluations for a Prototype

■ Prototyped package

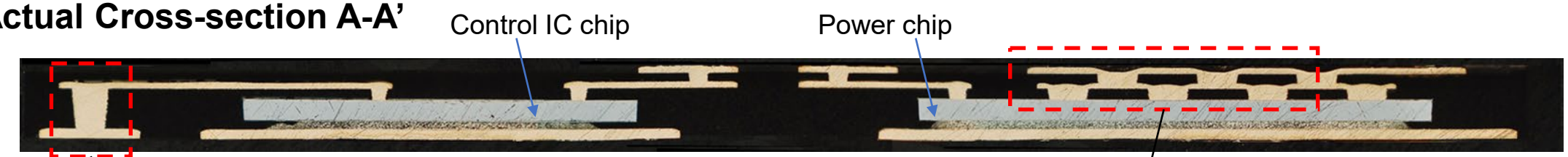


Cross-section SEM image

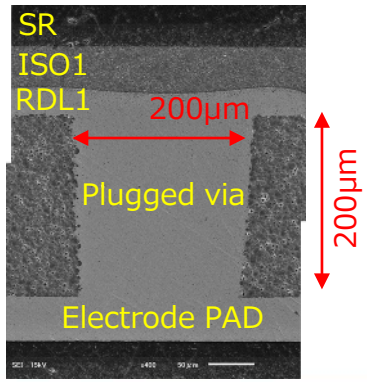


Cross-section A-A'

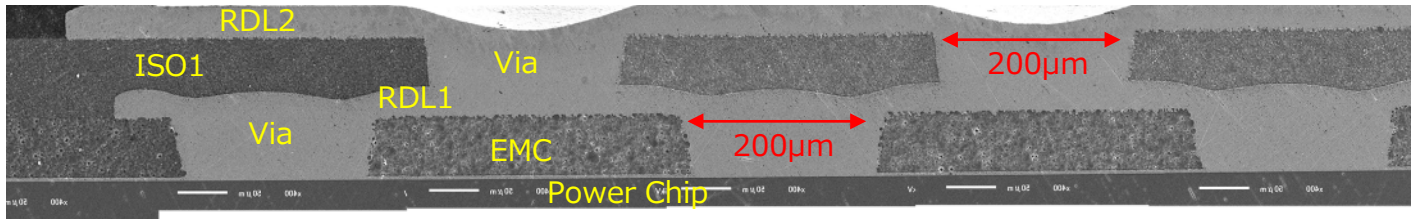
Actual Cross-section A-A'



Cu plugged via



Direct Cu plating connection of power chips



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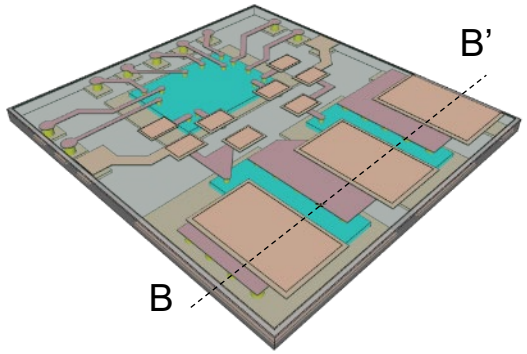
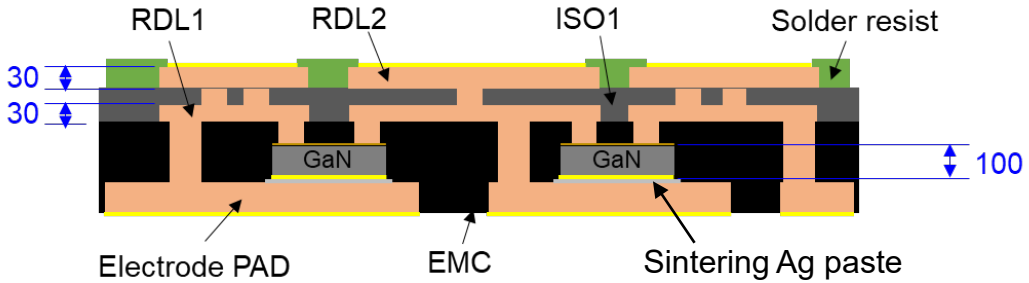
Trial production and evaluations for a Prototype

■ Prototyped package

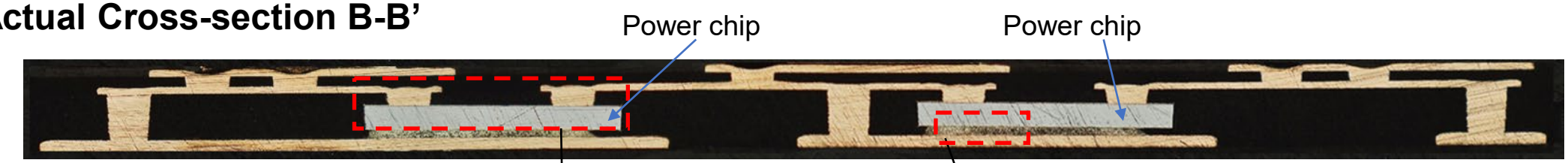


Cross-section SEM image

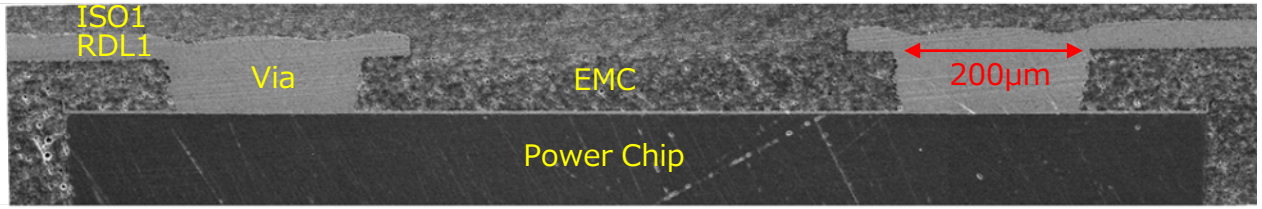


Cross-section B-B'

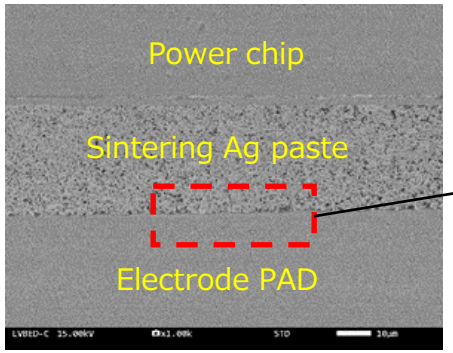
Actual Cross-section B-B'



Direct Cu plating connection of power chips

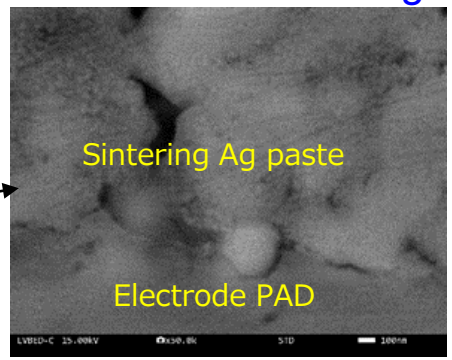


Chip attached paste



×1,000

Good Necking

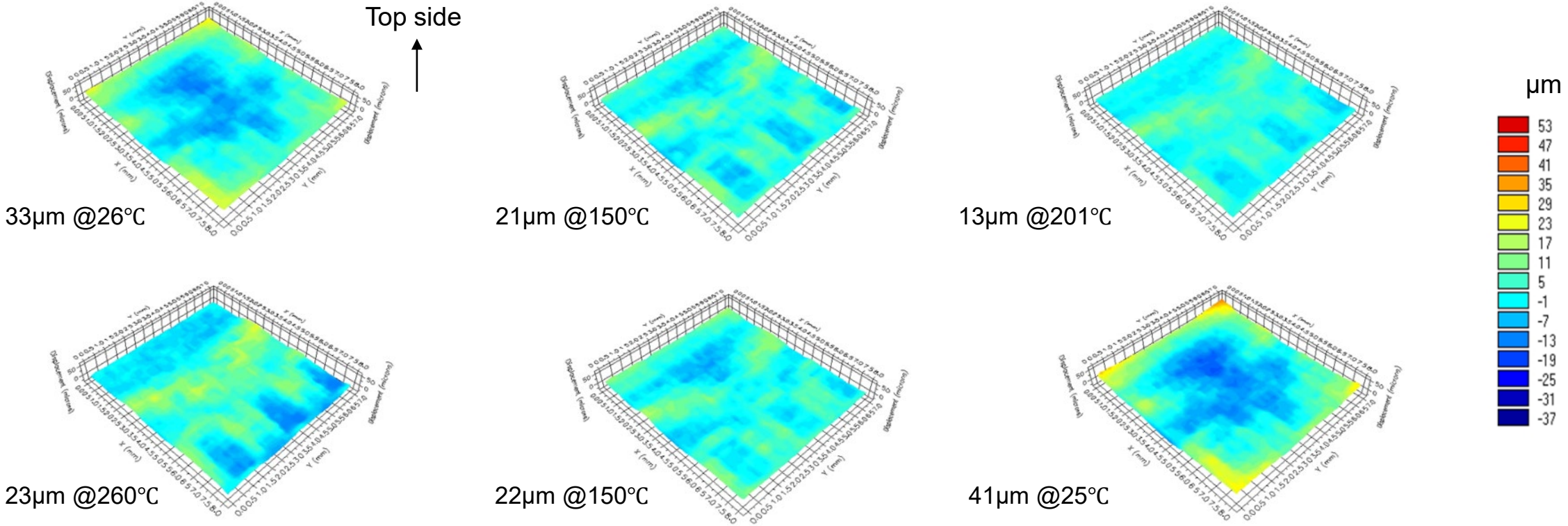


×50,000

Trial production and evaluations for a Prototype

■ Package warpage

Warpage Behavior in the Reflow Temperature Range using shadow moiré method (3D Plot)



At room temperature, warpage was maximized (less than 50μm) with smile shape.
At high reflow temperature, warpage became small, tended to be flat.

Trial production and evaluations for a Prototype

■ Reliability test

Test Items	Test Condition	Duration	Judgment	Status
Precondition	85℃, 60%RH, 168hr ⇒ >260℃, 30sec. 3X (JEDEC J-STD-020D MSL Level2)	-	SAT Open/shot test	Ongoing
HTHH	Precondition ⇒ 85℃ 85%RH	1,000hr	SAT SEM Cross-section Open/shot test	Ongoing
Unbiased HAST	Precondition ⇒ 121℃, 100%RH, 2atm	100hr	SAT SEM Cross-section Open/shot test	Ongoing
HTS	Precondition ⇒ 150℃	1,000hr	SAT SEM Cross-section Open/shot test	Ongoing
TC	Precondition ⇒ -65℃～150℃	500cycle	SAT SEM Cross-section Open/shot test	Ongoing

There is no initial failure at Unbiased HAST 48hr, TC 100cycle (SAT, Open/shot test).

- Background
- Introduction of Our Coreless Chip Embedded Technology
- Trial production and evaluations for a Prototype
  - Manufacturing flow
  - Process flow
  - Package structure
  - Prototyped package
  - Package warpage
- **Summary**

Summary

- ✓ We have demonstrated a very thin thickness of 350μm and higher heat dissipation new advanced chip-embedded power module package with 300mm square panel-level process.

- ✓ This proposed new package is very suitable for high power delivery solutions, especially for complex power delivery structures such as multi-core processors, FPGAs and so on, with thinness and being placed in close proximity to each point of load.

- ✓ Very thin SoC-like analog and power module package such as heterogeneous chip bonding can also be realized.

Thank you for your attention.

Our presentation will also be in Poster Session.
Please join and discuss!