ADVANCED IC SUBSTRATES FOR HETEROGENEOUS INTEGRATION

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PRESENTATION OUTLINE

- Industry Trends
- IC Substrates Drivers
- AT&S Solutions
- Summary

DIGITALIZATION EVERYWHERE

Data driven society

THE RISE OF THE DATA ERA

Global Data Volume:

- 2020: 59 Zetabyte
- 2025: 175 Zetabyte

→ (24% CAGR)

Autonomous Driving

Cameras, Lidar, Radar

Genomics

High performance computing for human genome sequencing

Climate Research

Data generation and analytics

Vision Processor

Augmented reality applications

Source: IDC (2019, 2020)

DATA GROWTH DRIVES COMPUTE, STORAGE, CONNECTIVITY & NETWORKING DEMAND

- Technology changes
- Increased packaging solutions at system level
- There is NO standard technology which serves all application or customer needs and architecture.
- New module & system in packages driven by multiple new disruptive technologies

“We are at the tip of an iceberg where we can go with packaging”

Babak Sabi – Intel
Corporate **VP Assembly and Test Technology Development Intel**

Data storage

Server farms / data centers (e.g. server substrates)

- Solutions for increasing data speed (50gbit/second+)
- Reduced power consumption
- High level of integration and miniaturization

Data generation

Sensors (e.g. mainboard, substrates for edge- & cloud computing)

- Ever-smaller L/S through innovative production processes (mSAP)
- Miniaturization and increased functionalities
- 140 GHz solutions for next generation radar applications

Data transfer

Antennas (e.g. antenna modules, RF-modules, 5G communication, Car2Car, V2X)

- High end technologies for best in class signal integrity
- Low latency
- Higher bandwidth with new technical concepts

Data processing & analytics

Devices (e.g. mainboard, substrates for edge- & cloud computing)

- Ever-smaller form factors
- Integration of advanced active and passive RF components
- High end technologies for best in class signal integrity

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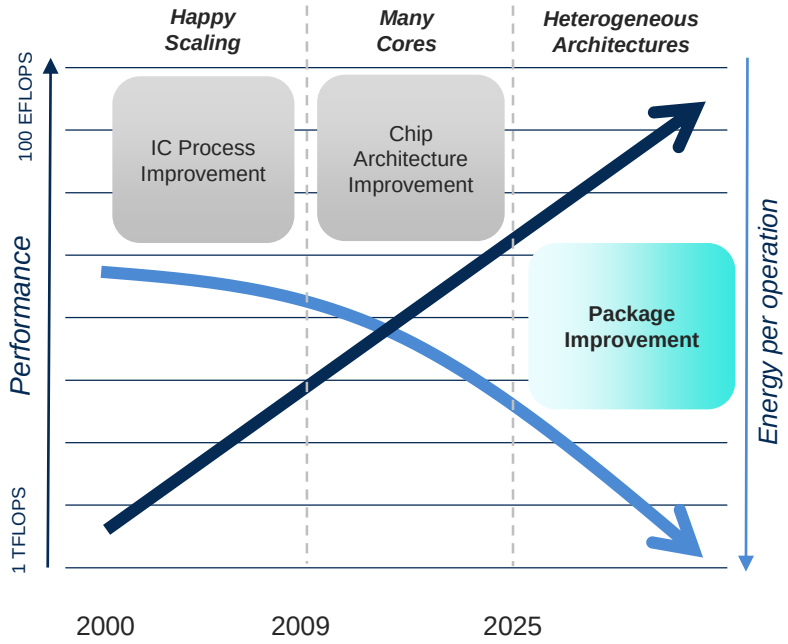
FUTURE TREND FOR ADVANCED COMPUTING

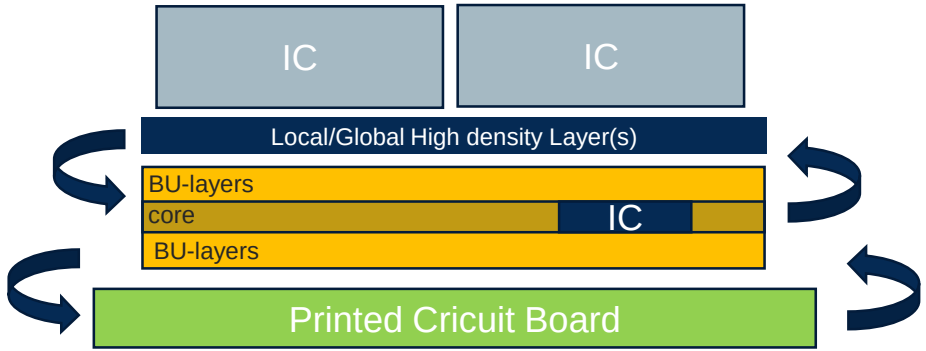
Node scaling alone does not provide desired performance



Advanced Substrates & Packaging

New Challenging Functions in Packaging

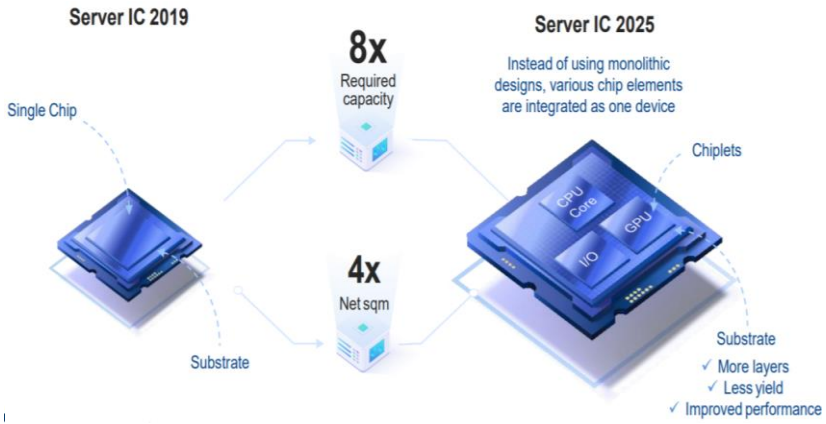
- Larger Body Sizes (Chiplets, HIR)
- CTE Mismatch (Chiplets, Interposer)
- D2D Connection (BW, low latency)
- Power Delivery (Power Mgmt./conversion)
- Thermal Dissipation (Efficient Cooling)



Which functions can/should be optimized where in the Package?

ABF SUBSTRATES DRIVERS

FCBGA Development trends



Drivers	Requirement trends
Heterogeneous integration	Large body/package size (up to 100x100)
High I/o COUNT	High layer count >20L
High-density interconnect	L/S 9/12µm
Bump pitch	90µm and below
Increase bandwidth	High-speed transmission
Increase assembly yield	Low warpage
More functionalities	Thermal management

What else can be done with IC Substrates?

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AT&S PRODUCT PORTFOLIO

Wide range of products for interconnection solutions

IC Substrates
Allow complex integrated circuits to be connected to PCBs while saving space. Also known as flip-chip technology.

High Density Interconnect PCBs
More compact PCBs thanks to a multi-layer structure can connect components with shorter and faster signal paths.

Embedded Component Packaging
A wide variety of micro-electronic components can be integrated directly into the IC substrates/PCBs.

Multilayer PCBs
Consist of several layers, are space-saving and ensure fast connections between components.

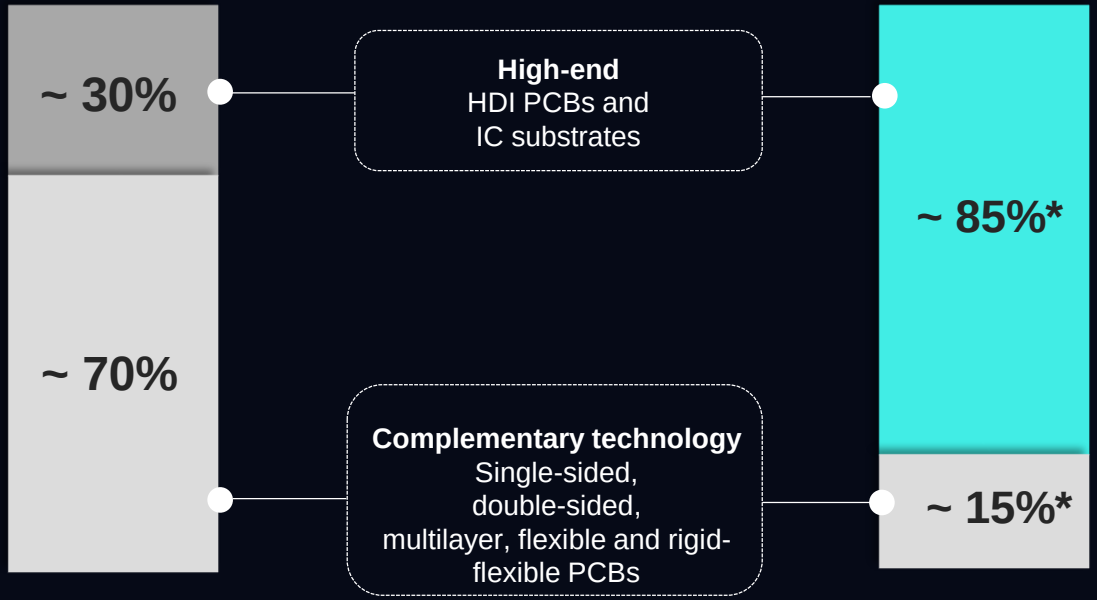
Modules
Modules fulfill a specific electrical function within a system. Miniaturized modules help to reduce overall system size.

Thermal Enhanced PCBs
Inlay PCBs, provided with copper coin inlays which allow heat to be dissipated selectively and to prevent overheating.

High Frequency & High Speed PCBs
Future 5G cellular networks and radar stations will work with high signal frequencies (mmWave), requiring new PCB solutions.

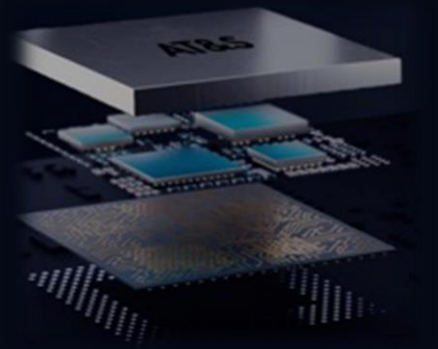
Flexible & Rigid Flexible PCBs
Can be installed twisted, folded or bent. This allows designs that get by without cables and plug connections.

STRATEGIC FOCUS ON HIGH-END TECHNOLOGIES



General PCB and IC substrates market

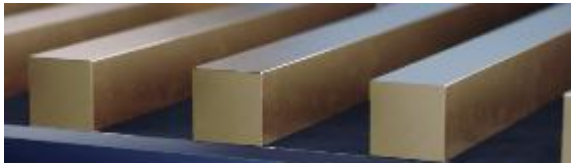
AT&S revenue



*for FY 2020/21; Source: ACT, AT&S

R&D PROGRAMS FOCUSING ON THE MAJOR TRENDS

Innovation focused on major trends and industry needs



Miniaturization

Increased computing power for fast data processing

Modularization

More functionality at same or reduced space

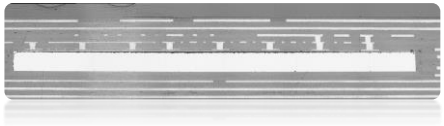
Increased speed / Low latency

Communication of high data volumes (5G, Autonomous Driving)

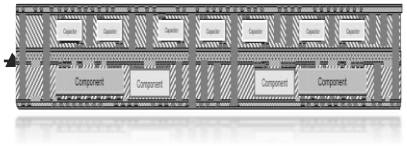
Increased power / Power efficiency

Reducing non-value adding electrical loss

ADVANCED PACKAGING CONCEPTS ON LARGE PANELS



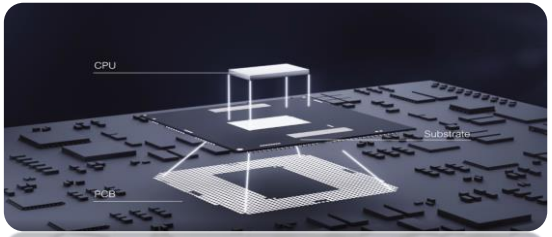
ECP® - 256 Id ePMIC IC embedded pkg



Cavities
THK reduction

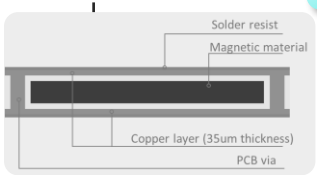
ECP
Passive/Active embedding

Multilayer PCB
Multi Functional Core



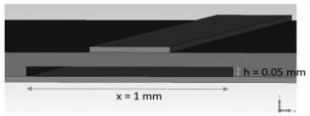
IC Substrate

Magnetics
Inductors/Shielding



Embedded Magnetic Material

SIW
Substrate Integrated Waveguides



75µm Dielectric Material
50µm Air Gap

MINIATURIZATION & MODULARIZATION

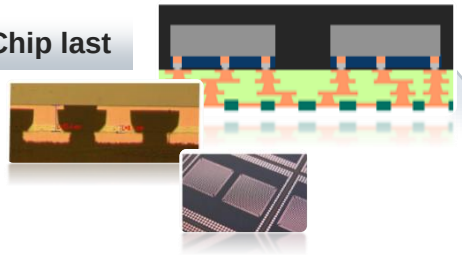
Novel Packaging Concepts

Chip first

Package Parameters

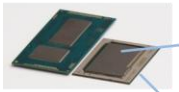
- Package Size: 15x15mm
- 2 components / PKG
- Component Size: 6x6mm
- Component I/O: 1089
- Component Pad: 83µm
- Laser via: 30µm
- Line/ Space: 9/12µm

Chip last

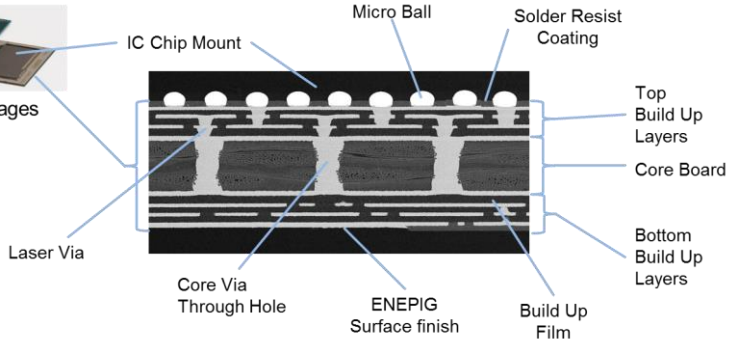


IC Substrate

Carries the IC chips and transmsitts the signals from the IC chips to the PCB

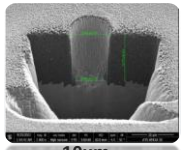


IC Packages



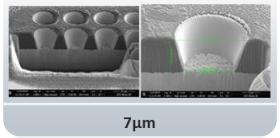
Small Via and High Density Routing

Laser



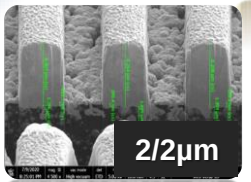
10µm

PID



7µm

5/5µm



2/2µm

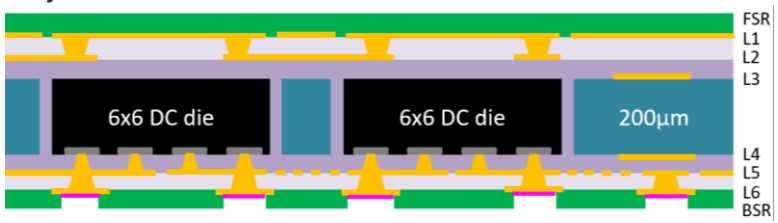
EMBEDDING OF COMPONENTS

Reliability test TV : MRT 10x, TCT 750cycle and uHAST 100hr → *No blister/delamination, R shift < 6%*

General package information:

- 6 Layer
- L/S: 9/12µm
- Via: 30µm
- Core thickness: 200µm
- 2 dies embedded

Symmetric BU : n-2-n structure with ECP®



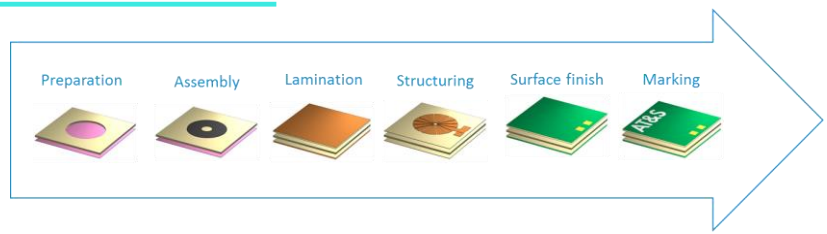
MSL3(Pre-condition), MRT 10X, TCT 750 cycles & uHAST test results : *Passed*

Test item	Standard	Failure mode	Pre-conditioning	Rel. Conditions
Multi Reflow	IPC/JEDEC J-STD-020D.1	Visual check Cross section analysis E-test	125℃ 24hrs, 60℃/60%RH for 40hrs, 3x Reflow(260℃ peak)	Reflow peak max 260℃, 10x (10 reflow cycles)
TCT	IPC TM650 2.6.2.7	Visual check Cross section analysis E-test		-55℃/+125℃, 750cycle (Readout at 250/500/750)
uHAST	JEDEC JESD22-A110E	Visual check Cross section analysis E-test		130℃/85%RH, 100hr (Readout at 50/100)

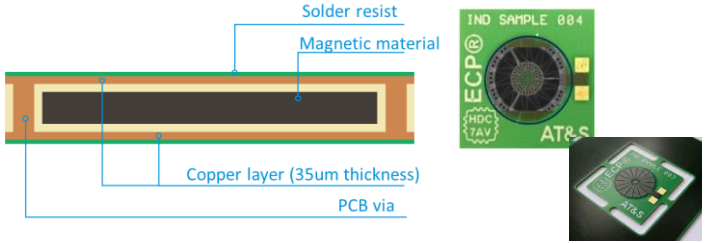
Source: AT&S AG

EMBEDDING OF MAGNETIC MATERIALS

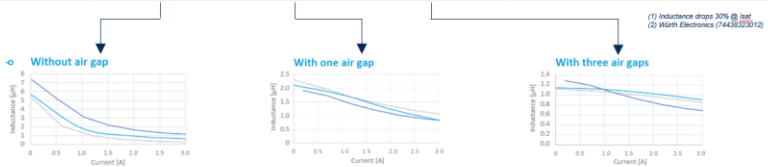
- Qualified process based on the ECP® technology
- Independent from layer count
- Can be applied to PCBs and Cores of ICS



Inductor	Value	Unit
Cu THK	35	µm
Magnetic Material THK	0.3	mm
Inner/outer diameter	3/10.5	mm
Windings	16	turns
Total thickness	0.5	mm
Inductance	5.7-1.15	µH
Saturation Current	0.3-3.6	A



Parameter	Symbol	Without air gap	With 1 air gap	With 3 air gaps	Standard SMD (2)	Benchmark
Inductance	L (@ 1 MHz)	5.7 µH	2.2 µH	1.15 µH	1.2 µH	Equal
Saturation current	I_{sat} (1)	300 mA	1.5 A	3.6 A	3.8 A	Equal
Rated current (DC)	I_R (@ ΔT = 40 K)		2.0 A		1.9 A	Equal
DC Resistance	R_{DC} (@ 0.1 A)		79 mΩ		82 mΩ	Equal
Self-resonance fr.	f_{res}	30 MHz	40 MHz	80 MHz	75 MHz	Equal
Package size	D_I/D_O		3/10.5 mm		2.5 x 2 mm	↘
Air gap length	l_g	-	500 µm	3 x 170 µm	-	
Total thickness	h		500 µm		1 mm	↑



Source: AT&S AG

CONCETS FOR LOSS REDUCTION

Solutions to improve Signal Integrity Performance

Loss factor Base Material (Dielectric Losses)

- Suitable Materials

Length of Traces (Conductor Losses)

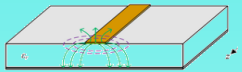
- Miniaturization (L/S)

Skin Effect (Ohmic load)

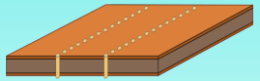
- Low Copper Foil Treatment (low / no profile)
- Smooth Traces (Adhesion Promoter)
- Suitable End Surface Platings (Ni less …)

+

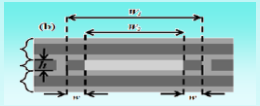
Micro Strip line



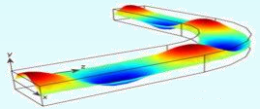
Substrate Integrate Waveguide



Air filled Waveguide



Waveguide

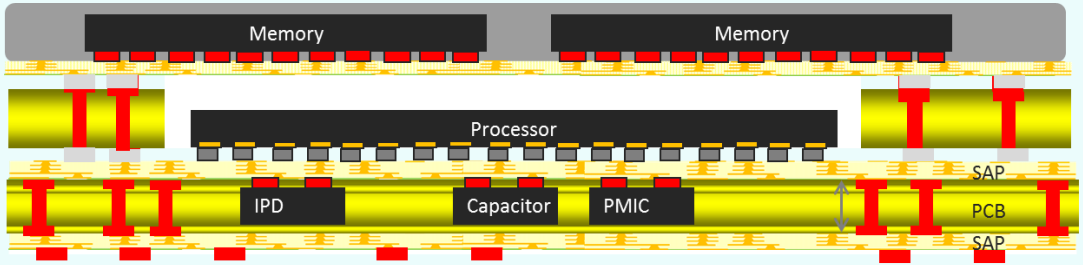


COMBINATION OF DIFFERENT CONCEPTS

Chip First + Chip last + AirGap

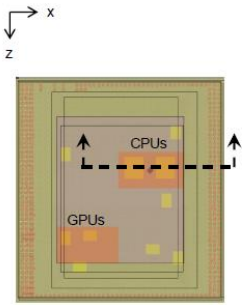
Computing/Processing Module with:

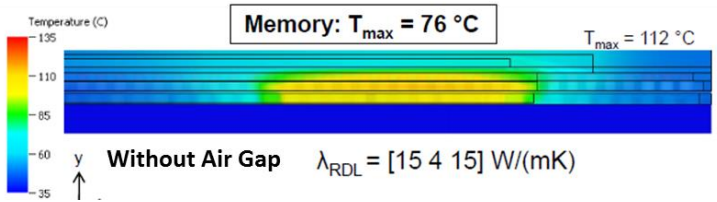
- Integrated power supply
- Solution to connect processor and memory in a PoP structure (if needed)
- Integrated signal stabilization
- Potential for additional functionality (communication, anti-fraud, etc.)
- Improved Thermal Management

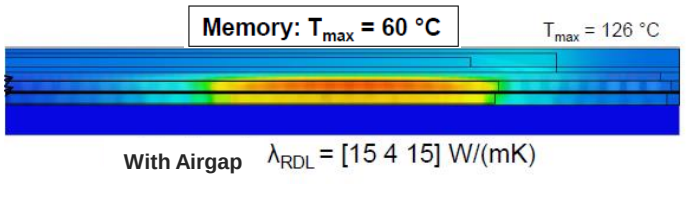


Patent Pending

Thermal Simulation







Conditions in package improved due to air gap

- Temperature of memory decreases (76°C to 60°C)
- Temperature of Processor increases (112°C to 126°C) → can be decreased with tool box

Source: AT&S AG

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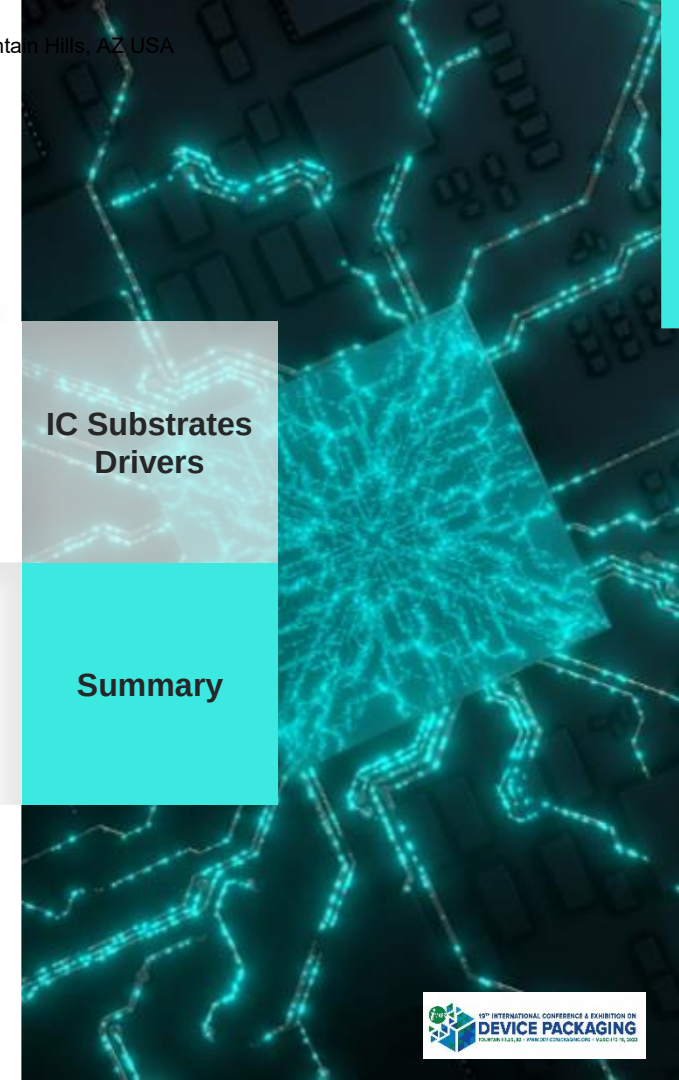

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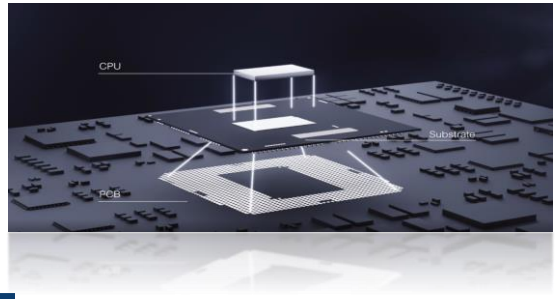
SUMMARY & CONCLUSION

New Interconnect Requirements drive Advance Packaging Solutions

- Increased packaging solutions at system level integration are required
- Miniaturization of electronic systems drives the need for larger, multi-functional modules
- The IC Substrate is a major building block in nearly all advanced system architectures

PCB/IC Substrate Technologies offer a versatile Tool Box

- Fan-Out capabilities for fine pitch components enable chip first and chip last integration
- Magnetic materials can be embedded for various functions (Inductor, shielding, etc.)
- New concepts offer improved Signal Integrity
- Advanced Cooling concepts use Copper plated vias, cavity walls and inlays



THANK YOU!

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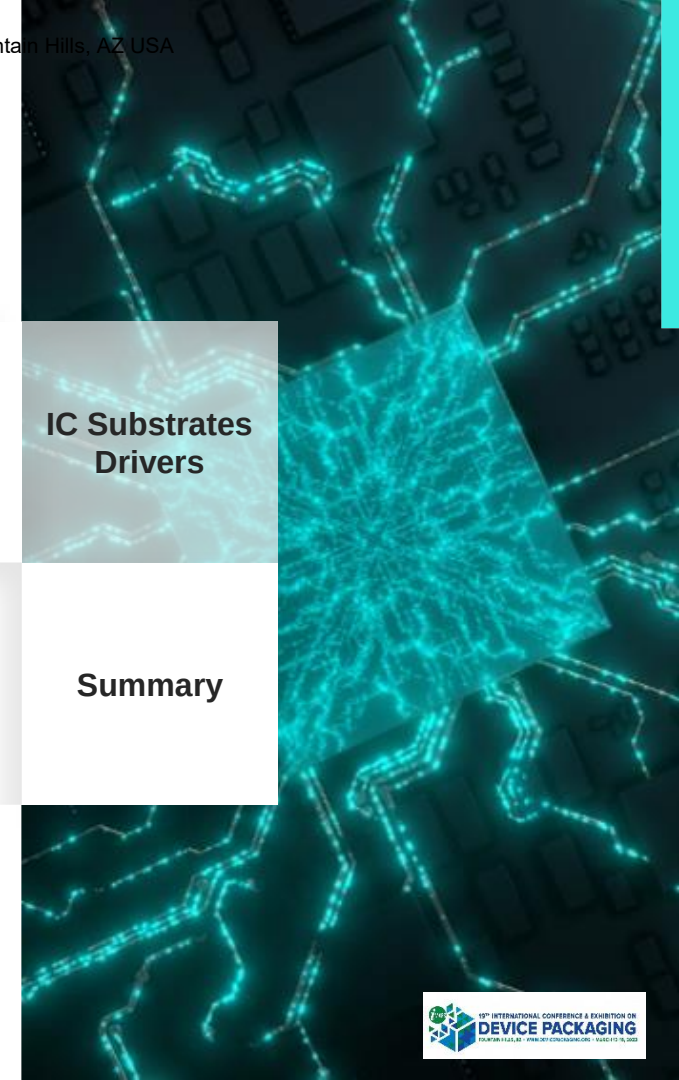

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