Thermo-compression Bonding Assembly Technology

IMAPs March 2023

Kulicke & Soffa®

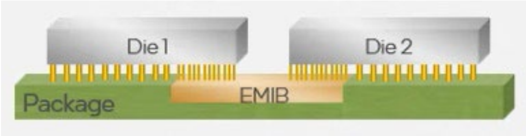
Agenda

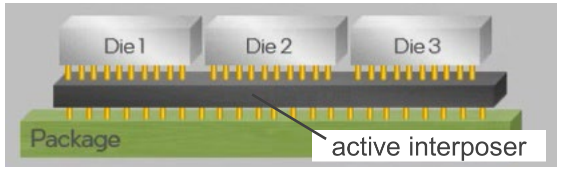
- Packaging Technology Roadmap
- Fluxless TCB
- Compare TCB to Hybrid Bonding
  - Process steps
  - Cost Model
- Cu to Cu TCB

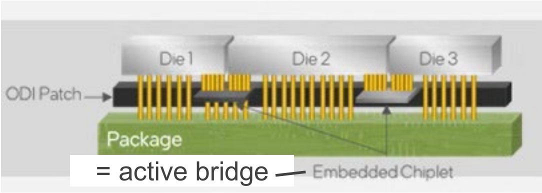
Introduction

- **Moore's Law** has driven performance for the SEMI industry for decades.
  However, in recent years, Moore's law has ground to a halt:
  - Rising wafer manufacturing cost & increased chip design complexity outweigh the benefits of die shrinks
  - This results in lower pace of new Si nodes with fewer and fewer state-of-the art fab's being constructed
- **Where does increased performance come from**
  - The answer is packaging technology
  - Increasing 2D and 3D I/O and chip packaging density through Heterogeneous Integration
- **Heterogeneous 2.5D/3D re-integration of dissimilar chips ("More than Moore"):**
  - Combining different functions, from different wafers, with different feature sizes…
- **Heterogeneous Integration** requires high bandwidth and low power communication between chiplets,
  - This drives an aggressive roadmap for Advanced Packaging technologies and fine-pitch interconnects

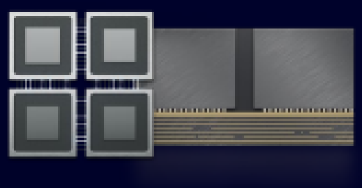
Example Interconnect Pitch Scaling – Intel AP Roadmap







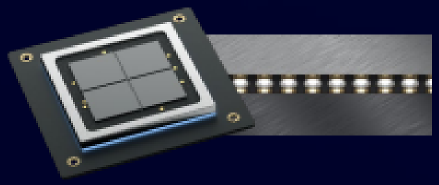
Embedded Multi-die Interconnect (EMIB)



bump pitch **50-40 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

Foveros Omni

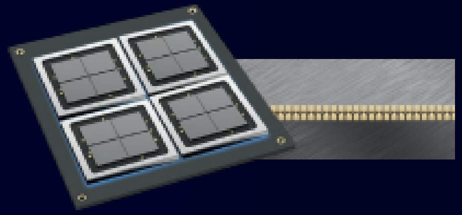
(ODI – Omni Directional Interconnect)

@ launch; Roadmap ~10um

bump pitch **~25 microns**

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

Foveros Direct

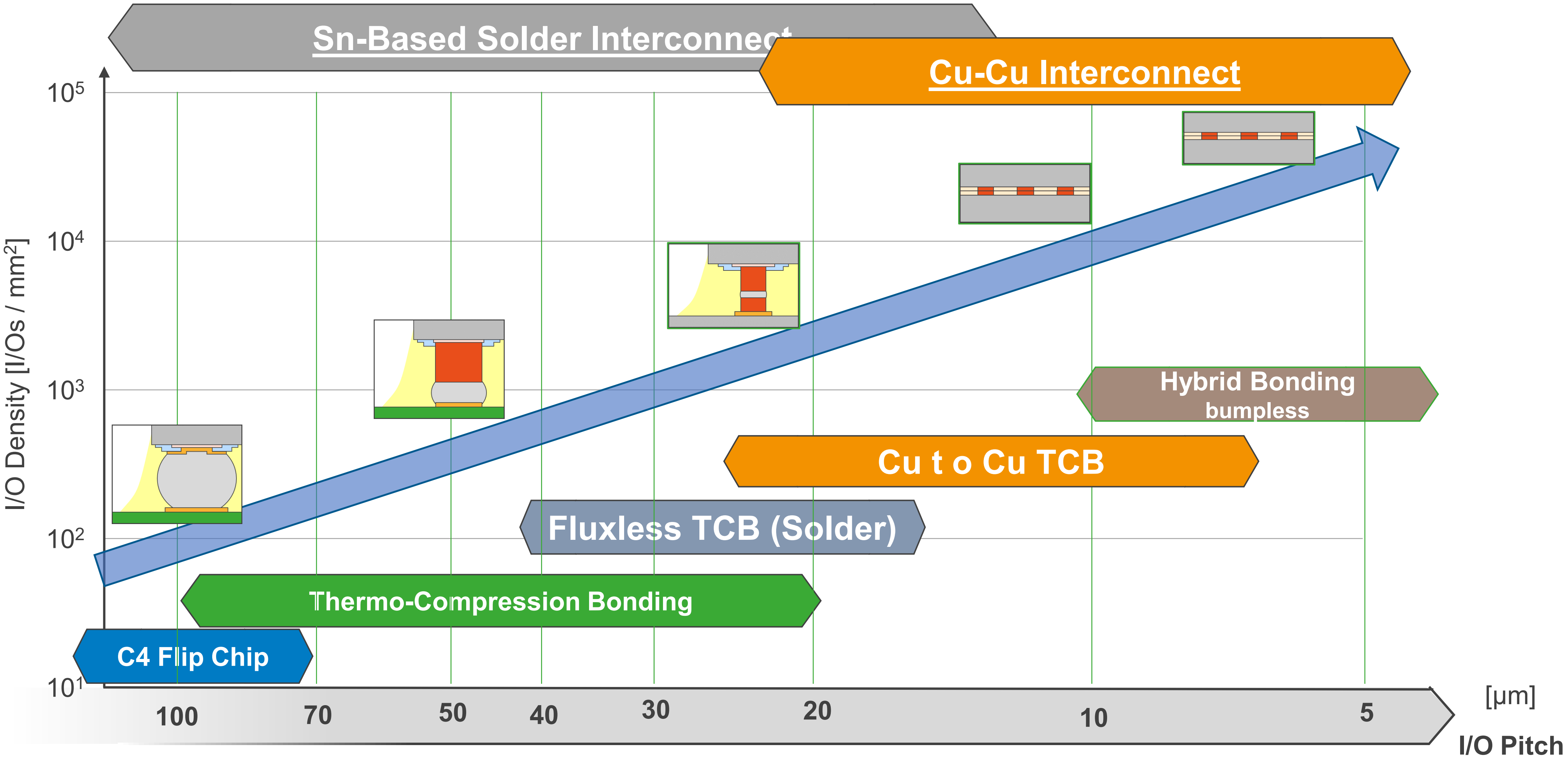


bump pitch **< 10 microns**

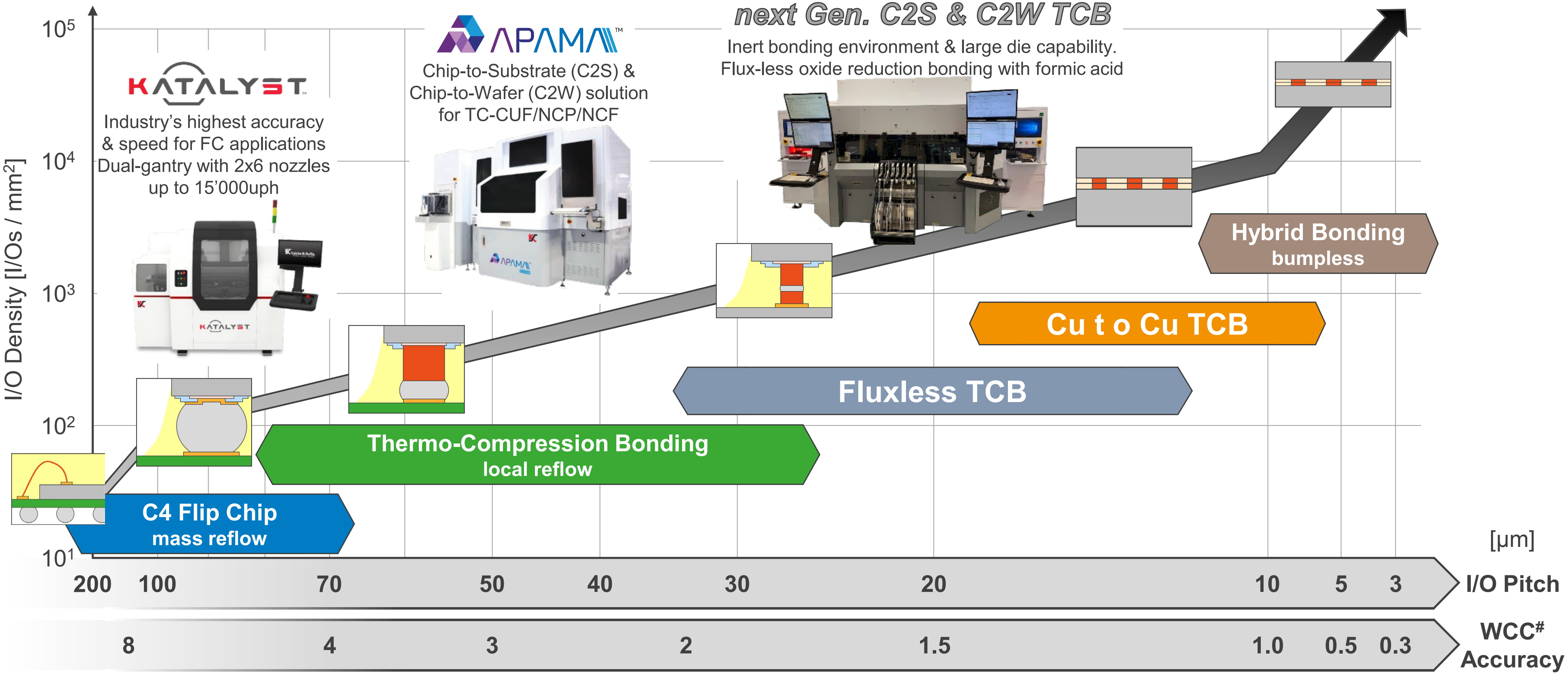
- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

Source: Electronic Design Magazine

Interconnect Roadmap for Advanced Packages



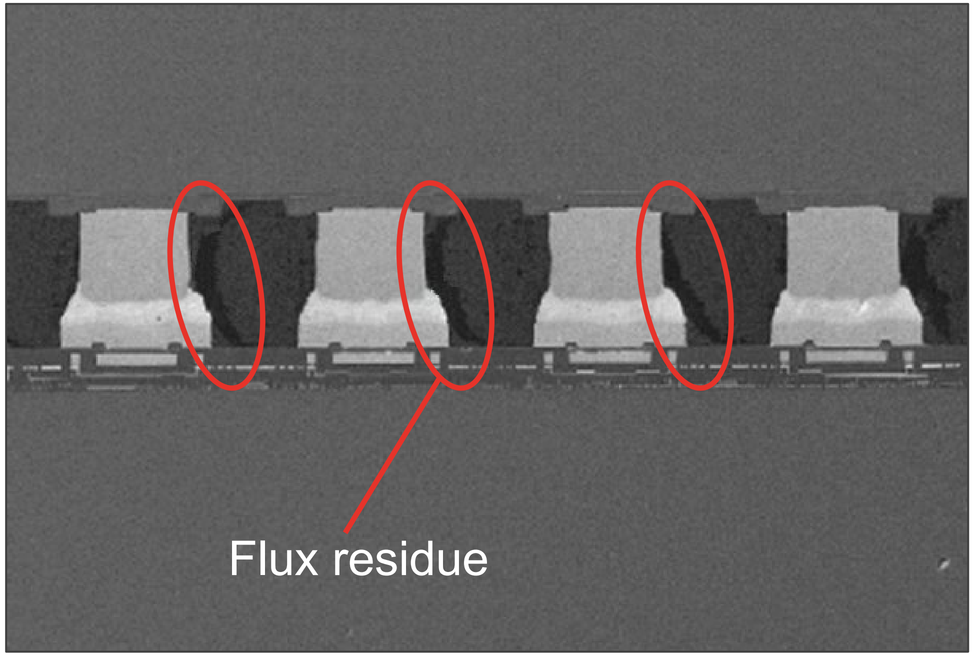
Interconnect Pitch Scaling for Heterogeneous Integration



#Refers to the Upper Control Limit for **W**orst **C**ase **C**orner $Cpk_{WCC} > 1$. Includes repeatability and mean offset!

Challenges with Flux Based TCB Process

- Fluxing adds TCB process complexity
- Pre-bonding fluxing step is required:
  - Flux pre-applied to the substrate has a limited activation time and imposes limits on maximum substrate temperature
  - Dipping large die in flux can be challenging and extended flux activations times may be required to fully clean the substrate

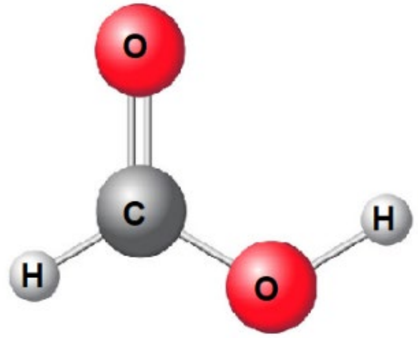


- Post-bonding flux cleaning step is required even for ‘no-clean’ materials:
  - Flux residual clean-up required for high package reliability after underfilling
  - Thorough cleaning of large chip areas with small chip gap and/or high density interconnects can be challenging and time consuming

Advantages of Fluxless TCB Process

- No pre-applied flux or flux cleaning steps
- No flux vapor contamination of equipment, tooling, or sensitive components such as optical/photonics devices
- Possible to run higher substrate and/or die contact temperatures for higher quality interconnects as there is no flux burn off time needed
- Higher accuracy/more consistent alignment possible as there is no flux for the vision to see features through

Oxide Reduction via Formic Acid Vapor



Formic acid molecular formula: HCOOH

- **Step 1: Sn (II) formate creation (100°C < T < 150°C)**

$$SnO_{(s)} + 2HCOOH_{(g)} \longrightarrow Sn(COOH)_{2(s)} + H_2O_{(g)}$$

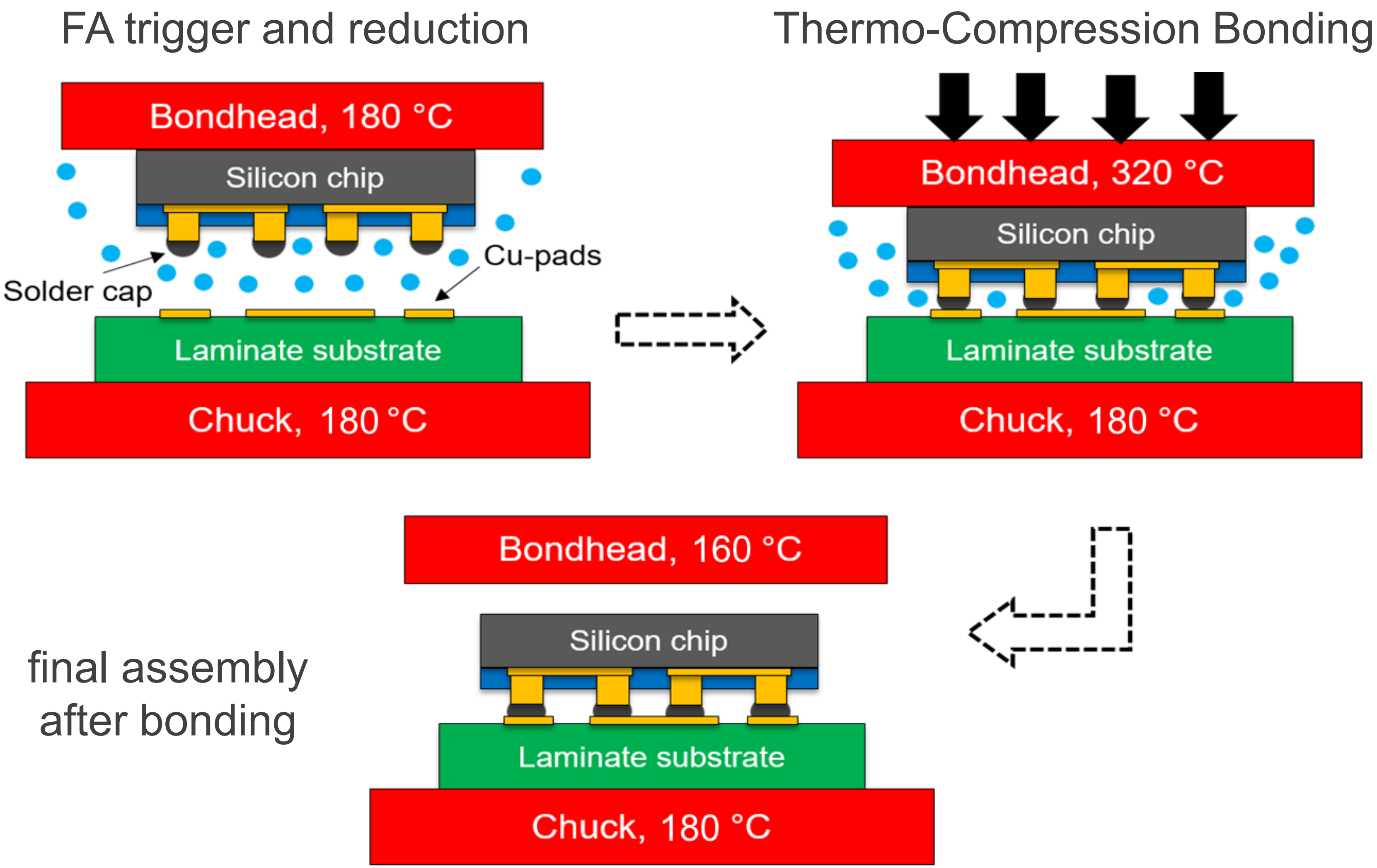
surface oxide on solder | FA vapor | organic tin formate layer replaces oxide | water vapor byproduct

- **Step 2: Sn (II) formate decomposition (T > 150°C)**

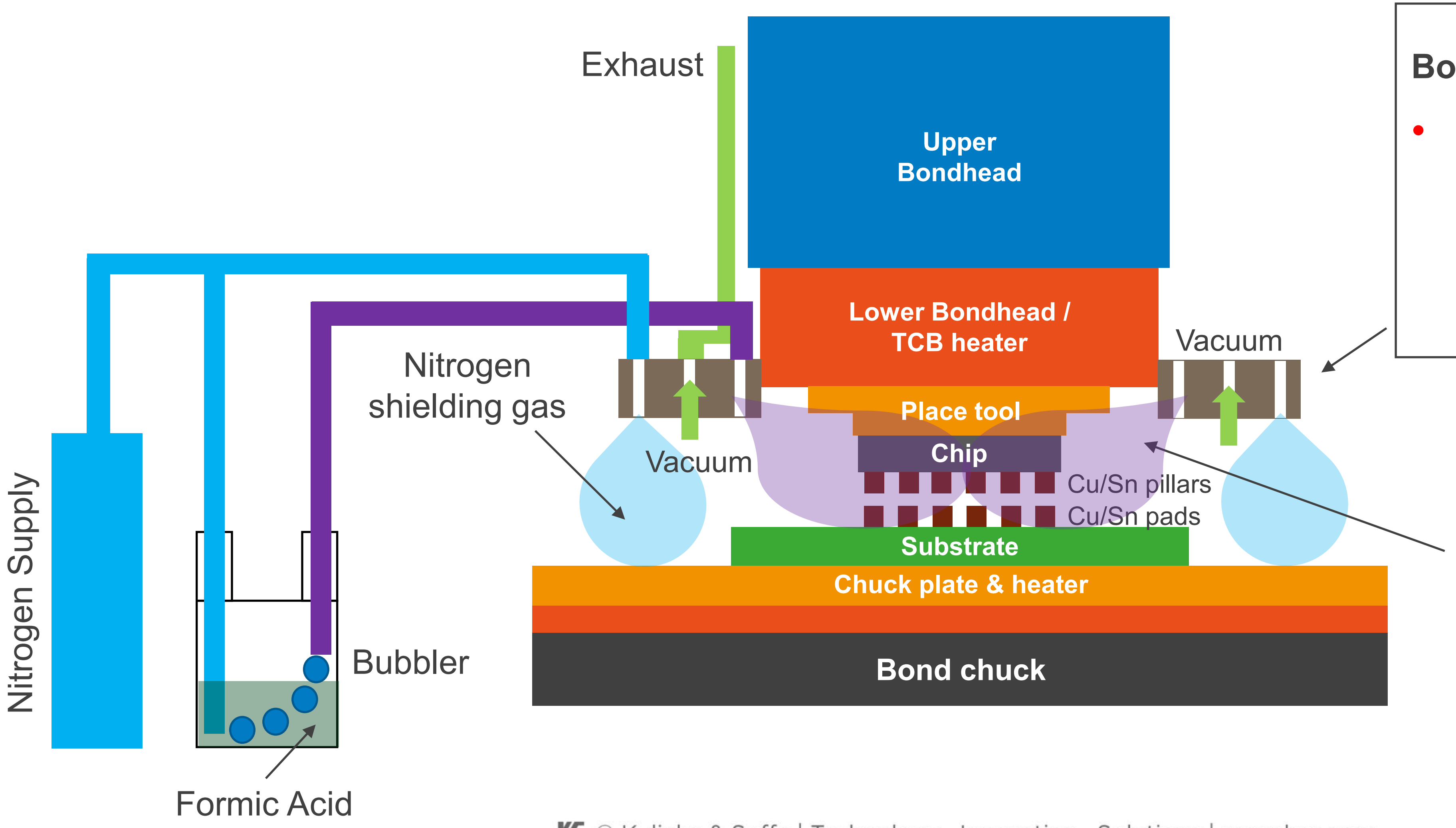
$$Sn(COOH)_{2(s)} \longrightarrow Sn_{(s)} + 2CO_{2(g)} + H_{2(g)}$$

tin layer remains on solder surface | carbon dioxide and hydrogen byproducts

Example In-Situ Formic Acid TCB Process Flow



Schematic of a Formic Acid Delivery System

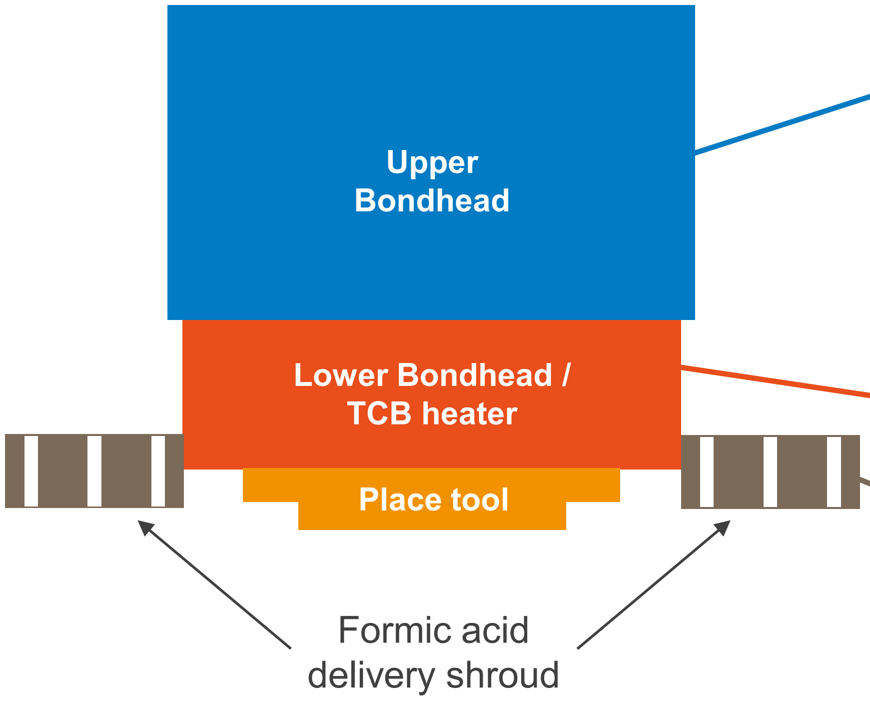


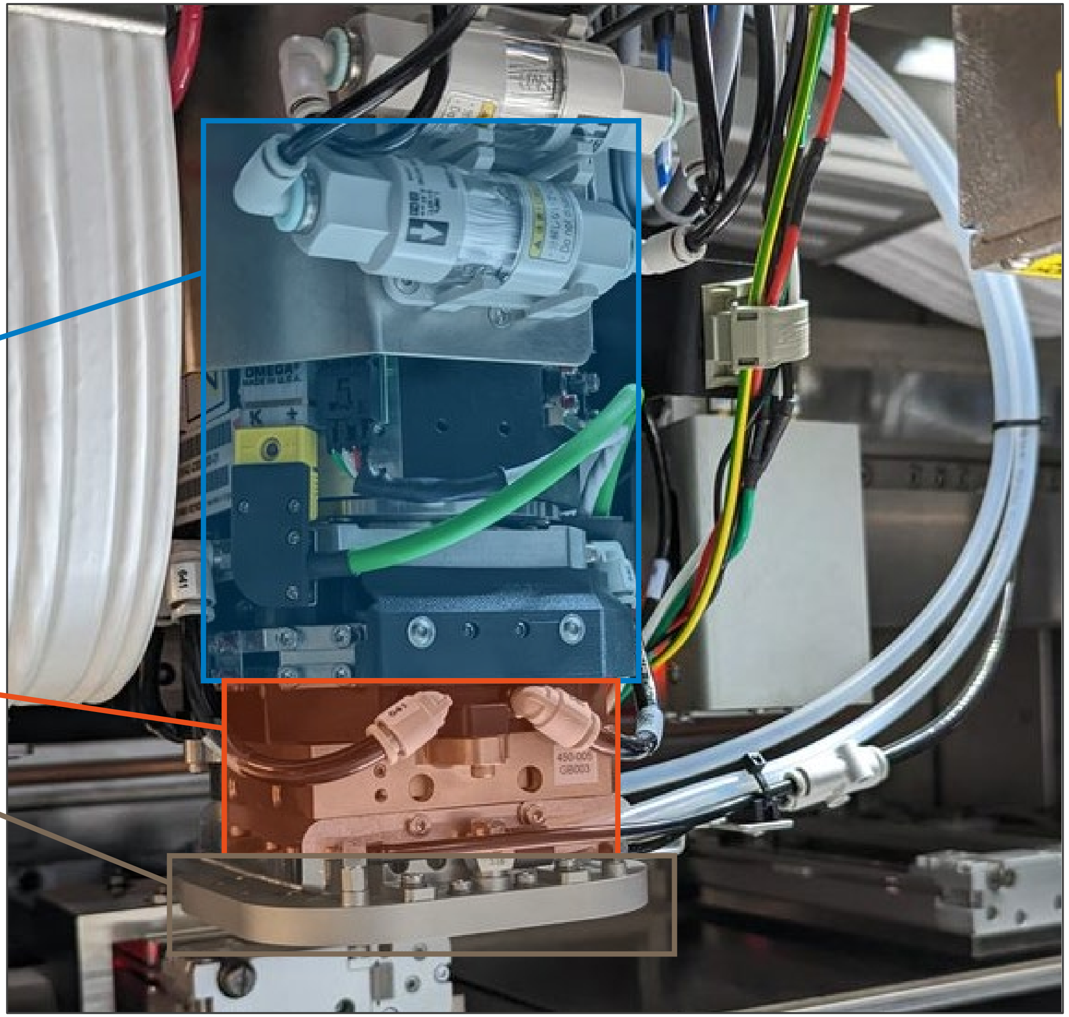
Bondhead Shroud

- The bondhead mounted shroud creates a mini formic acid rich environment prior to and during chip placement

Formic Acid Delivery System Overview

- Formic acid vapor is delivered to the bonding area using a bondhead mounted delivery shroud





Animation of the Fluxless Bond Process

APTURA – 3rd Generation TCB Tool

- Specifically designed for the most demanding TCB processes
  - Large die, ultra-fine pitch 10um, multi-die
- High throughput dual head bonding
- Up to 70 mm die size
- Accuracy < 1.0 um 3S
- Active co-planarity control with non-contact measurement
- Advanced TCB process options
  - Inert environment bond chamber < 100 ppm O2
  - K&S patented flux-less bonding

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Future Accuracy Needs

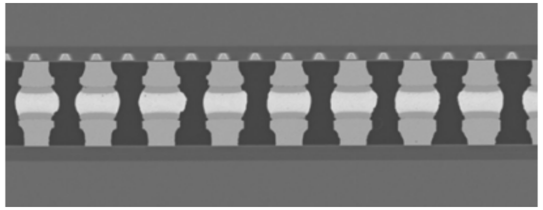
- **Heterogeneous integration and packaging are replacing Moore's law in driving semiconductor performance. This trend is driving interconnect pitch scaling requirements**

Pitch (um)	Bump Dia (um)	Bump gap (um)	Accuracy requirements	Comments
35	24.5 (70%)	10.5	2.0 um	Aptura →1.0 µm
25	17.5 (70%)	7.5	1.5 um	Aptura → 1.0 µm
10	5.5 (55%)	4.5	0.8 um	Aptura Next → 0.8 µm

Intel 10um Test Vehicle

Bump dia = 55% pitch
Source: Intel, ECTC 2022

Intel 20um Test Vehicle



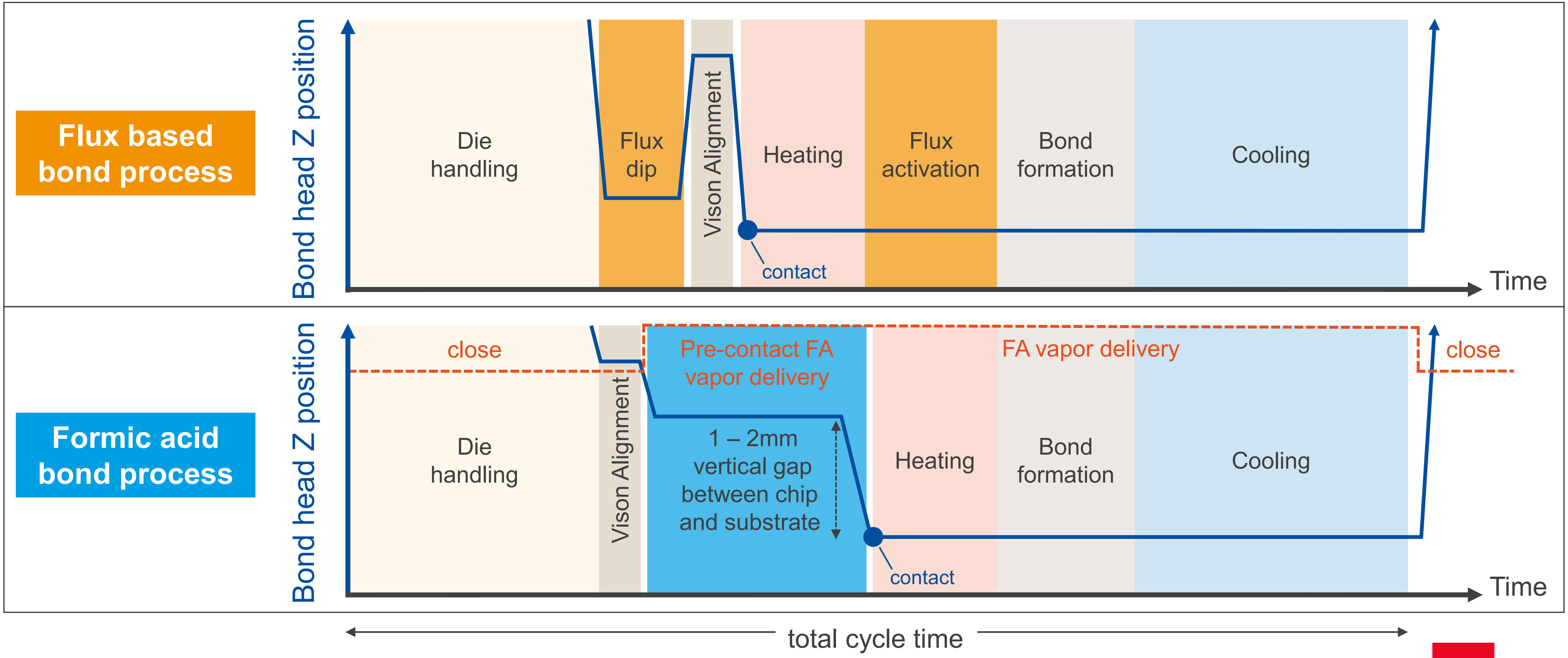
Bump dia = 70% pitch
Source: Intel, ECTC 2022

Fluxless Bonding Productivity

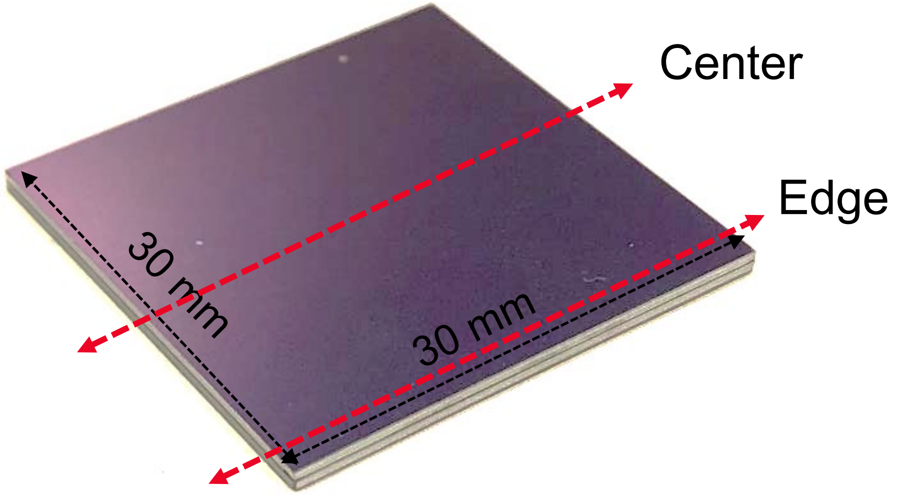
- The fluxless process delivers about the same productivity as a conventional TCB flux based TCB processes
- The formic acid process requires a short pre-bonding cleaning step for formic acid vapor to remove oxides from the chip and substrate
- No time required for flux dipping and flux activation during bonding

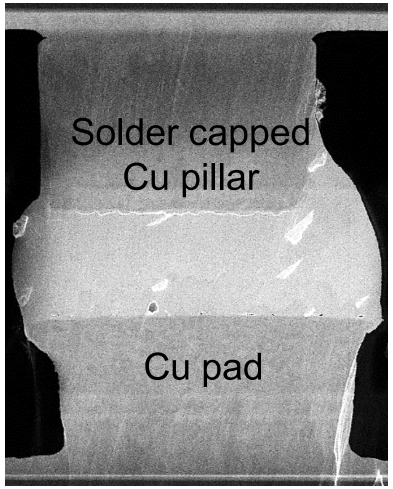
Formic Acid vs. Flux Based Example Bond Cycle

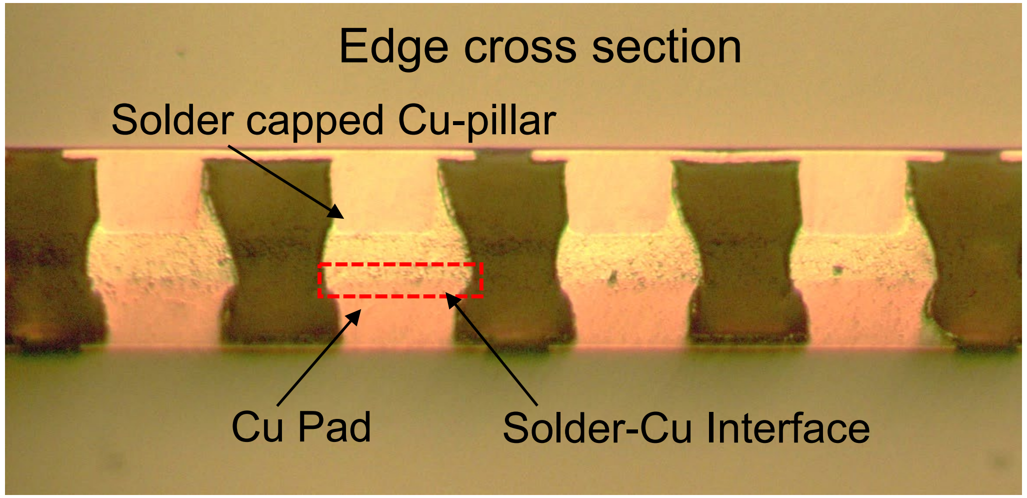
- The FA process delivers nearly the same productivity as a conventional flux based TCB process:



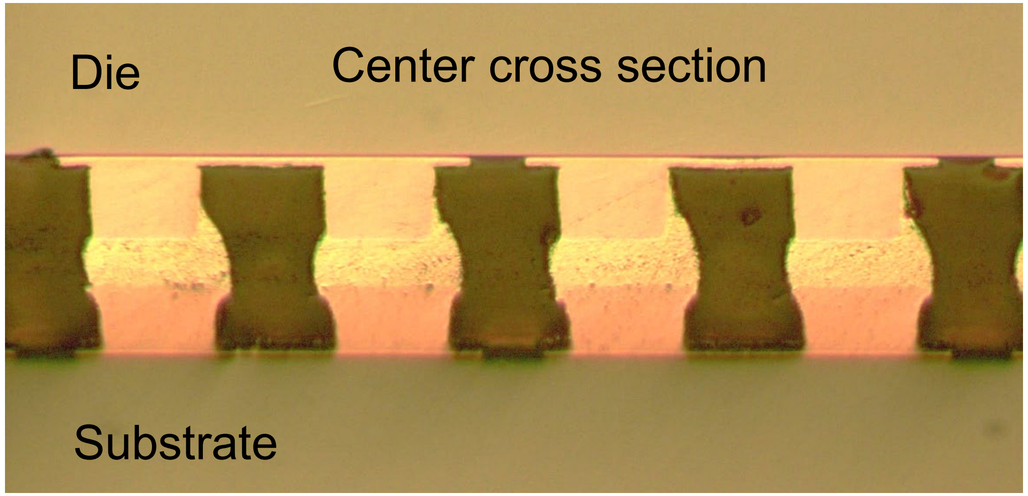
Copper-to-Solder Fluxless Bonding in Inert Environment







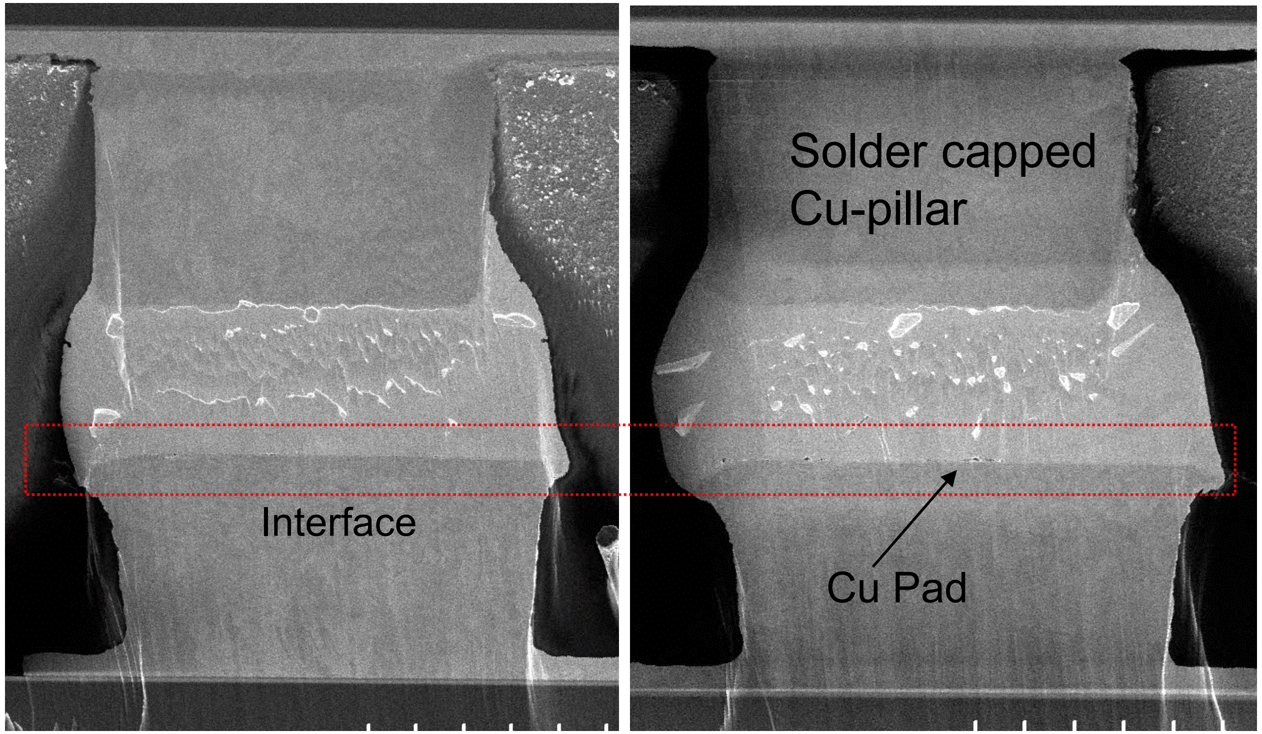
- 30 mm X 30 mm die-to-die assembly
- Top die: Solder capped copper pillar
- Bottom die: Cu pillar
- Interconnect: Cu-to-Solder



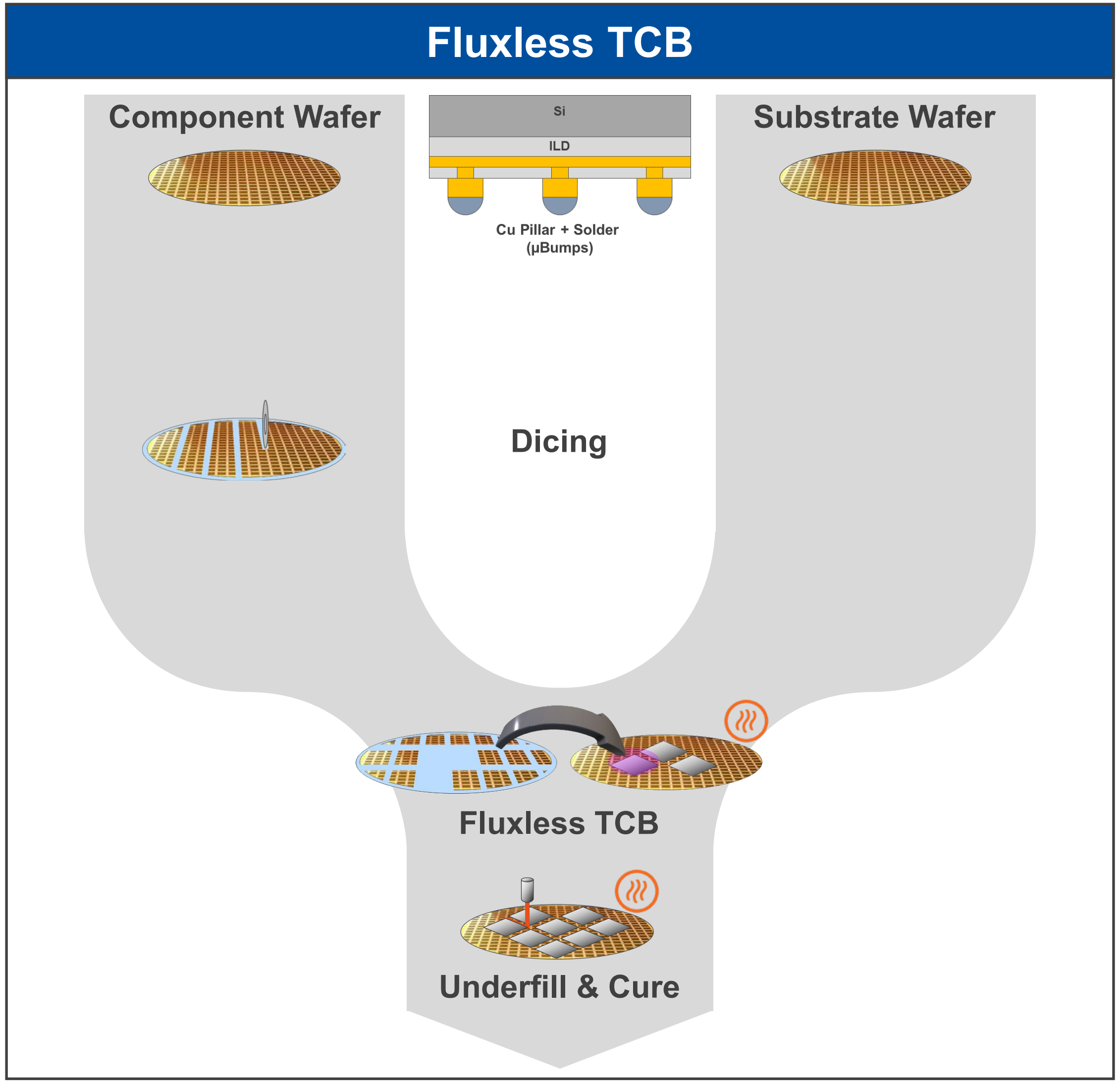
Cu-Solder Bonding in Inert Environment after 45min Heat Exposure

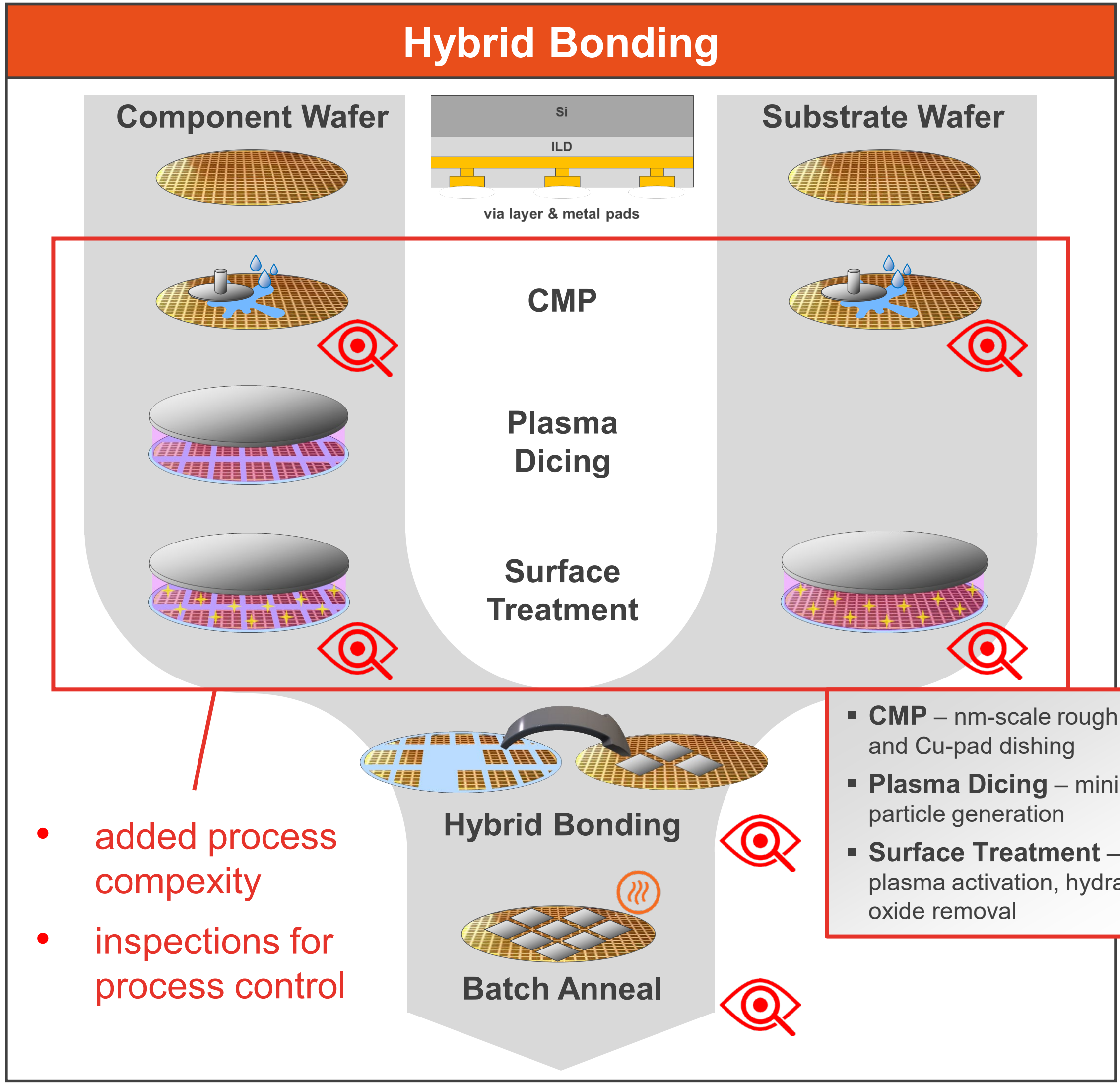
- Pre-bond FA vapor cleaning time 1 sec

- Cu surface was held at 150 C in nitrogen for 45 min before bonding process
- Oxygen concentration in nitrogen chamber was less than 100 ppm
- Localized FA supply get rid of any natural or existing copper oxides prior to bonding step



Fluxless TCB vs Hybrid Bonding – C2W Process Flows





- added process compexity
- inspections for process control

- **CMP** – nm-scale roughness and Cu-pad dishing
- **Plasma Dicing** – minimized particle generation
- **Surface Treatment** – clean, plasma activation, hydration, oxide removal

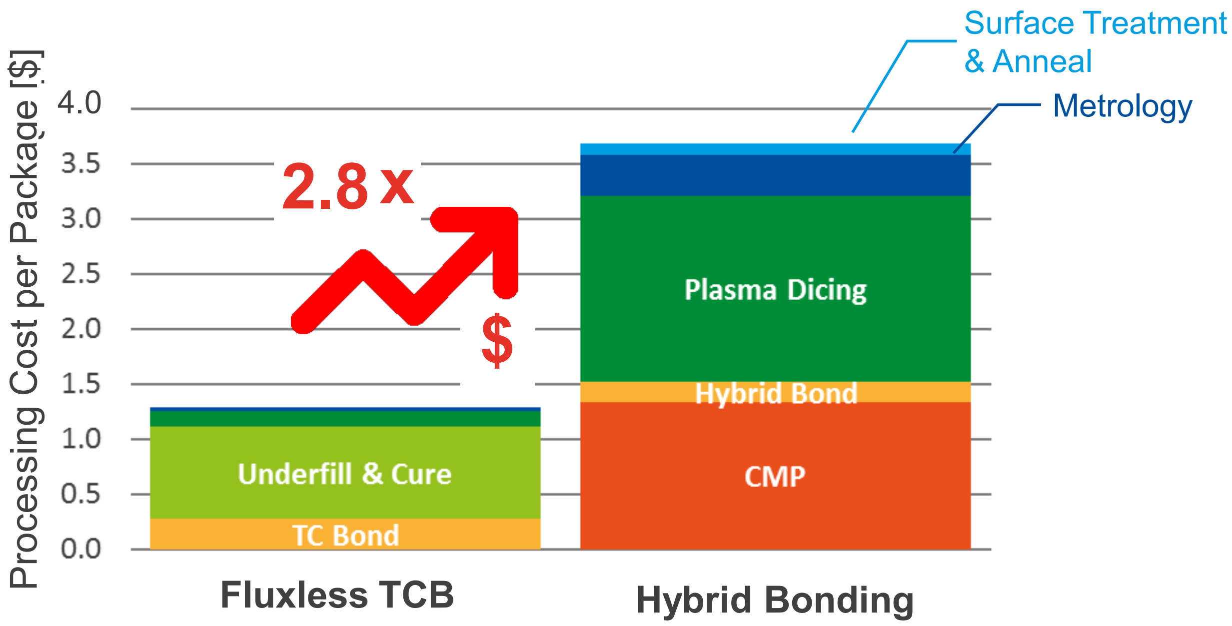
Fluxless TCB vs Hybrid Bonding – Pro's & Con's

Packaging Considerations	Fluxless TCB	Hybrid Bonding
• Finest Pitch	20µm, extendable to 10µm or below	< 10µm
• Productivity	up to 1200 units per hour	1000 – 2000 units per hour
• Process Sensitivity to Debris	not sensitive to small debris	super critical – small debris = yield loss
• Assembly Cleanliness Req's	use existing facilities	similar to Front-End
• Die Surface Roughness	no change from current practice	special CMP, < 0.5nm Ra, Cu dishing critical
• Die Surface Preparation	no change from current practice	wet clean, plasma activation, hydration, oxide removal
• Special Dicing Requirements	no change from current practice	plasma dicing
• Cu Area vs Dielectric Layout	no special requirements	Needs carefully control – Cu distribution and %
• P&P Accuracy Requirements	proven 1µm @ 3σ	< 200nm @ 3σ
• Bonding Process	large temperature cycle	room temperature bonding, very low force
• Interconnect	liquidous	non-liquidous – special (1,1,1) plating R&D
• Underfill	ultra fine pitch challanges – exploring new methods	no underfill required
• Start Up Cost	natural extension of TCB	huge investment required
• Cost of Ownership	lower cost	higher cost

Fluxless TCB vs Hybrid – Process Cost Comparison

SavanSys
www.savansys.com

- Bottoms-up «acitivity-based» cost modeling, allocating cost to each process step:
  - Cost categories: labor, capital, material/tooling, yield loss# and indirect/OH cost



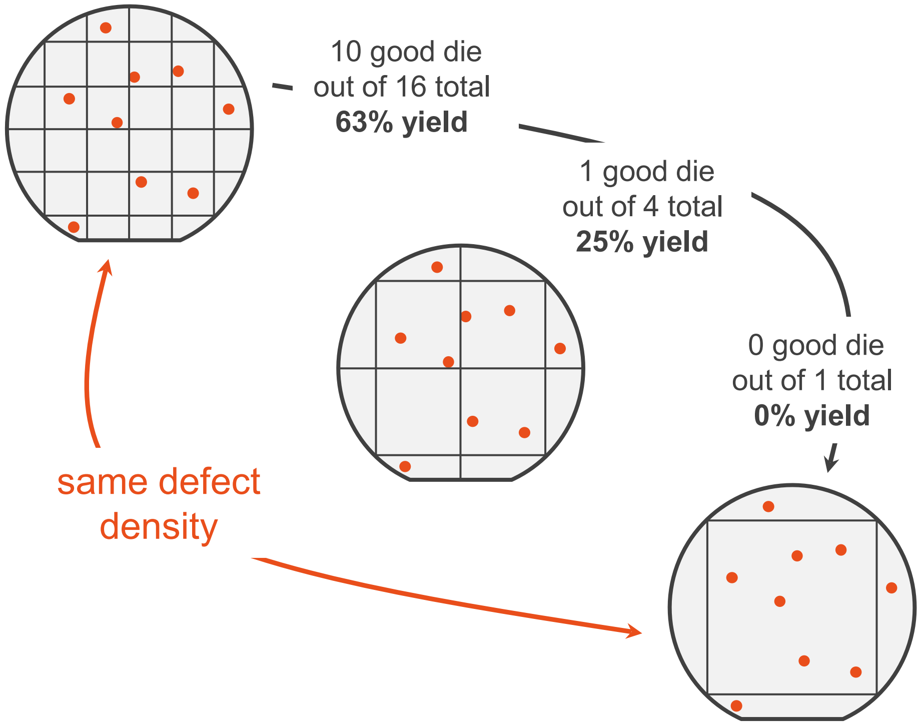
Assumptions:
- Process cost comparison assumes 100% yield for both processes.
- Package cost includes Si cost (~9'300$ per 7nm node wafer)
- Assumes Large Die.

Fluxless TCB vs Hybrid – Yield & Package Cost Comparison

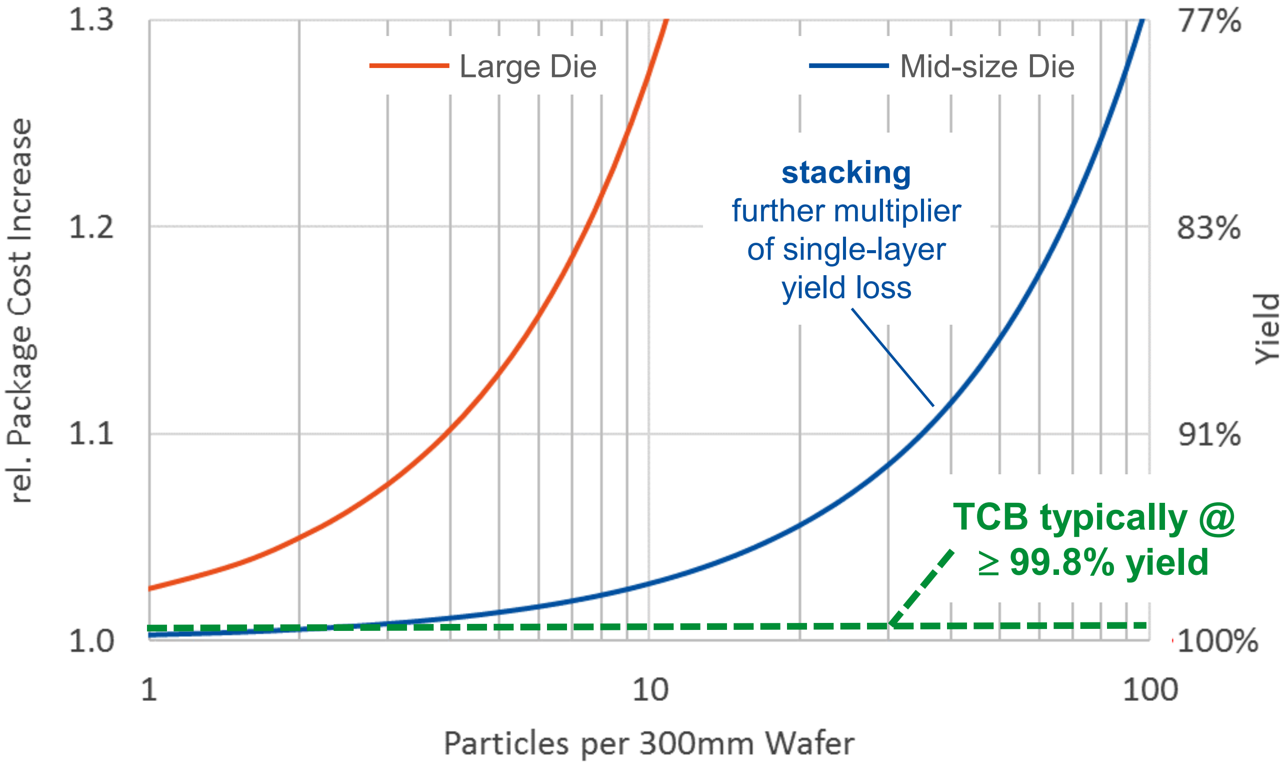
SavanSys
www.savansys.com

- TCB much less sensitive to particles, Hybrid Bonding requires front-end cleanliness
- Small particles covered in underfill or solder – no effect for TCB

- Hybrid Bonding yield drastically dropping as die size increases:



- Hybrid Bonding package cost vs defect density#:



#Assuming particles as the only source of yield loss, i.e. perfect alignment, perfect Cu pad dishing, etc.

High Density Cu-Cu Interconnects : K&S-UCLA Partnership

- Cu Pillar pitch: 10 µm
- Total contacts per chip: 36,000
- Roughness on both pillar & pad : < 2 nm
- Test vehicles fabricated by UCLA
- TCB Tool: K&S with FA delivery system

UCLA

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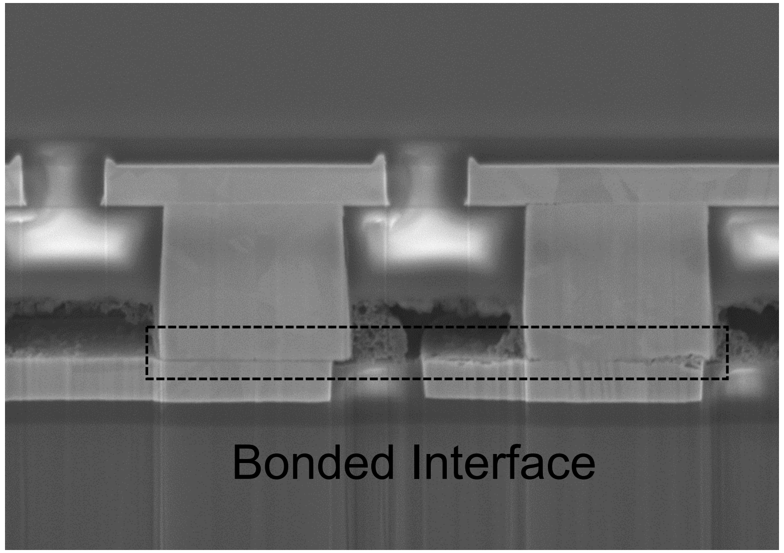
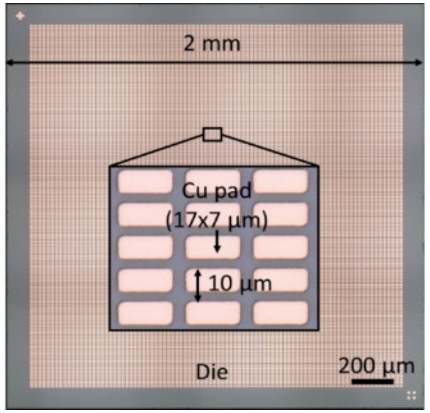
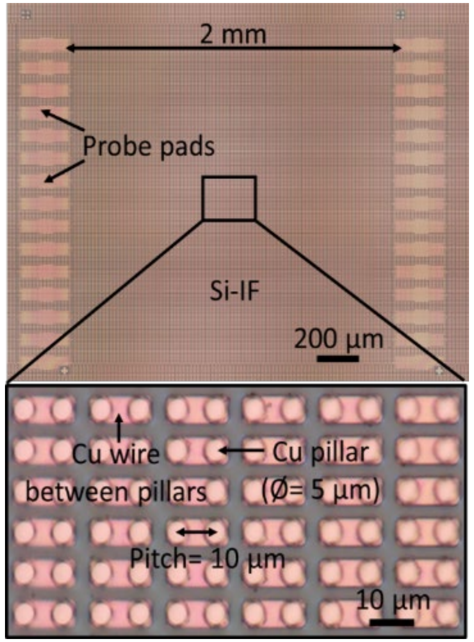


Chip with bond pads



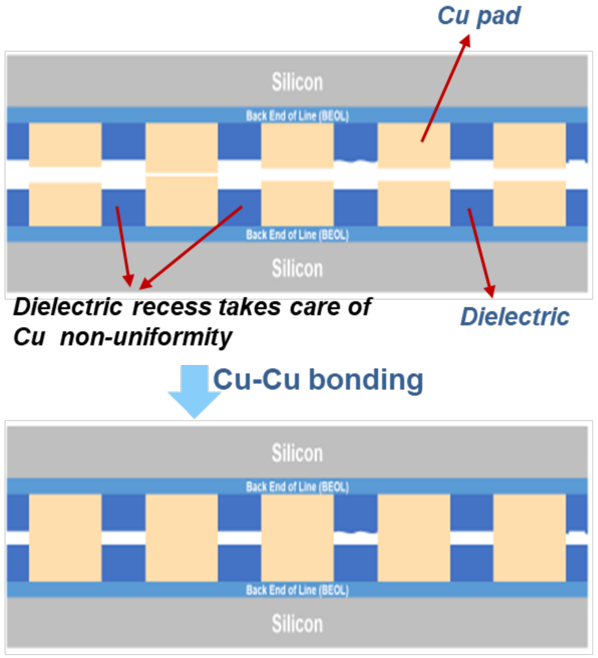
Substrate with Cu-pillars



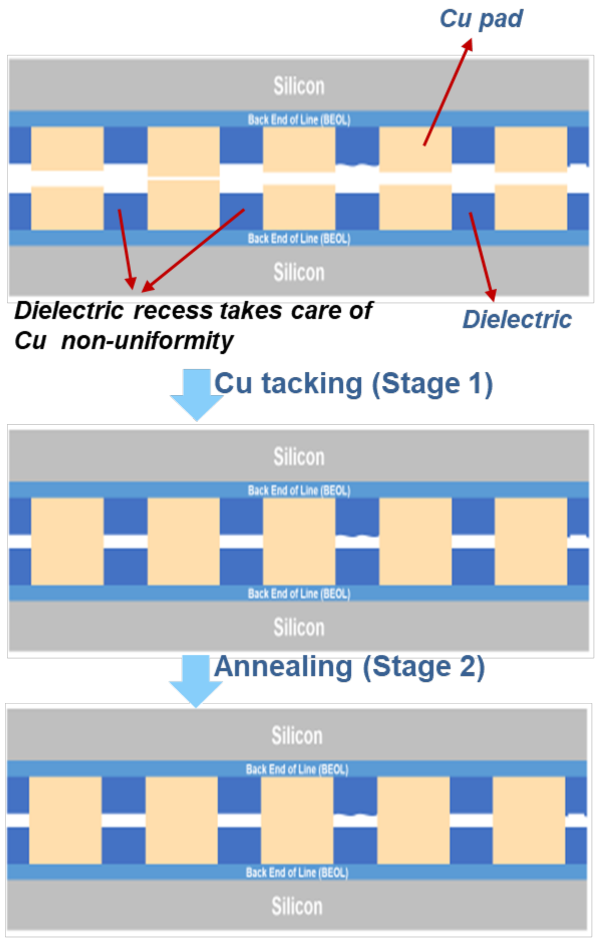
S. Jangam *et al*, ECTC 2019
K&S-UCLA Paper

Improving throughput of conventional TCB

Conventional thermal compression bonding



Two-stage thermal compression bonding



- Conventional TCB has challenges
  - Single step TCB is time consuming (30s – 40s/die)
- To overcome these challenges, we propose a two-stage TCB.
  - **Stage 1:** die tacking process (< 10s).
  - **Stage 2:** batch annealing process
  - Annealing several wafers at once eliminates anneal time as a throughput concern.
  - Current process **> 320 UPH (~11.2s/die)**

Throughput improvement

- **90 UPH → 320 UPH → 1100 UPH**

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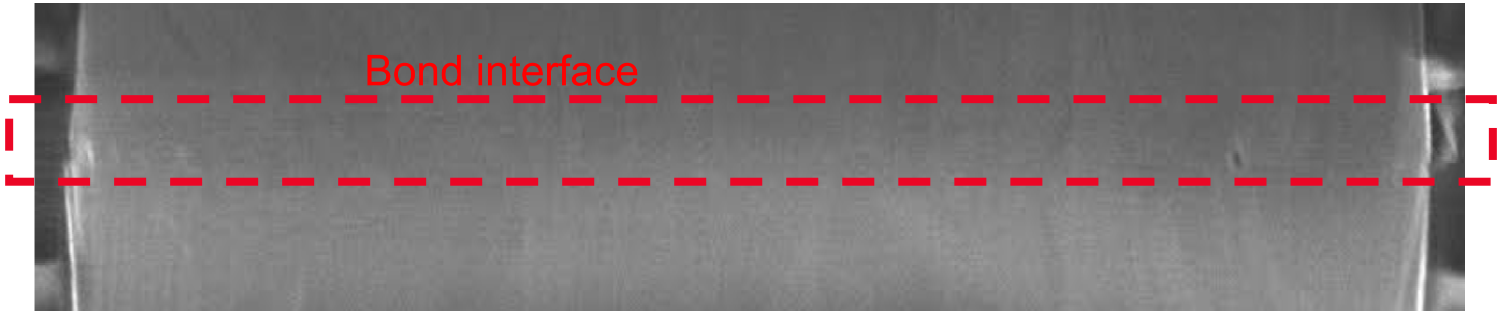
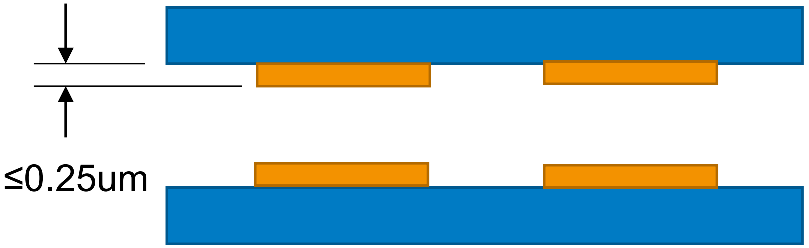
Executive summary

- We have developed a high throughput (up to 1000 UPH) thermal compression bonding scheme using a novel two-stage bonding approach.
- We have achieved 2x MIL-SPEC bonding strength (> 100N for 2x2mm^2 dielets) post anneal with specific contact resistance ~ 1.2x10^{-9} ohm-cm^2.
- We have demonstrated MIL-SPEC reliability using UHAST 96 hours testing.
- We believe that TCB using this scheme is a viable and **potentially more manufacturable assembly process** down to ~7 µm bump pitches, with further scaling possible with tool alignment improvements.

Hybrid-like Cu-Cu Formic Acid Process on the Aptura

- We've developed a Cu to Cu interconnect for customers as an alternative to Hybrid bonding
- Process uses very short pads on the die and substrate prepared with low roughness
- The Formic acid TCB process uses < 5 sec total cleaning and bonding time which results in well attached chips, in a class 10k cleanroom
- The CMP like finish helps to enables reduces bonding pressures to <10 MPa (applied for 2 sec.)
- Process is capable of fine pitches < 10 um
- No additional equipment upgrade needed beyond the normal formic acid
- 2 step process: Cross section image shows an example bond before annealing





Summary

- Heterogeneous integration and packaging are replacing Moore's law in driving semiconductor performance. This trend is driving interconnect pitch scaling requirements
- Flux contamination and residue limits the pitch of thermo-compression flip chip and is a serious problem for ultra fine pitch interconnect
- K&S has developed a fluxless TCB process for chip to substrate and chip to wafer bonders which solves problems with flux
- The process is capable and being used for Sn to Sn, Sn to Cu, and Cu to Cu interconnect
- Formic acid vapor fluxless TCB can extend the pitch capability for flip chip packages down to 10 – 20µm and possibly beyond
- Fluxless TCB bonding is an extension of standard semiconductor assembly practices and does not require massive process and infrastructure changes that Hybrid bonding does
- The process and equipment have been matured and are in high volume manufacturing

Questions?

Thank You!

Copyright Statement

Fluxless High Volume Manufacturing Readiness

- Chemical safety has been designed into the formic acid (FA) bonder system from the early design stages
- Machine conforms to multiple chemical safety standards including SEMI S2, S6, and EN 1127-1
- Machine features redundant sensors/valves on safety critical functions and safety systems are monitored/controlled by a safety rated PLC
- FA is only flammable under a limited set of conditions, however all electronics that could be exposed to formic acid under normal and failure condition are protected by intrinsically safe barriers
- Additionally multiple environmental monitor sensors are present to monitor FA vapor concentration at various points in the machine

12/2017 – Version 1 FA shroud tested

6/2018 – **Prototype FA TCB system shipped to UCLA CHIPS#**

11/2018 – External chemical safety expert engaged

9/2019 – Version 4 FA shroud tested

1/2020 – Version 1 HVM gas delivery system prototype testing

3/2021 – Version 2 HVM gas delivery system design started

6/2021 – Design review with external chemical safety expert

7/2022 – **3rd party safety audit completed successfully**

9/2022 – **1st HVM bonder shipment**

#University of California, Los Angeles, Center of Heterogeneous Integration and Performance Scaling

Thermal compression bonding is NOT demanding

	Hybrid Bonding	Direct thermal compression bonding
Process Development	• Necessitates meticulous control over 1) dielectric flatness (6σ roughness ≤ 1 nm) and 2) metal recess • Extensive CMP optimization	• Simpler process development: only optimizing the metal-metal bonding • Relaxed CMP requirements
Dicing process	• Mandatory particle-free dicing.	• Cu pads/pillars are recessed so, blade dicing with standard wet cleaning is feasible.
Bonding environment & activation	• ISO-4 or below (Literature suggests ISO-2) • Plasma activation and particulate removal prior to bonding is crucial.	• ISO-8 and above, even outside cleanroom. • Requires in-situ reducing environment during bonding – studied extensively [1].
Dielet size	• Almost any size due to less tacking pressure requirements.	• Limited by max. bond-head pressure during tacking. • Works well for dielet sizes within dielet golden regime.
Throughput	• 1000+ units-per-hour (UPH) due to fast dielectric bonding during tacking phase.	• 1000+ UPH possible with **optimized tack and anneal process**.
Conclusion	• **TCB has low process development cost as well as low operation cost compared to HB.** • **TCB is less sensitive to particles during dicing and bonding.** • **Therefore, we believe TCB should be used for bonding pitches up-to 7 µm.**	

[1] S. Jangam and S.S.Iyer, T-CPMT 2021

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