Hybrid Bond Interconnect and Advanced Packaging Solutions

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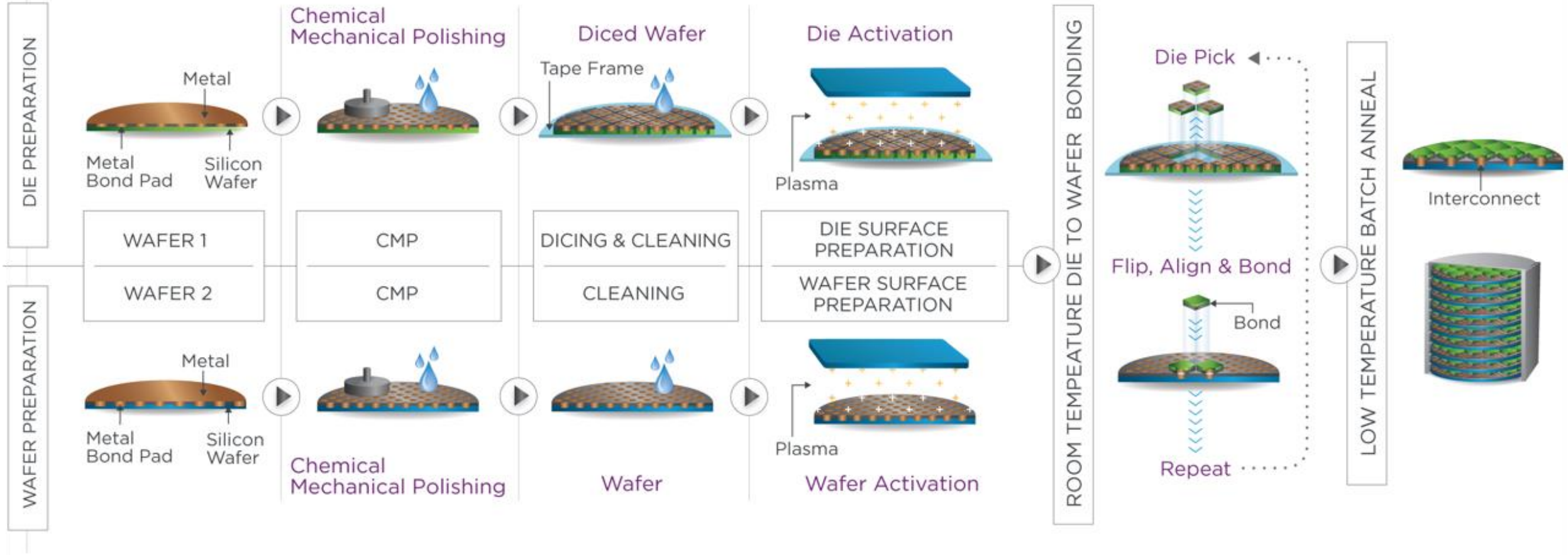
Outline

- Hybrid Bonding Overview
- Criteria for HVM-compatible D2W Hybrid Bonding
- Adeia Demonstrated Range of D2W Hybrid Bonding
- Summary

DBI® Ultra Process Flow

Die to Wafer Hybrid Bonding



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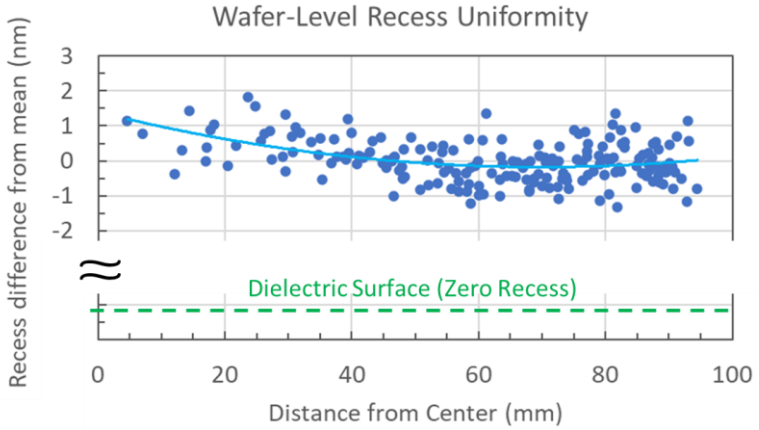
Criteria for HVM D2W Hybrid Bonding

- Robust nanoscale surface engineering (CMP)
  - Smooth dielectric with recessed metal bond pads
  - Tight control of mean metal recess depth
  - Minimal within wafer and within die recess variation



- Processing from Dicing through Bonding must be compatible with HVM
  - Processing in appropriate clean environment (~ISO 6)
  - Saw, Laser Stealth, or Plasma dicing can be used depending on specifics of the device
  - Dicing and post-dicing processing performed with wafer on tape frame
  - Process needs to be compatible with long queue times (weeks)

- Pick and place bonder design must be compatible with hybrid bonding
  - Alignment accuracy suitable for device pad / pitch (3σ <0.25 x Pad Size)
  - Bonding mini-environment & robotic motions compatible with particle control down to 0.2 μm

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D2W Hybrid Bonding Assembly Considerations

D2W Hybrid Bond Parameters Validated by Adeia Test Vehicles:

- Pad Size & Pitch
    - Required Bonder Alignment Capability
- Die Size
    - Yield vs Die Size Considerations
- Die Thickness
- Interconnect Layout and Edge Exclusion
- Multiple Chips / Die (non-stacked)
- Die Stacking (# Layers)
- Anneal Temperature
- Reliability Testing

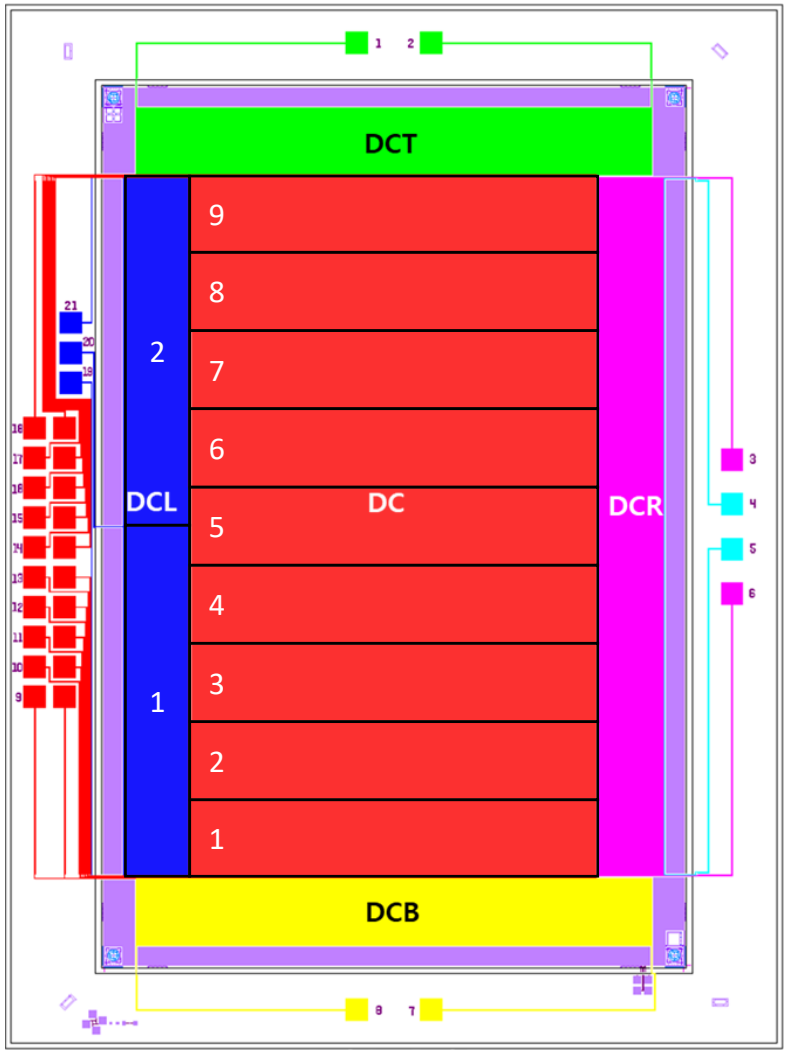
Typical Adeia D2W Test Vehicle

Fine-Pitch Test Vehicle

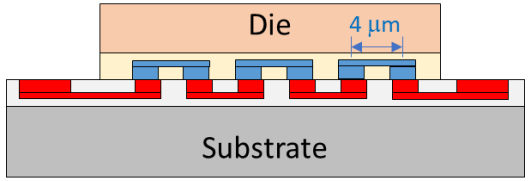
- 8 x 12 mm x 200 μm thick die
- 2 μm pad on 4 μm pitch
- Daisy Chain Arrays:
  - 5 major blocks / 15 sub-chains
- E-Test measures chain resistance
- Manually processed in ISO 6 cleanroom

Array	Area (mm^2)	Links	Features
Center Main (DC)	50	1,600k	9 subchains
Top & Bottom (DCT) (DCB)	6	190k	
Left (DCL)	8	250k	2 subchains
Right (DCR)	8	125k +125k	2 subchains intertwined serpentines

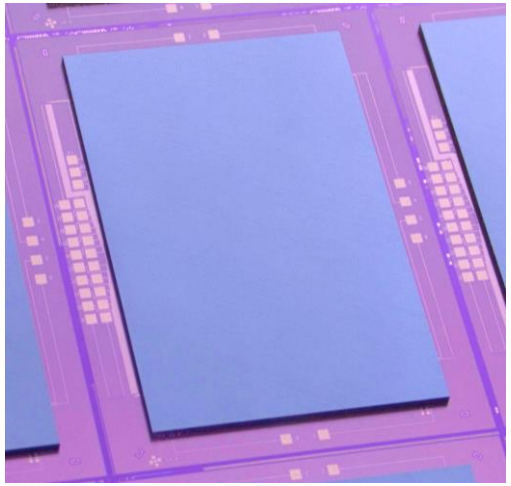
Schematic with Subchains



Schematic – Cross Section of Daisy Chain



Top View – Bonded Die



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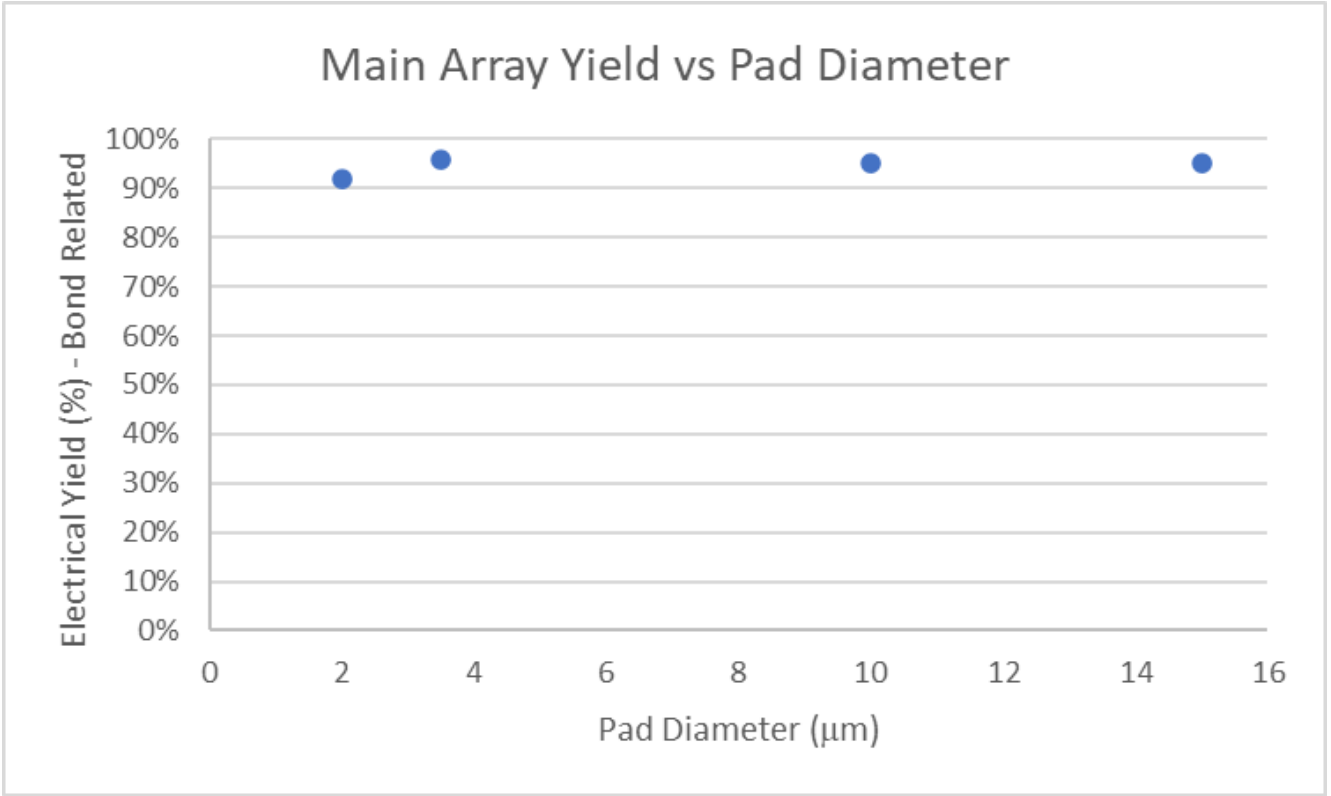
D2W Pad & Pitch Size Range

Test Vehicles: All are 8 x 12 mm die with 50 mm^2 center array

Pad / Pitch (μm)	Main Array # of Links	Bonder / Alignment Capability (±3σ)	
2 / 4	1,600,000	Chameo Ultra-Plus	0.25 μm
3.5 / 7	520,000	Chameo Advanced	3 μm
10 / 40	32,000	Chameo Advanced Evo Plus	3 μm 7 μm
15 / 40	32,000	Evo Plus	7 μm

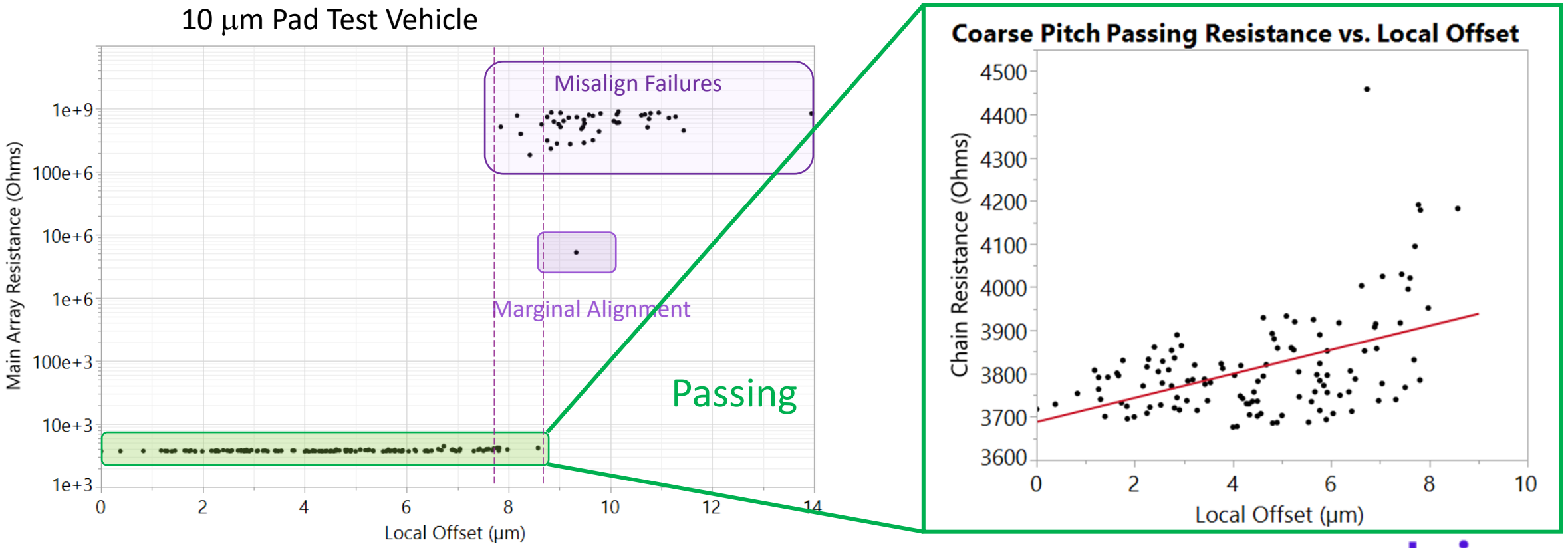


Results

- All test vehicles have electrical yield >90%
- No significant drop in yield with pad size down to 2 μm

Determining Yield vs Misalignment Tolerance

- Perform an intentional alignment skew with misalignment out to >1.2 x Pad Diameter
  - Measure daisy chain resistance & plot vs offset
  - Transition from passing to failing = Maximum Passing Offset
  - Slope of passing resistance vs offset shows bond interface resistance increase due to misalignment



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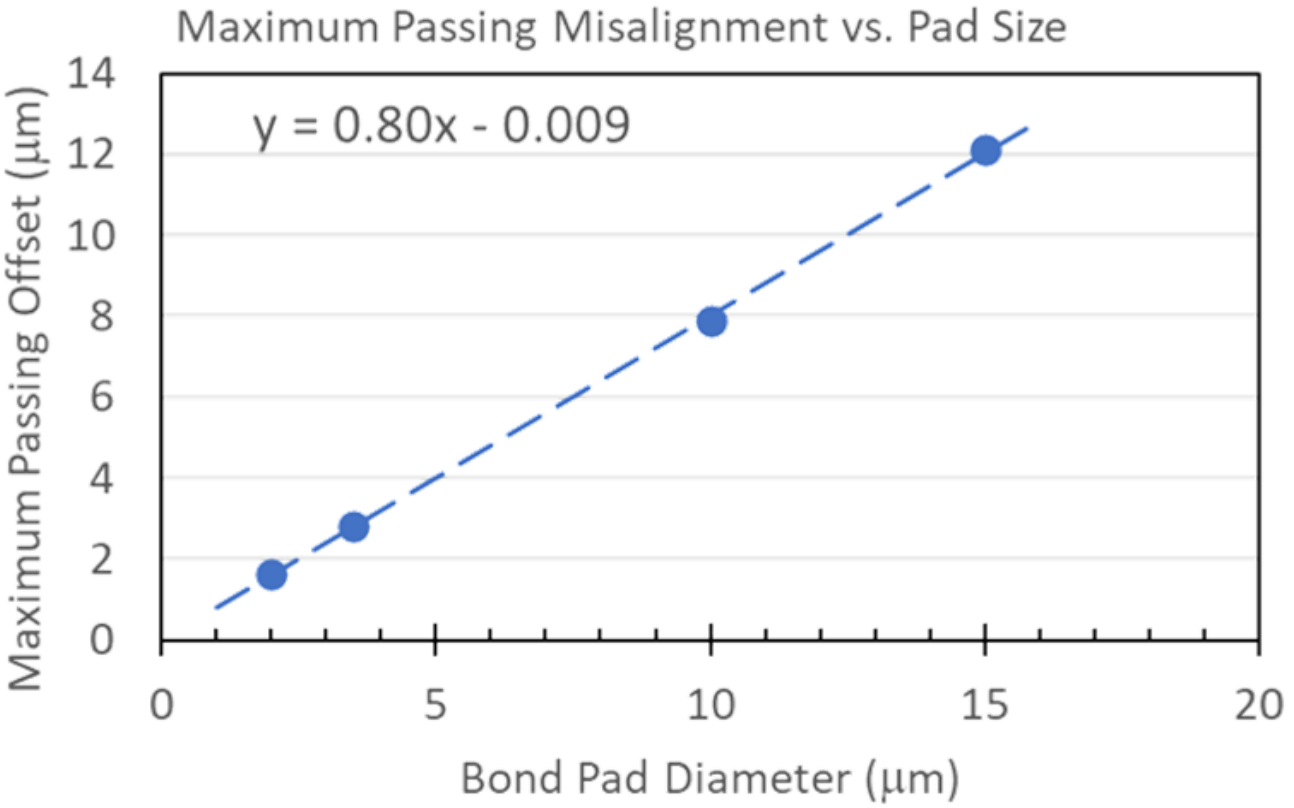
Misalignment Tolerance vs Pad Size



Alignment skew:

- 8 x 12 mm test vehicles
- Pad size ranging from 2 - 15 µm

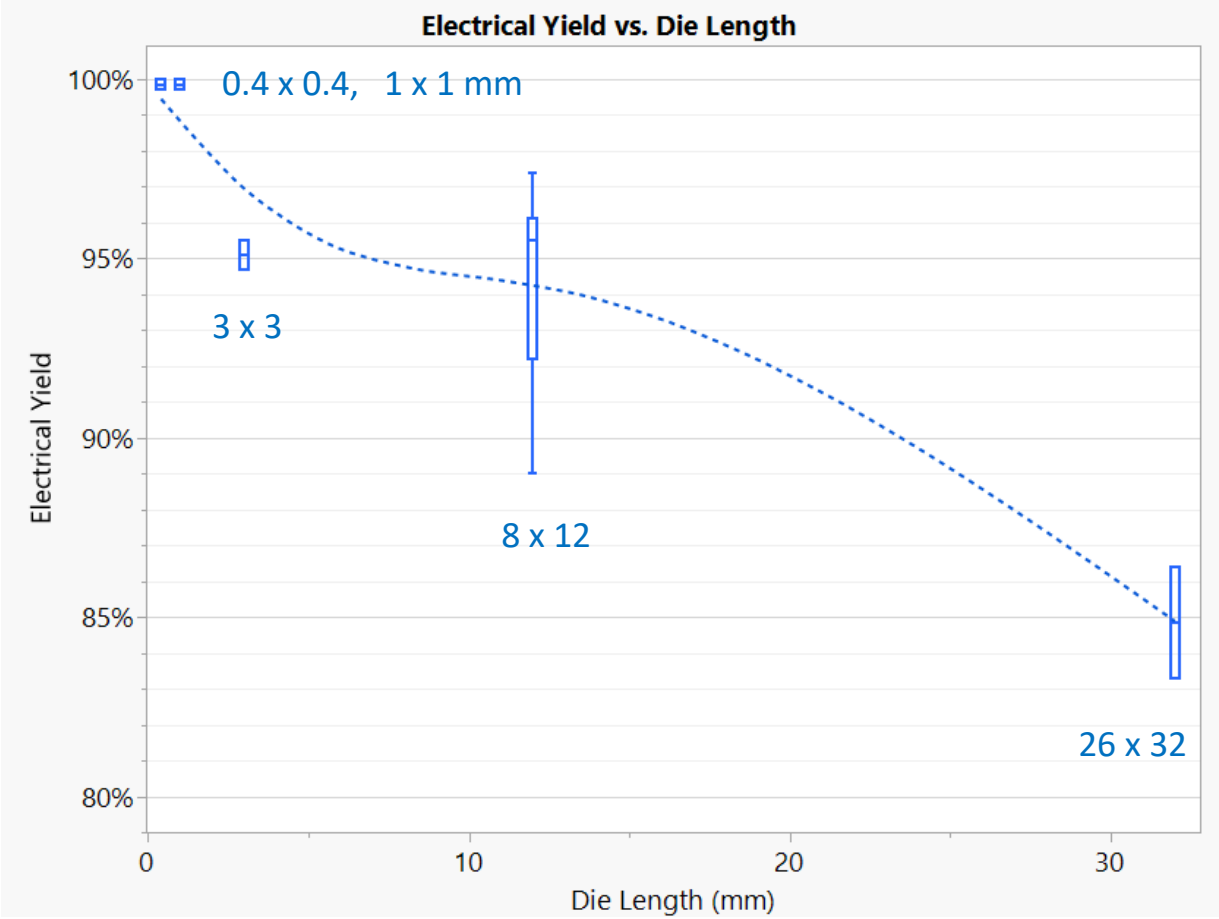
Results

- The misalignment tolerance is at ~80% of pad diameter for all pad sizes tested
- Increase in resistance at Maximum Passing Offset is dependent on specifics of the metal stack, but in general is a 5 – 20% increase, or ~10 mΩ per link

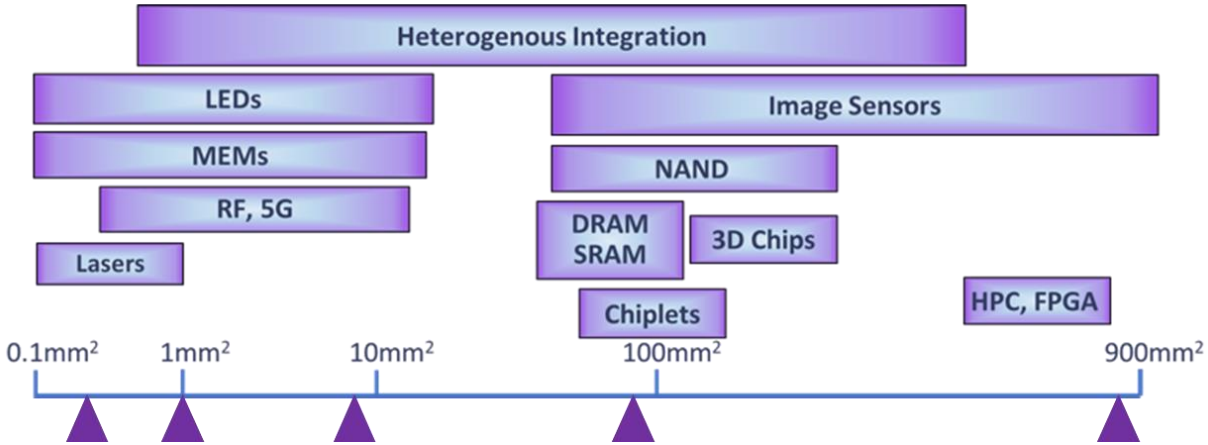
Yield vs Die Size

Test Vehicles

- 0.4 – 32 mm Die Length, all with 10 µm bond pads



Semiconductor Die Size with Application Space



Yield > 99.7% for 0.4 & 1.0 mm Die

Multiple small die have a yield advantage over a large, monolithic die of equivalent area, but advantage decreases as die become small enough that edge defects dominate.

- There is sweet spot in die size ~100 mm²

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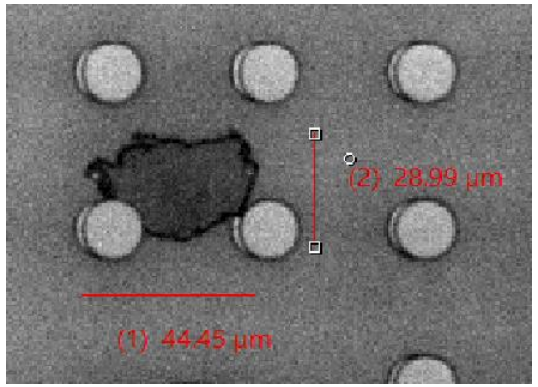
Yield vs Die Size – Failure Analysis

Failure Analysis Methods

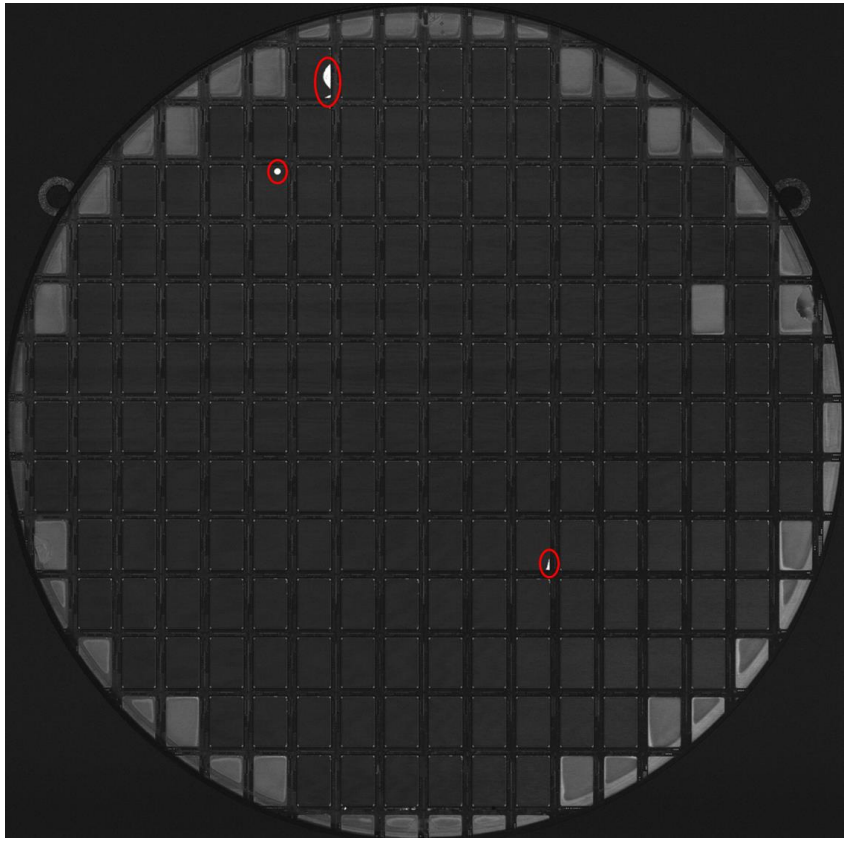
- 100% E-test
- Each E-test failure examined by one or more of:
  - CSAM, IR Microscopy, SEM cross-section

Results

- >99% of electrical yield loss is correlated to voiding
- Voids were randomly distributed within wafer
- Within die, voids were more likely to be at edges or corners
- Vast majority of voids had a detectable particle at the void center
  - Particle size was generally in the 5 – 50 μm range.



IR Image of particle at center of a void

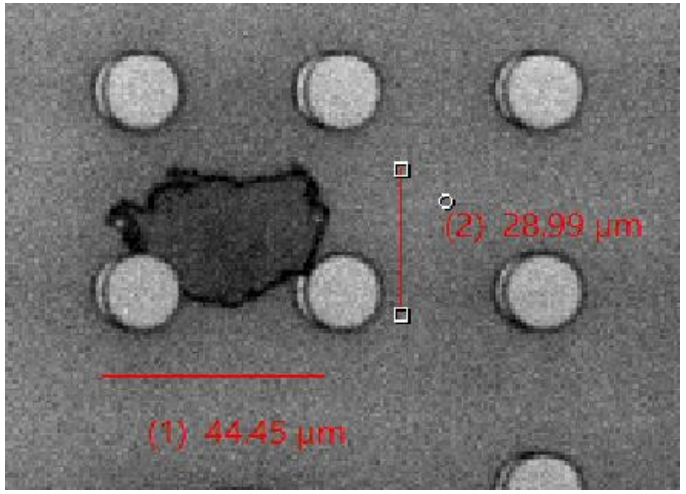


CSAM Image of bonded wafer with 98% Void-free Yield

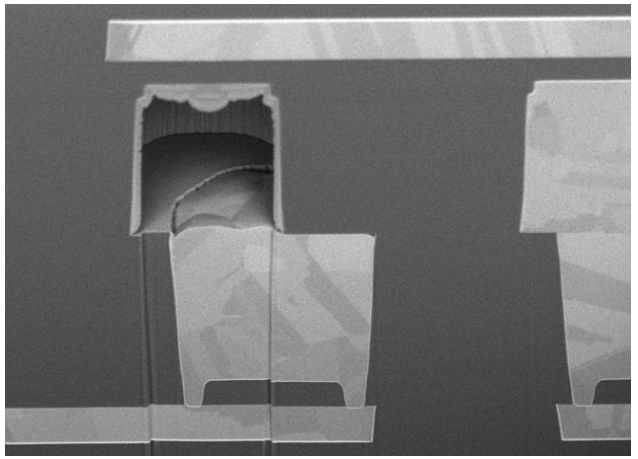
Yield Dependence on Die Size

Potential Sources of Yield Loss:

Defect	Cause
Void	Environmental Particles
Void	Dicing / Edge Quality
Void	Bonder Related: Eject, Flip, Gantry motion
Misalignment	Die Rotation / Deformation
Unconnected bond pads	Excessive Recess Insufficient Anneal
Intrinsic Defects	Defects in metal stack **Not related to hybrid bond**



IR Image of particle at center of void



XSEM of Missing Bond Pad

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Die Thickness

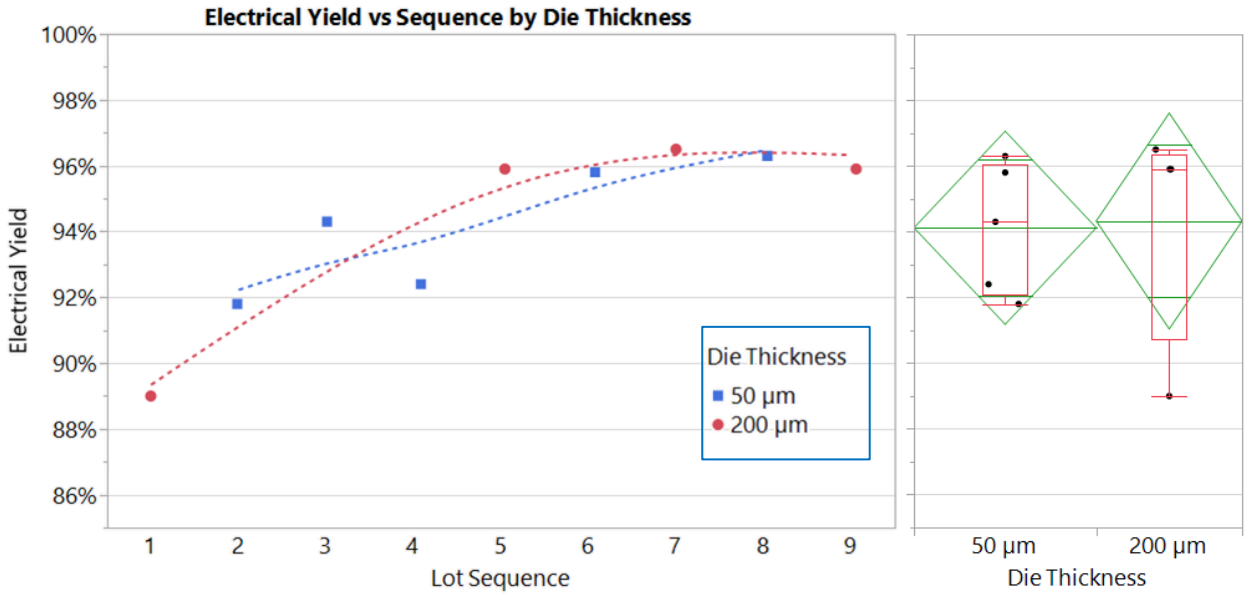
Test Vehicle: 8 x 12 mm Die with 10 μm bond pads, thinned to 50 or 200 μm

Process Flow

- Process flow identical except for thinning process (50 μm required temporary bond to carrier)
- Bonder used the same multi-pin ejector and for both die thicknesses

Results

- Both die thicknesses increased in yield as the process was optimized
- **No decrease in yield for the thinner 50 μm die vs. 200 μm die (statistically equivalent)**

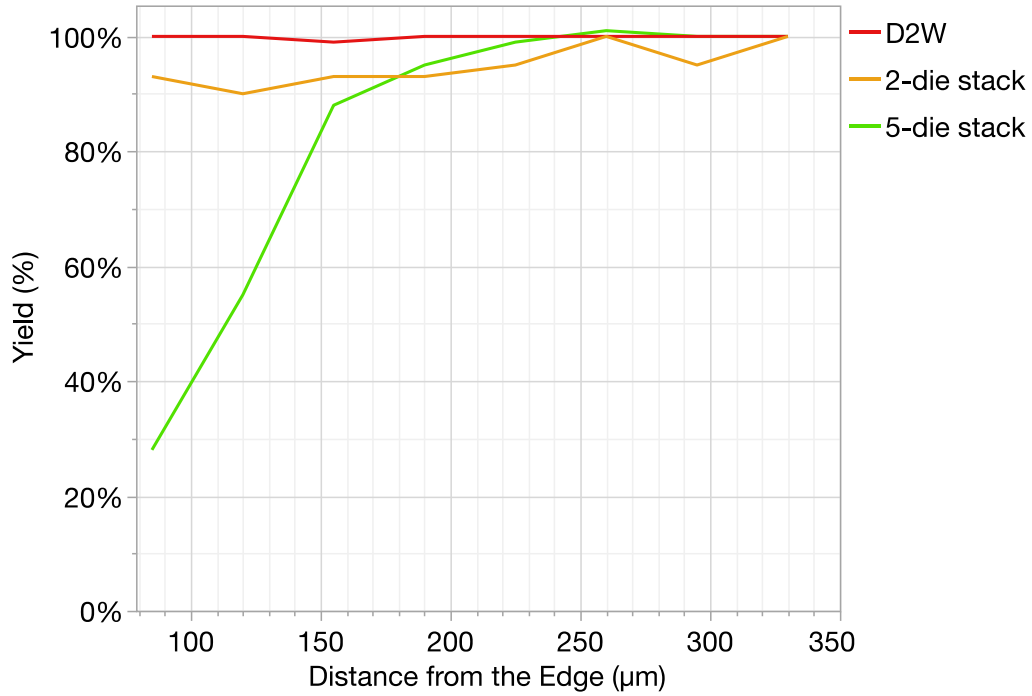


Interconnect Layout and Edge Exclusion

Test Vehicle: 8 x 12 mm Die with 15 μm bond pads, thinned to 50 μm

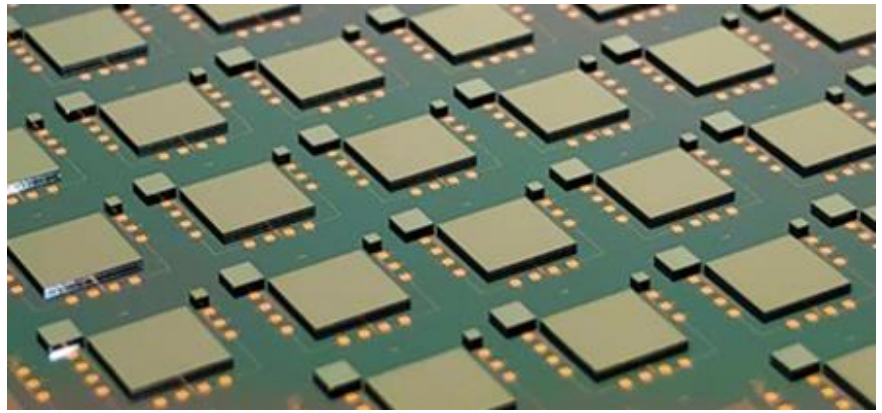
Results

- For single die (D2W), electrical yields >99% are observed down to ~75 μm distance from die edge
- For die stacks, yield loss extends farther from the edge (~200 μm) as stack height increases



Multi-Chip Bonding (2.5 D)

Multi-Chip Test Vehicle



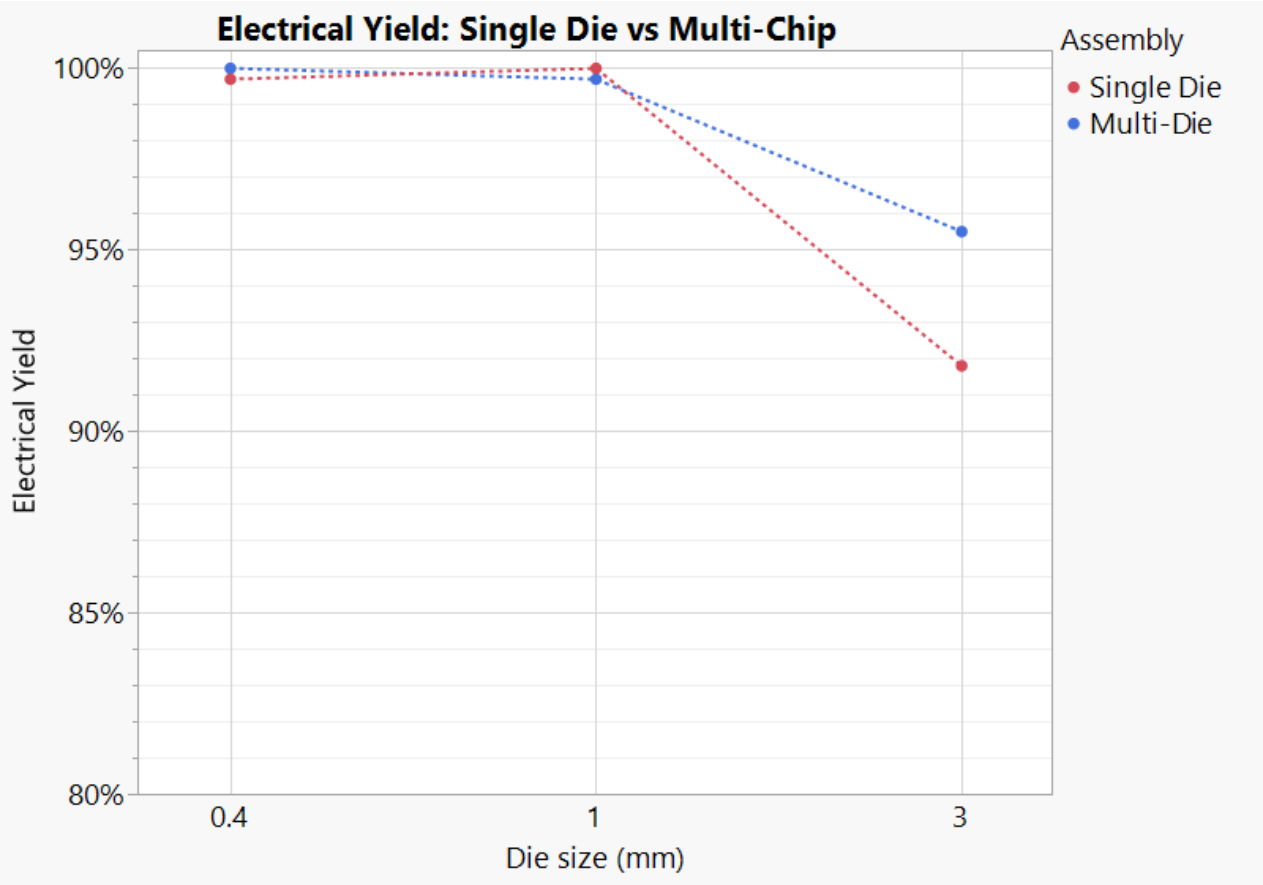
- 0.4 mm, 1.0 mm, and 3 mm Test Die
- Substrate with one of each die type per site

Yield Comparison

- Bond only a single die size per substrate
- Bond all three die sizes sequentially on a single wafer
  - Ejector, Flip Tool, Bond Tool, Dicing Frame setup change between each die size

Result

- No decrease in yield when bonded as multi-chip compared to bonding individually



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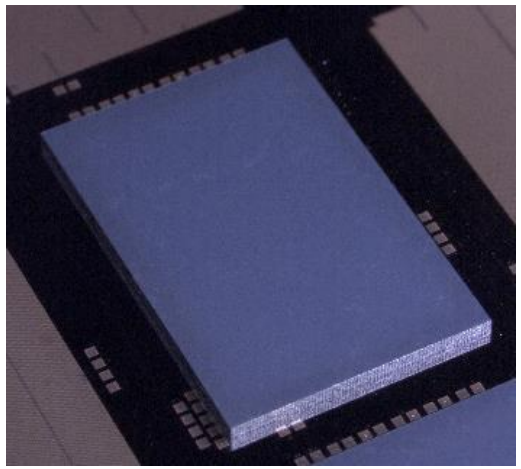
Stacking Yield

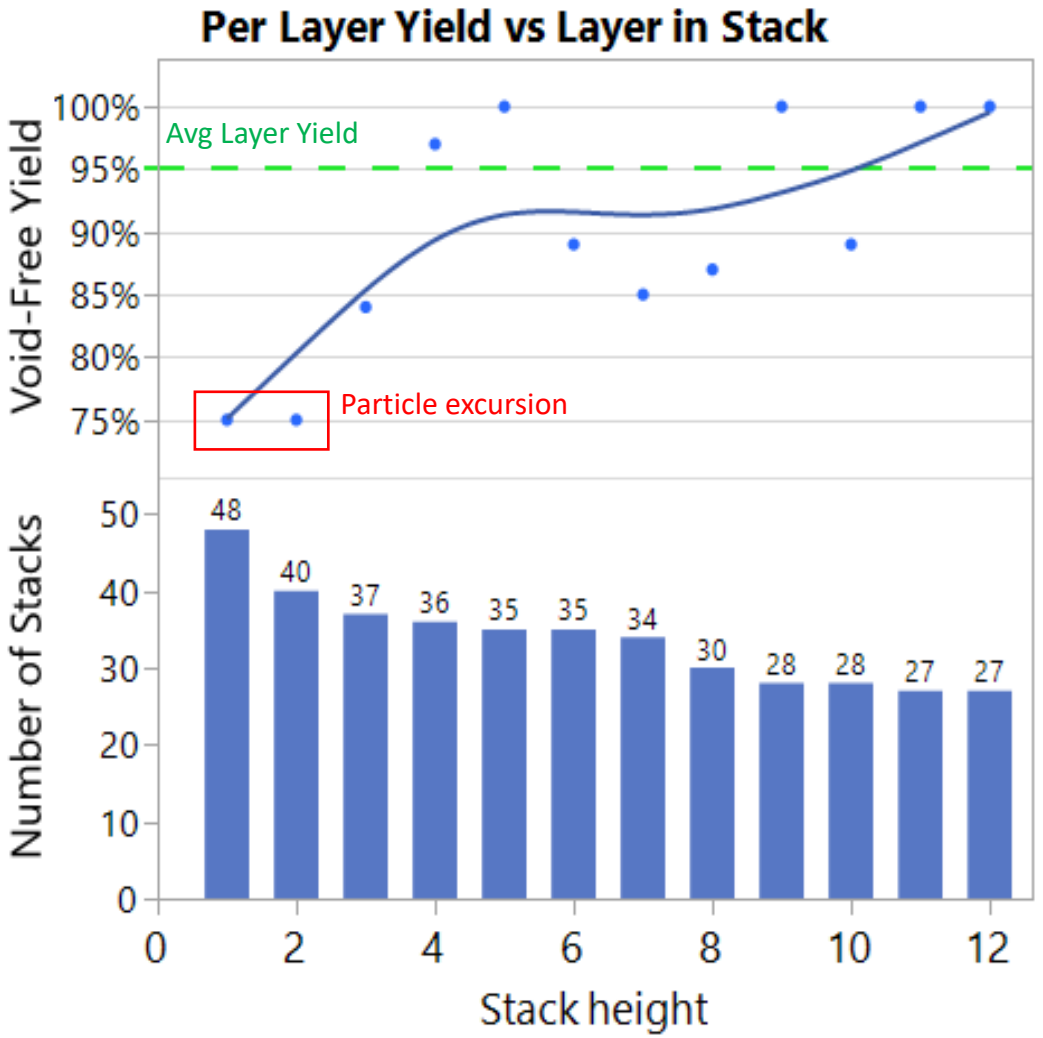
Stacking Test Vehicle

- 8 x 12 mm x 50 μm thick die with 15 μm bond pads



Results

- 12-die stack had overall yield of 56%, with an average per-layer yield of 95%
- After an initial particle contamination excursion, per-layer yield increased as stacking continued and matched the yield for non-stacked devices
- No fundamental limit to the number of stacked layers was found up to 12 layers



Minimum Anneal Temperature (Thermal Budget)

Test Vehicle

- 8 x 12 mm x 200 μm thick Die with 10 μm bond pads

Process Flow

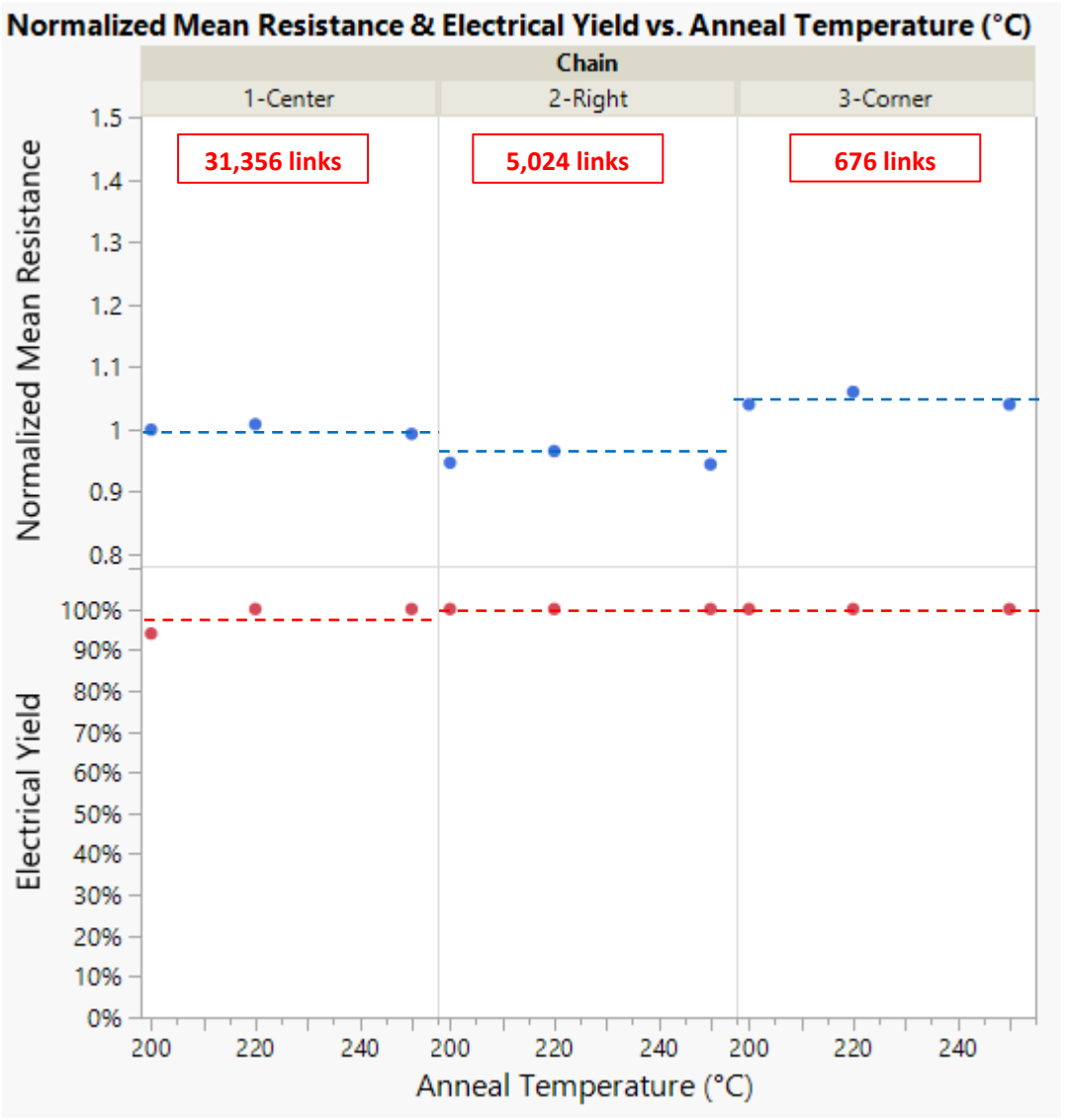
- Bonded wafer cleaved into several pieces
- Each piece annealed at set temperature for 2 hours
- E-test small, medium, and large (Main Center) arrays

Results

- No increase in resistance down to 200°C, indicating a fully bonded interface.
- No drop in electrical yield down to 200°C

Next steps

- Explore anneal temperatures below 200°C



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Hybrid Bond Interconnect Reliability Performance

	Single layer DBI		5-die TSV stacked DBI	
Test	Test condition	Results	Test condition	Results
Temperature cycling	-40°C to 150°C 2000 cycles	**Pass**	-40°C to 125°C 2000 cycles	**Pass**
High temperature storage	225°C, 2000 hrs 275°C, 2000 hrs	**Pass**	150°C, 2000hr	**Pass**
Autoclave	121°C, 100% RH, 15 psi, 168 hrs	**Pass**	121°C, 100% RH, 15 psi, 168 hrs	**Pass**
Moisture sensitivity MLS3	24 hr prebake+30°C / 60% RH 192 hrs + 3X reflow	**Pass**	24 hr prebake+30°C / 60% RH 192 hrs + 3X reflow	**Pass**

- Hybrid Bond Interconnect (DBI) is More Reliable than μbump Interconnect:
  - Enhanced Reliability (all-Cu interconnect, no underfill)
  - Enhanced Resistance to Electromigration (all-Cu interconnect)
  - Dielectric Hermeticity protection (<10^{-11} atm-cc/s)

Summary: Demonstrated Range of D2W Hybrid Bonding

- Pad & Pitch Size: 2–15 μm pads demonstrated with equivalent yield across range
  - Bonder Alignment Capability: Need to align pads to within 80% of pad diameter
- Die Size: 0.4 x 0.4 to 26 x 32 mm die bonded successfully and with good yield
  - Yield vs Die Size: Yield drops with die area, caused by a combination of area and edge related defects
- Die Thickness: 50–200 μm thickness demonstrated with no yield drop for thinner die
- Interconnect Layout and Edge Exclusion: Edge exclusion of 50 – 75 μm is sufficient to prevent edge-related yield loss for single layer bonding, more may be required for stacked die (~200 μm)
- Multiple Chips / Die (non-stacked): Demonstrated 3-chip modules with no drop in yield vs. individual bonding
- Die Stacking (# Layers): Demonstrated 12-layer stack with equivalent per-layer yield to non-stacked die and no drop in yield as stack height increases
- Anneal Temperature: Demonstrated as low as 200°C
- Reliability Testing: All tests passed for single layer and 5-die stacks