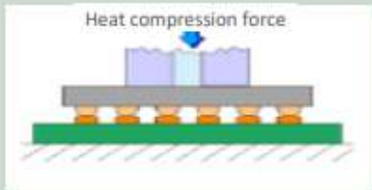
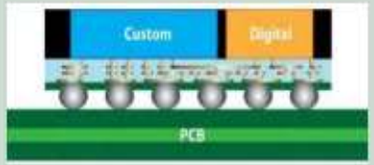
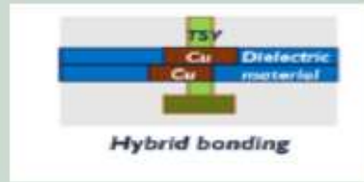
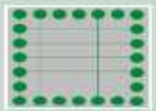
19TH INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
FOUNTAIN HILLS, AZ • WWW.DEVICEPACKAGING.ORG • MARCH 13-16, 2023

Chip to Wafer Hybrid Bonding Development for High Volume Manufacturing

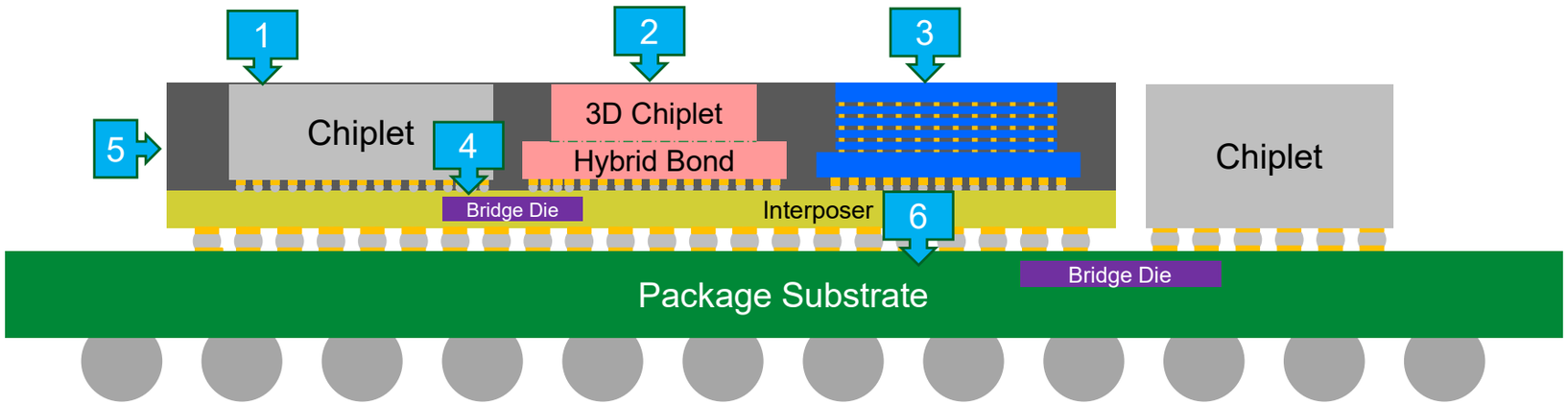
AGENDA

- Introduction
- Chip to Wafer Hybrid Bonding Process Flow
- Characterisation and Electrical Yield
- Die to Wafer Hybrid Bonding
- Conclusion

Hybrid Die Bonding: Next Generation Bonding Technology

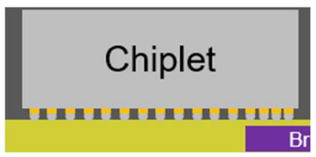
	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Architecture					
Contact Type	 Wire	 Solder ball or copper pillar	 Copper pillar	 RDL or copper pillar	 Copper to copper
Contact Density	 5-10/mm²	 25-400/mm²	 156-625/mm²	 500+/mm²	 10K-1MM/mm²
Substrate	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Accuracy	20-10µm	10-5µm	5-1µm	5-1µm	0.5-0.1µm

New 3D Chiplet Structures Use Variety of Processes



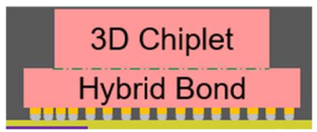
1

Chip to Wafer TCB



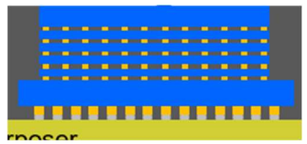
2

Hybrid Bonding



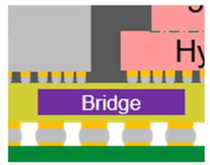
3

High Bandwidth Memory Stacking



4

Embedded Bridge Die Attach

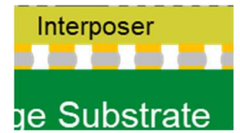


5

Wafer Level Die Molding

6

HD Interposer to Substrate



Besi – Industry leading portfolio

Die Attach

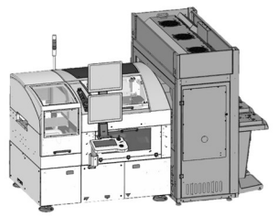
Hybrid Bonding

- 8800 CHAMEO *ultra plus*

Thermo Compression

- 8800 TC *advanced*
  (Substrate)
- 8800 TC *NEXT*
  (Chip to Wafer)

Embedded Bridge Attach



- 8800 FC CHAMEO *Ultra*

Flip-chip

- 8800 CHAMEO *advanced / PLP*
- 8800 FC Quantum *adv / sigma*
- 8800 FC Quantum *hs*
- 2100 FC hS

Direct Lid Attach

- DLA
- TGB 2.0

Epoxy / Soft Solder

- 2100 hS
- 2100 hS i
- 2100 sD *advanced i*
- 2100 hS ix
- 2009 SSI
- 2100 SSI
- 2100 DS

Multi-Module Attach

- 2200 evo
- 2200 evo *plus*
- 2200 evo hS
- 2200 evo *advanced*
- 2200 evo hf

Packaging & Plating

Wafer & Panel Molding

FML
- Wafer molding
- Panel molding

Substrate Molding

AMS-LM
- Substrate strip format
- Exposed die

Leadframe Molding

AMS-i
- MEMS
- Sensors

AMS-X
- HD Leadframe
- Power Devices

Singulation

FSL
Substrate strip singulation
Sorting

Trim and Form

FCL-X/P
Leadframe trim & form
Sorting

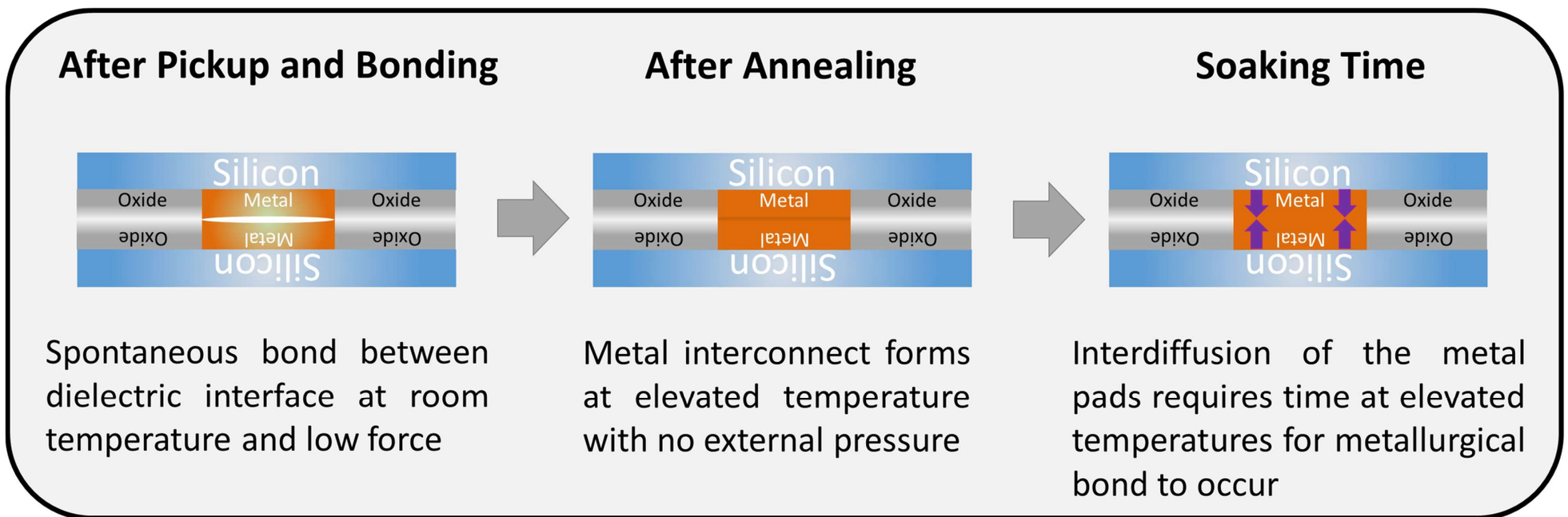
Plating

- Leadframe
- Solar
- Film & Foil
- Chemical Deflash
- Wettable Flank

Hybrid Bonding Basics

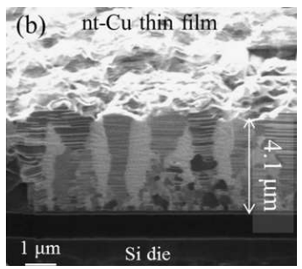
Procedural steps for conventional direct wafer bonding of hydrophilic silicon are:

- Wafer pre-processing — pre-cleaning and removing of specific contamination (particles, organic and ionic contaminants) and/or plasma activation.
- Pre-bonding at **<u>room temperature with low force (up to 15N)</u>** — primary adhesive effects are caused through van der Waals forces and hydrogen bonds. Subsequently, covalent bonds are created.
- Annealing at elevated temperature — from 150°C up to 400°C causes further diffusion of dielectric, strengthening the bond. Copper pads are also expanded resulting in electrical connection.

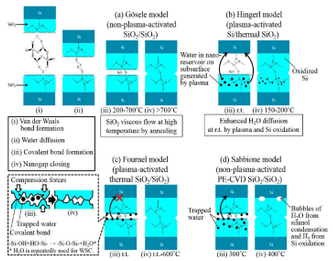


Hybrid Bonding – Many Challenges

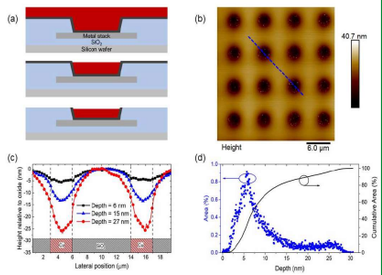
Copper quality and fill



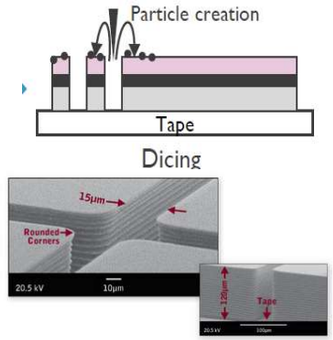
Impact of oxide depostion



CMP and Dishing

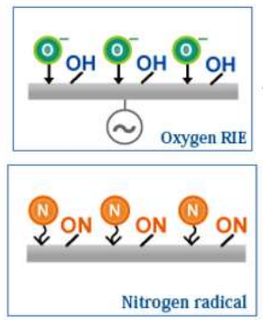


Dicing Cleanliness



Cleaning Parameters

Plasma Activation Parameters



Optimized Bonding Geometry

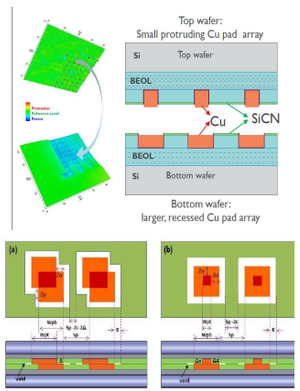
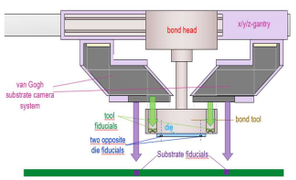


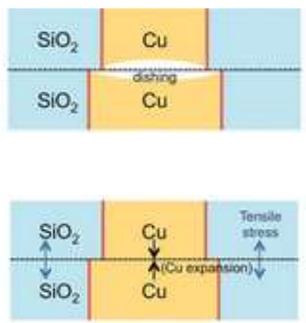
Figure 14. Cu pad design for hybrid wafer bonding; (a) equal pad size layout and (b) unequal pad size layout.

Bonding Process Industrial Solution

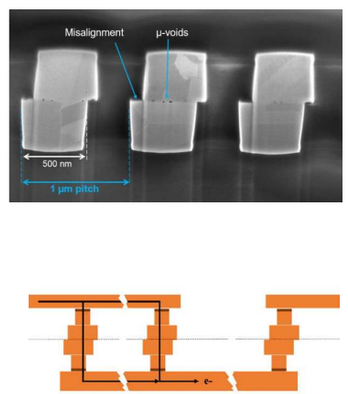


Integrated Process Flow, Low Particles, Inspection

Anneal

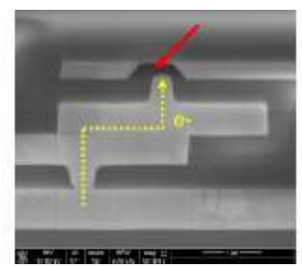


Electrical



Life Time

- Corrosion
- Electromigration
- Thermal Stability

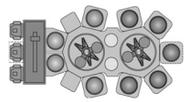


Applied Materials | Broadest Portfolio in Advanced Packaging

Bump FanOut RDL

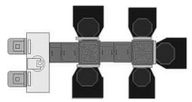
Al Pad / RDL Expose | Develop

Endura
Excecta 2 Al

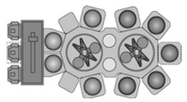


PVD

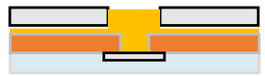
Charger



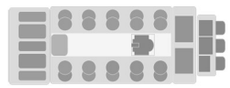
Endura



ECD

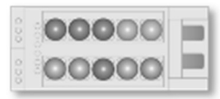


Nokota



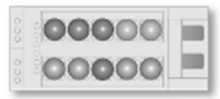
PR Strip

Raider



UBM Etch

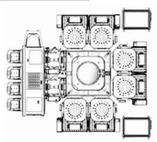
Raider



TSV Formation

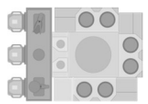
TSV Etch
(Si/FE films)

Centris
Sym3 Via
Sym3X



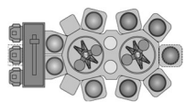
CVD Liner

Producer
InVia 2



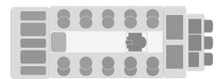
PVD Barrier | Seed

Endura
Ventura



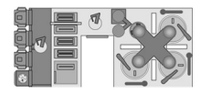
Cu Plating

Nokota
Raider
Mustang



Planarization

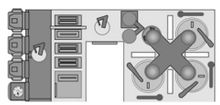
Reflexion LK
LKP



TSV Reveal

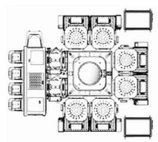
Silicon Polish

Reflexion LK



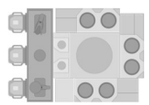
Recess Etch

Centris
Sym3 Via



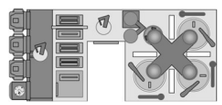
CVD LT Passivation

Producer
Avila



Cu & Oxide Polish

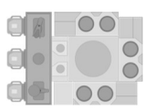
Reflexion LK



Hybrid Bonding

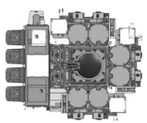
ILD Dep CVD

Producer
Avila / UHP
TEOS

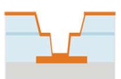


Damascene Etch

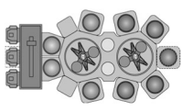
Sym3 GT



Barrier/Seed PVD

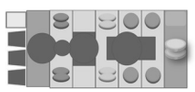


Endura
EnCoRe 2



Cu Pad Fill ECD

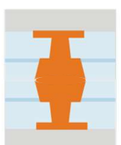
Mustang
Cu ECD



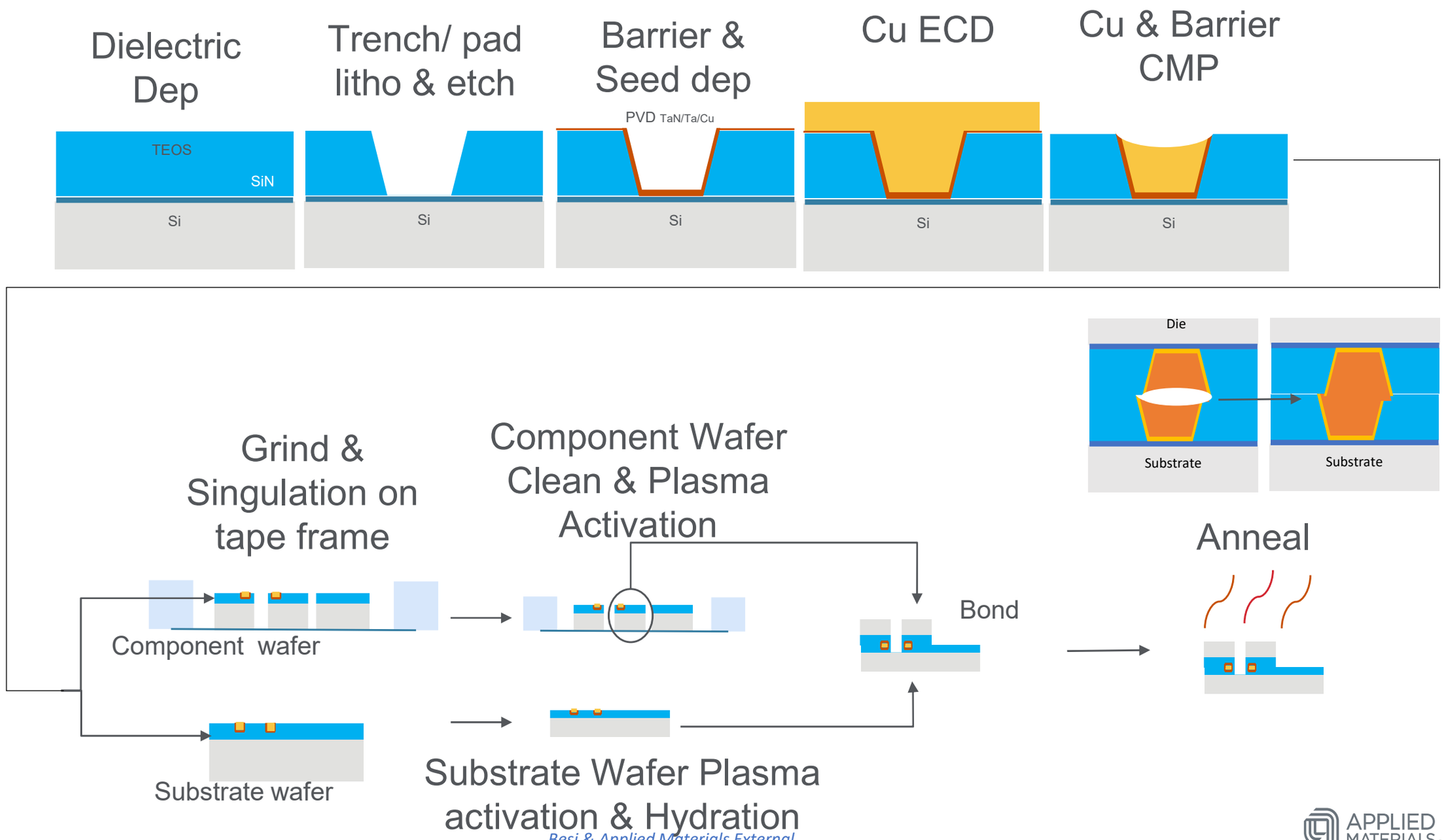
Cu CMP (w/Dishing)

Reflexion LK
LKP

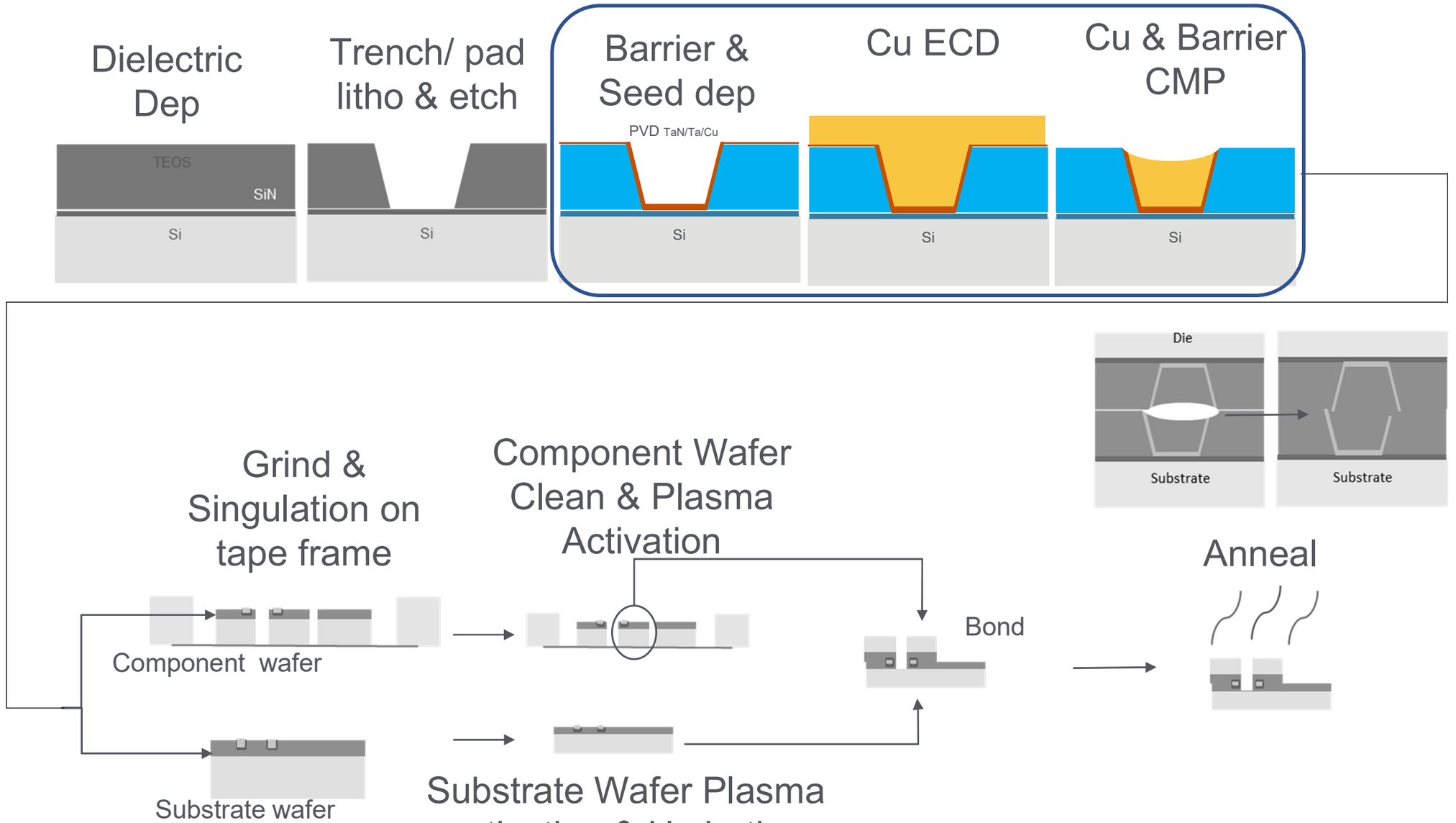
D2W Bonder



C2W Hybrid Bonding Process Flow



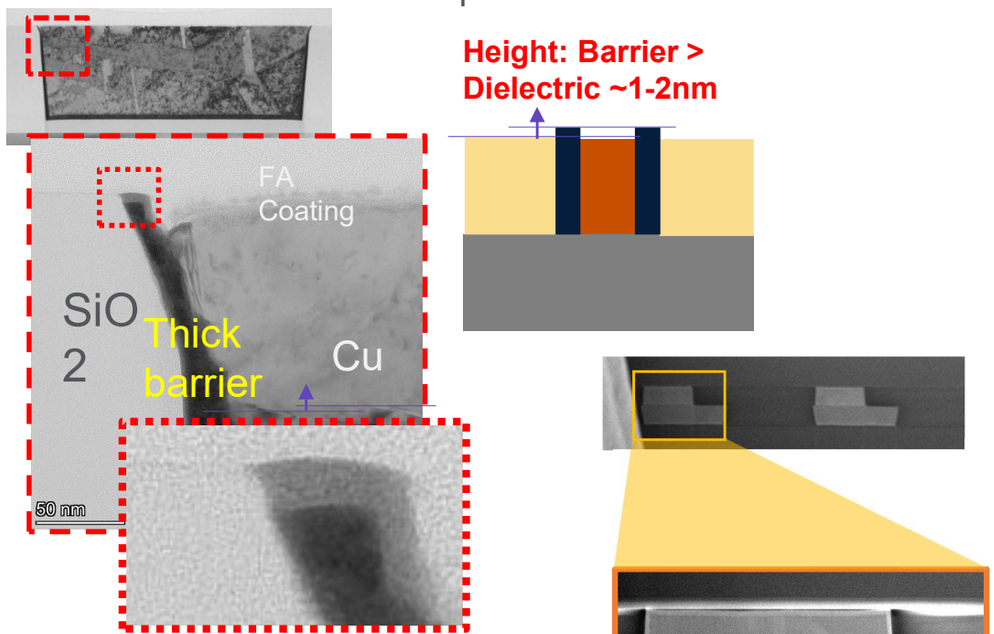
C2W Hybrid Bonding Process Flow



C2W Hybrid Bonding Process Flow - CMP

BEFORE OPTIMISATION

Thick barrier having slightly protruding profile before anneal. After anneal it becomes worse due to higher thermal expansion than oxide

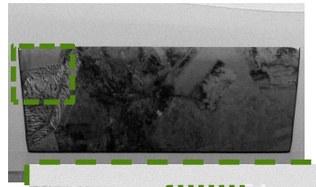


Height: Barrier > Dielectric ~1-2nm

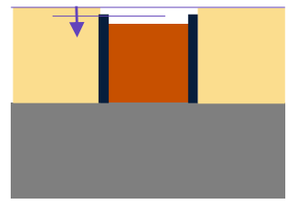
XSEM: showing Cu-Cu bonding gap

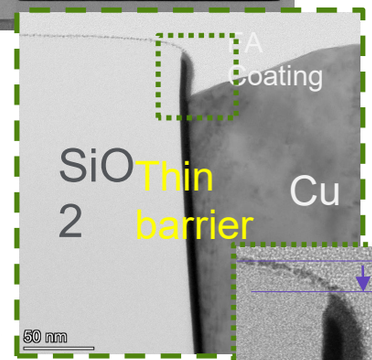
AFTER OPTIMISATION

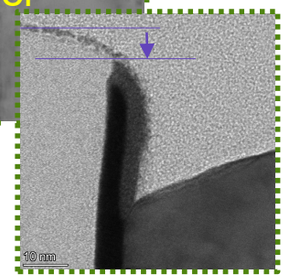
Thinner barrier and optimized CMP ensured barrier height was lower than SiOx profile

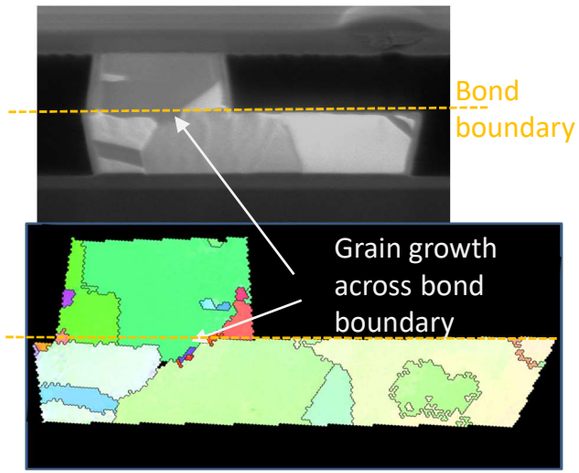


Height: Barrier < Dielectric



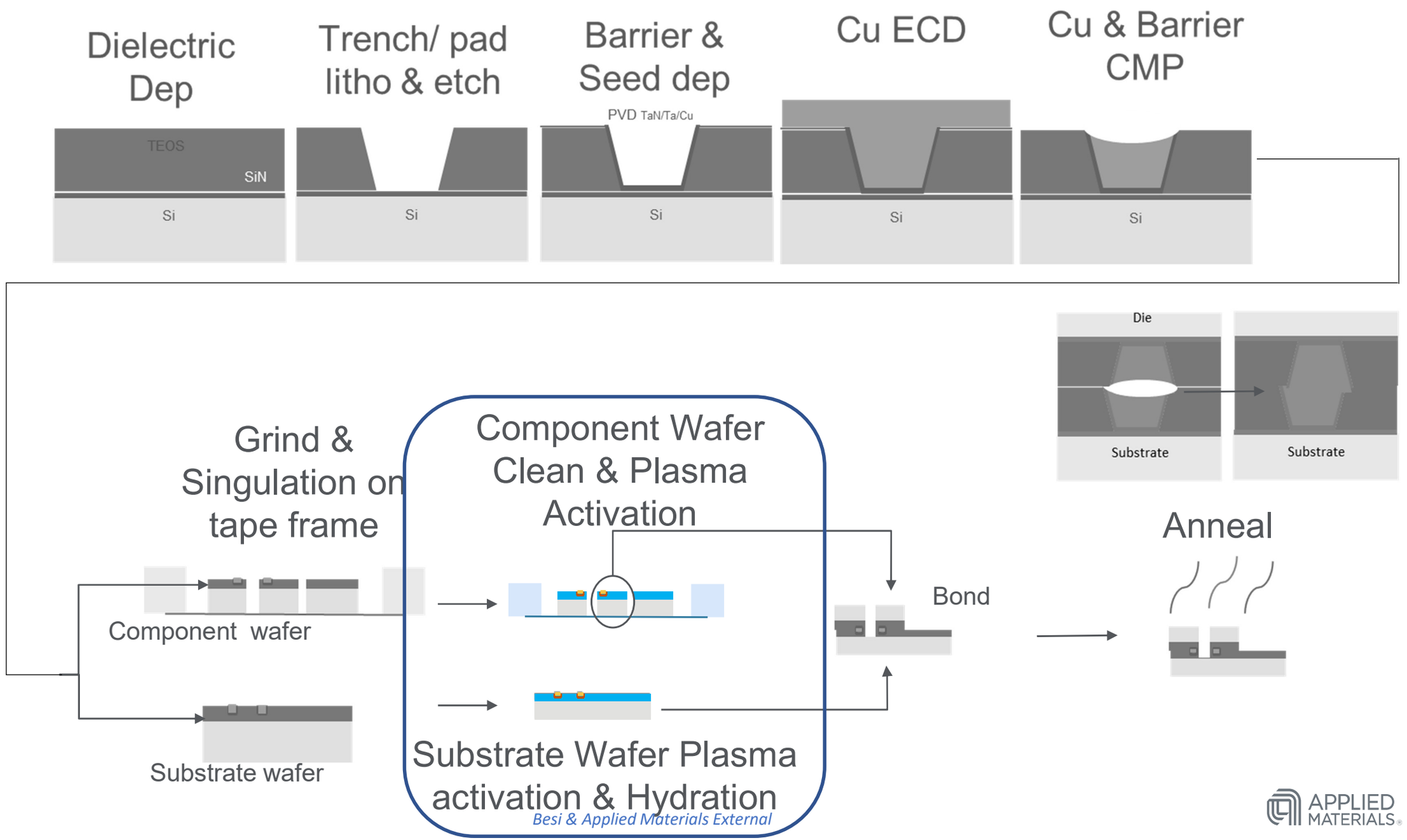






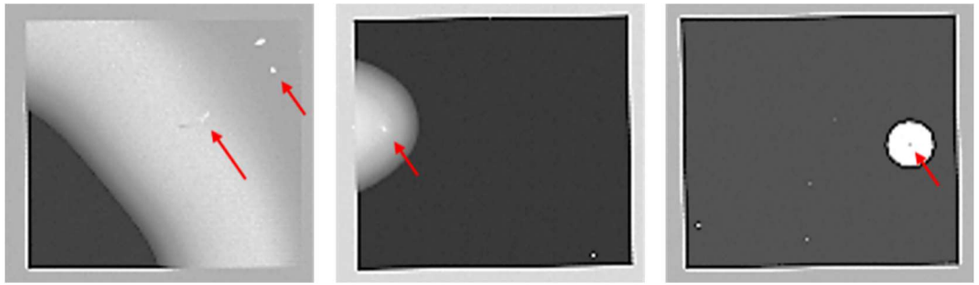
T-EBSD: showing grain continuity across bond interface indicating successful Cu inter-diffusion

C2W Hybrid Bonding Process Flow

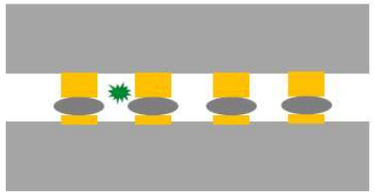


C2W Hybrid Bonding Process Flow - Cleanliness

- Cleanliness is paramount for hybrid bonding. Any particle on the bonding surface can lead to poor adhesion, weak bonds, or complete failure of the bond



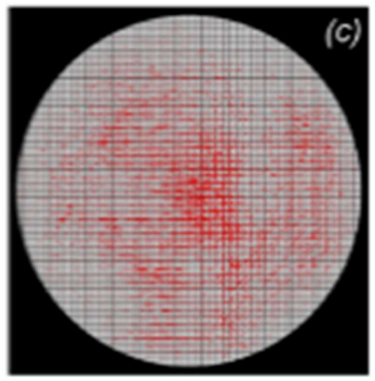
In TCB process, a small particle may have little effect

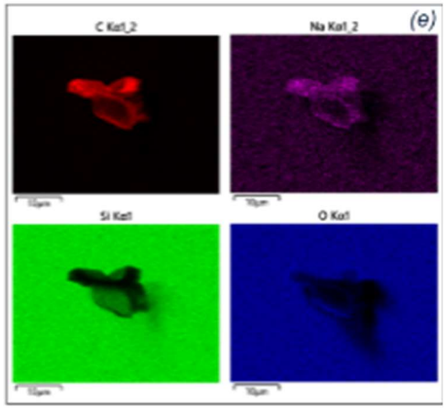


In hybrid process, a small particle may cause an open contact

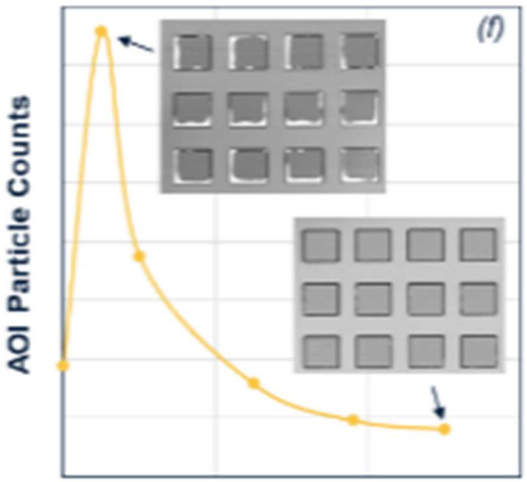
- Challenging for diced wafers on flexible tapes, since the dicing processes could introduce additional particles and/or contaminants.

Insufficient post-dicing cleaning could leave particles on the tape or die sidewalls

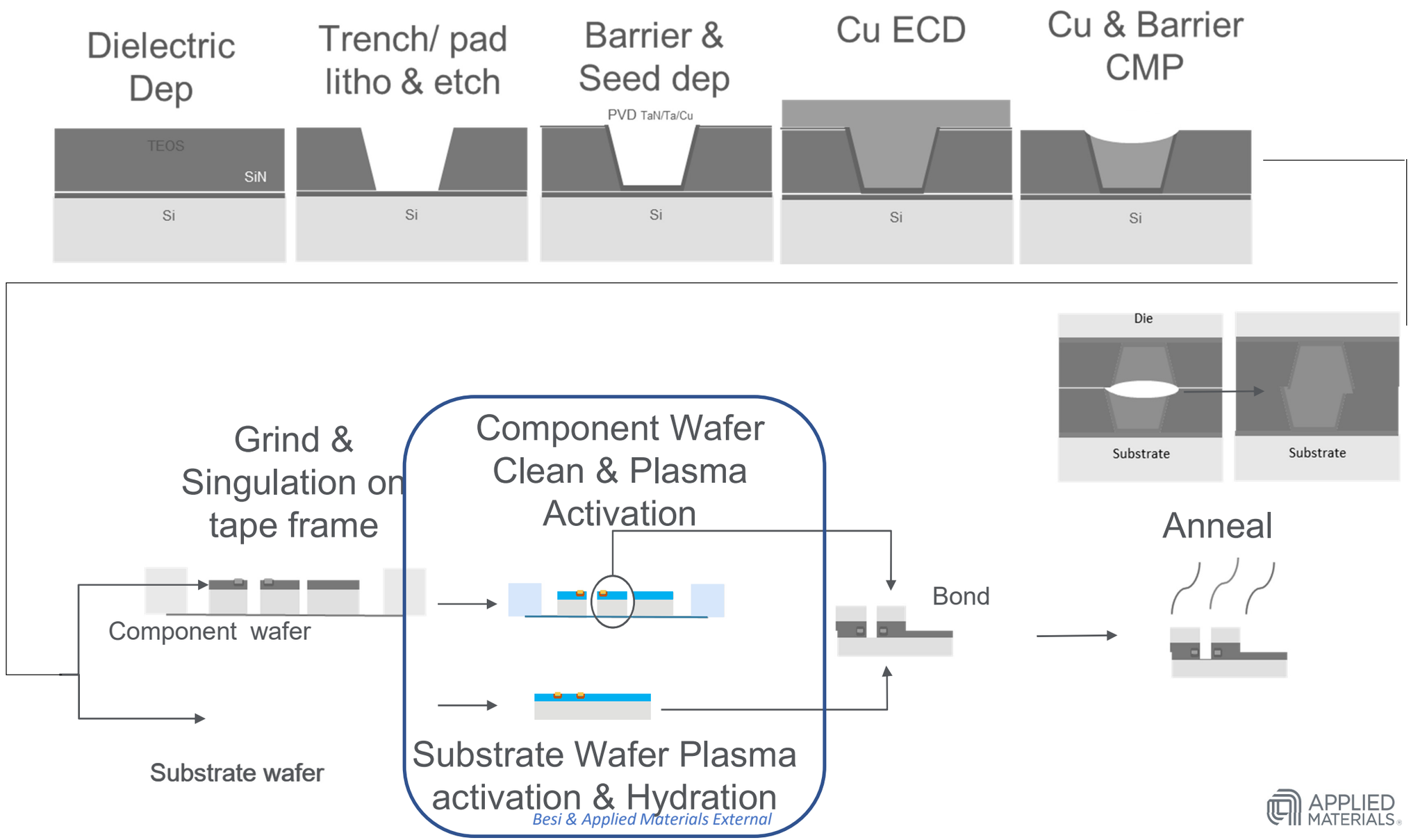




More particles on surface when stirred up from the tape or die sidewalls, causing delamination

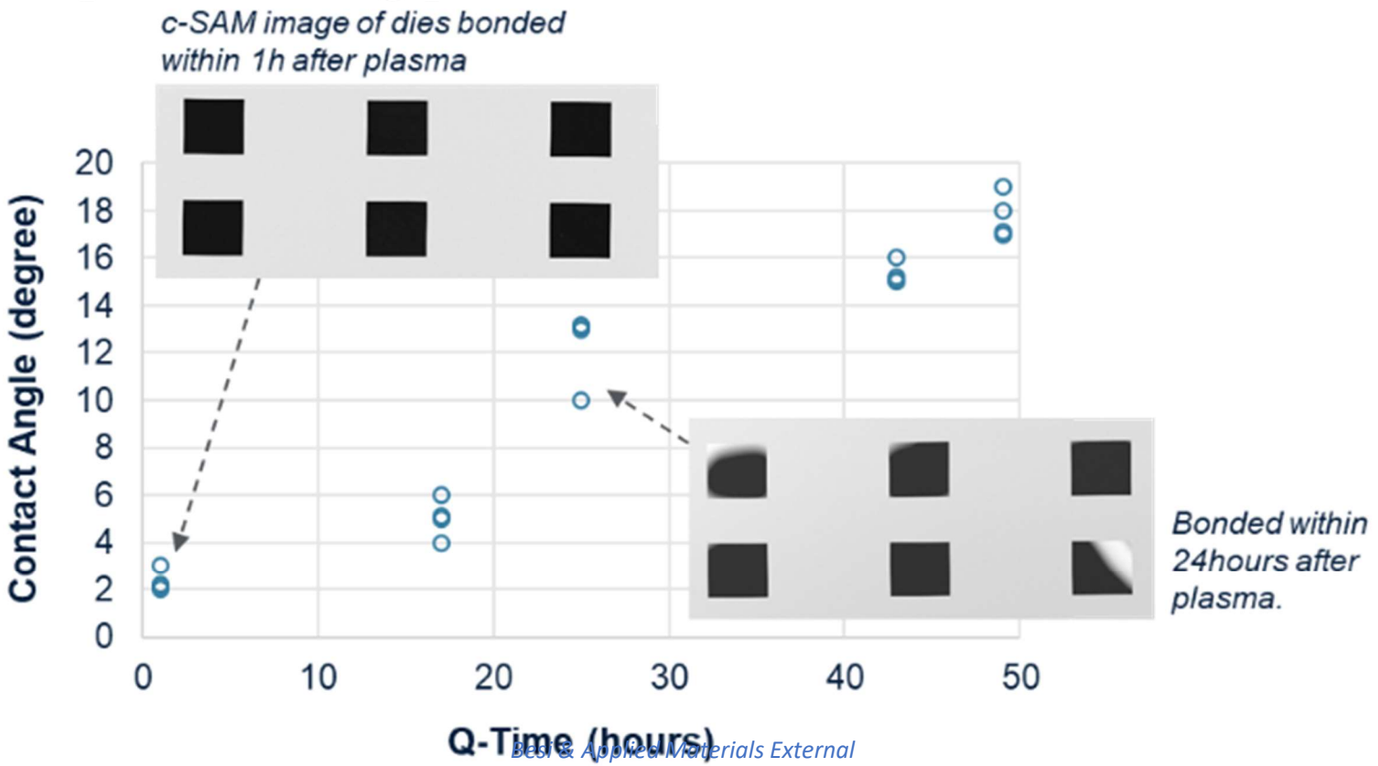


C2W Hybrid Bonding Process Flow



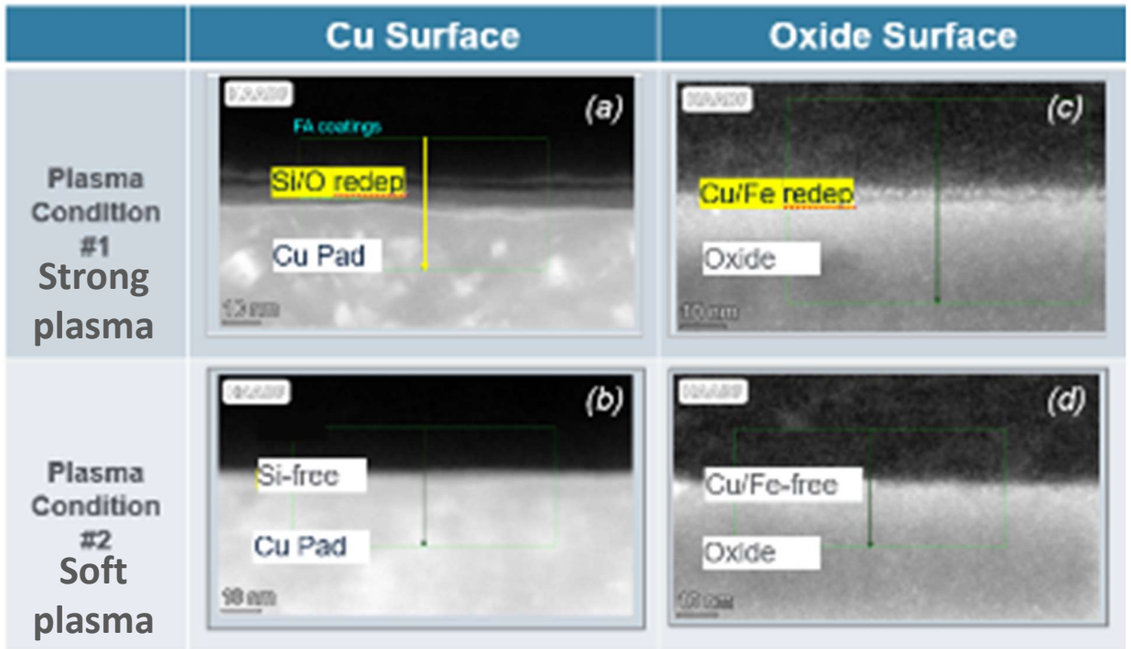
C2W Hybrid Bonding Process Flow - Surface Activation

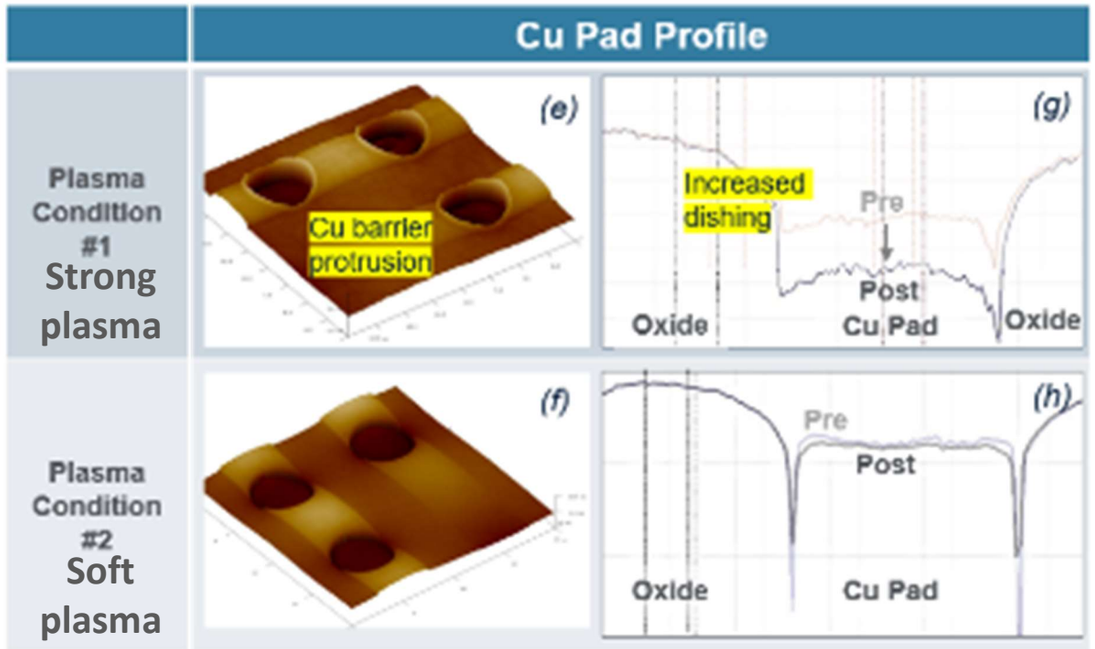
- Plasma activation effect and queue time impact on contact angle on SiO2 surface wrt bonding performance were investigated
- Bonding degrades with excessive queue time between activation and bonding as shown in C-SAM
- In correlation, the contact angle degrades over time if the wafers are exposed to air after activation, leading to poor bonding performance.



C2W Hybrid Bonding Process Flow - Surface Activation

- When the ion energy is too high, the dielectric surfaces are roughened, which creates voids and diminishes the bonding performance.

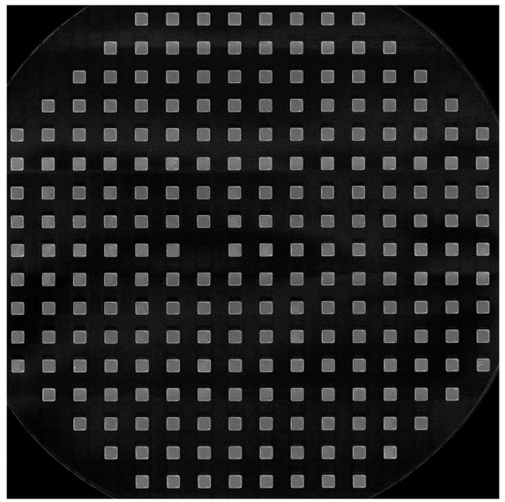




- In addition, the sputtered materials from the dielectric surface and organic adhesive can further redeposit on the die surface
- The redeposition creates an undesired Cu diffusion barrier during the post-bonding annealing stage

- Copper pad profile is impacted resulting in increased dishing
- Ideal plasma should achieve surface roughness of <0.5 nm and etching of SiO2 of <1 nm

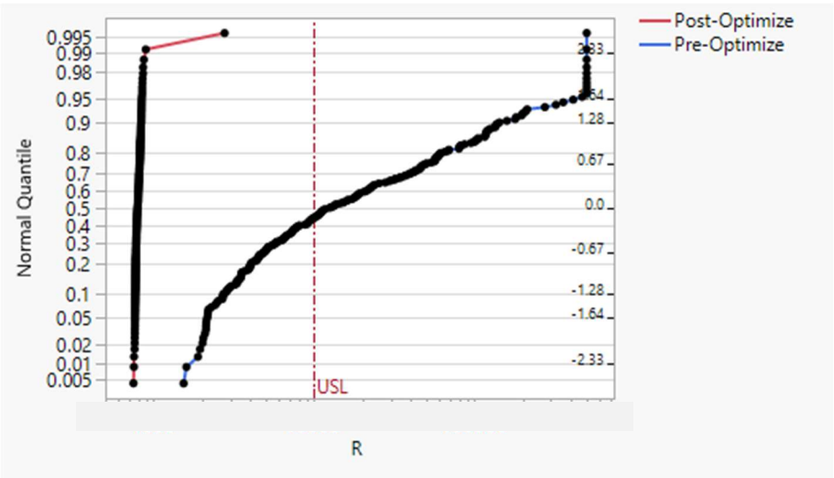
Characterisation and Electrical Yield



cSAM showing no gross random void indicating high cleanliness

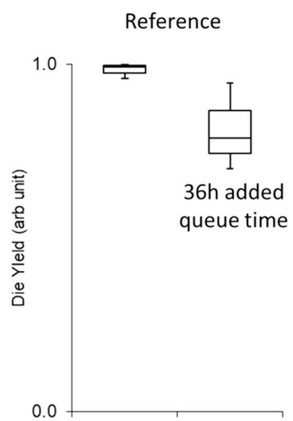
			793	793	828	2764	836	786	782	835				
		800	798	788	826	775	783	768	779	796	831			
	867	783	798	783	846	759	770	778	797	788	840	797		
892	812	777	823	772	810	764	776	785	765	775	800	773	785	
851	820	837	777	824	768	785	762	779	832	764	747	770	778	786	
839	814	812	814	811	763	788	772	798	821	767	753	766	804	776	785
819	815	820	818	802	767	810	771	840	817	767	769	752	804	777	819
836	816	813	820	802	770	836	788	813	814	773	772	761	816	769	829
798	819	797	807	822	776		822	779	778	770	777	773	775	769	838
823	803	812	820	843	806	799	811	801	773	780	778	785	819	767	801
830	815	832	812	804	841	784	815	831	767	784	781	770	789	777	791
847	812	849	818	778	806	777	832	817	765	824	779	770	771	778	780
857	814	839	807	769	831	773	785	778	765	816	772	773	777	780	
	858	824	826	771	830	770	771	774	766	785	782	783	786	791	
		830	805	771	800	780	767	766	783	798	785	800	799		
			837	788	790	791	762	772	770	823	795	804			
				791	801	804	777	787	794	847	807				

Electrical continuity test on a 10k daisy chain (DC) connectivity

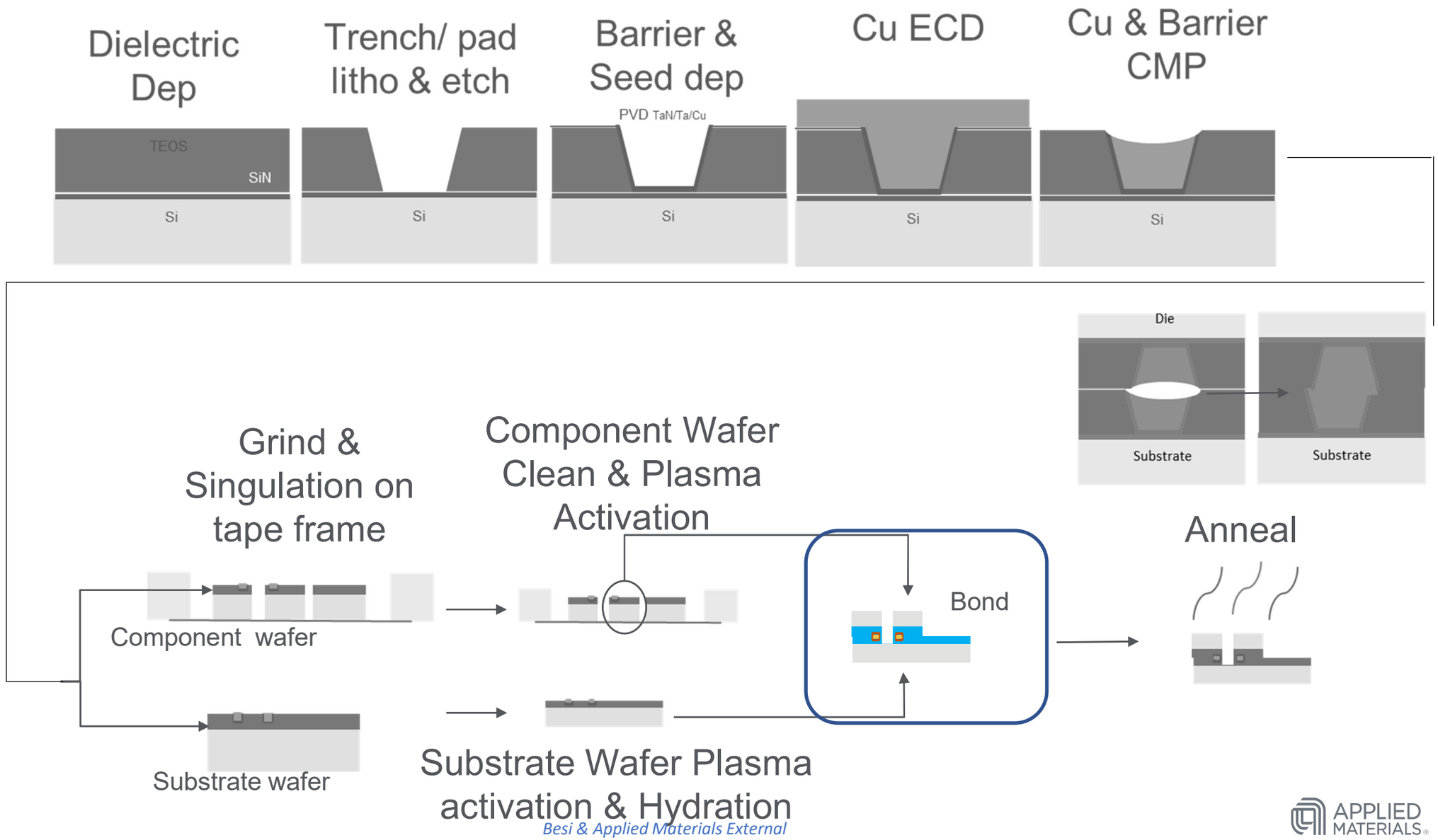


Normal-Quantile plot of 10k connectivity DC showing >99.5% yield (~230-dies)

- Electrical test shows a significant improvement for the post optimized process with >99.5% yield.
- The same test vehicle was used to characterize yield impact of queue time.
- Samples were processed with 36 hours queue time and compared with baseline; in HVM one could expect a queue time of 1 to 2 days bonding configurations with >3-5 different chiplets.
- Three bonded wafers from the "delayed" lot were compared to baseline. Conclusion is that adding queue time leads to significantly lower yield (80%) vs. the reference case (98%).



C2W Hybrid Bonding Process Flow

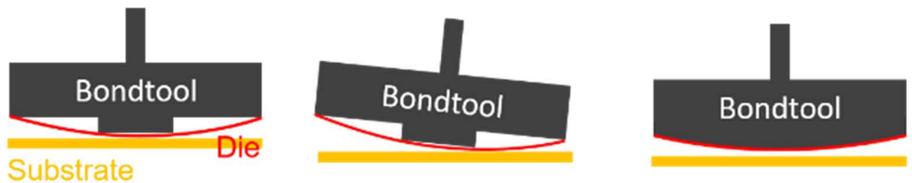


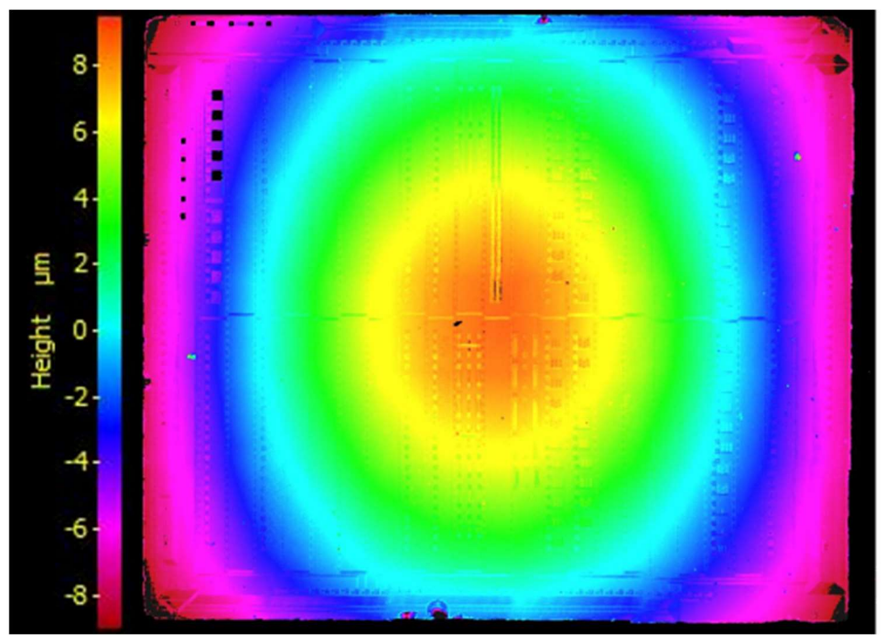
8800 Chameo *Ultra Plus* Chip-to-Wafer Hybrid Bonder

- First high-volume die-to-wafer hybrid bonder
- In production since 2022
- 200 nm placement accuracy
- At high speed of 2000 CPH
- Designed for use in front-end fab environment
- Die pickup from film frame and Silicon/glass carrier
- Integration via collaboration with AMAT
- 100 nm accuracy bonder in development
- Roadmap to <50 nm accuracy

Die to Wafer Bond Front Propagation

- To address the bond front propagation, tooling was developed which enables the die to be shaped in a convex manner, such that the initial point of contact when bonding is at the centre of the die.
- This ensures two things:
  1. The initial contact causes instant bonding through Van der Waals's forces, thereby locking the die laterally and rotationally and minimising placement accuracy loss from possible mechanical influences.
  2. This allows the air between die and substrate wafer to be expelled symmetrically outwards as the die is flattened, thereby ensuring equal conditions on all sides of the die as well as minimising risks of void entrapment.

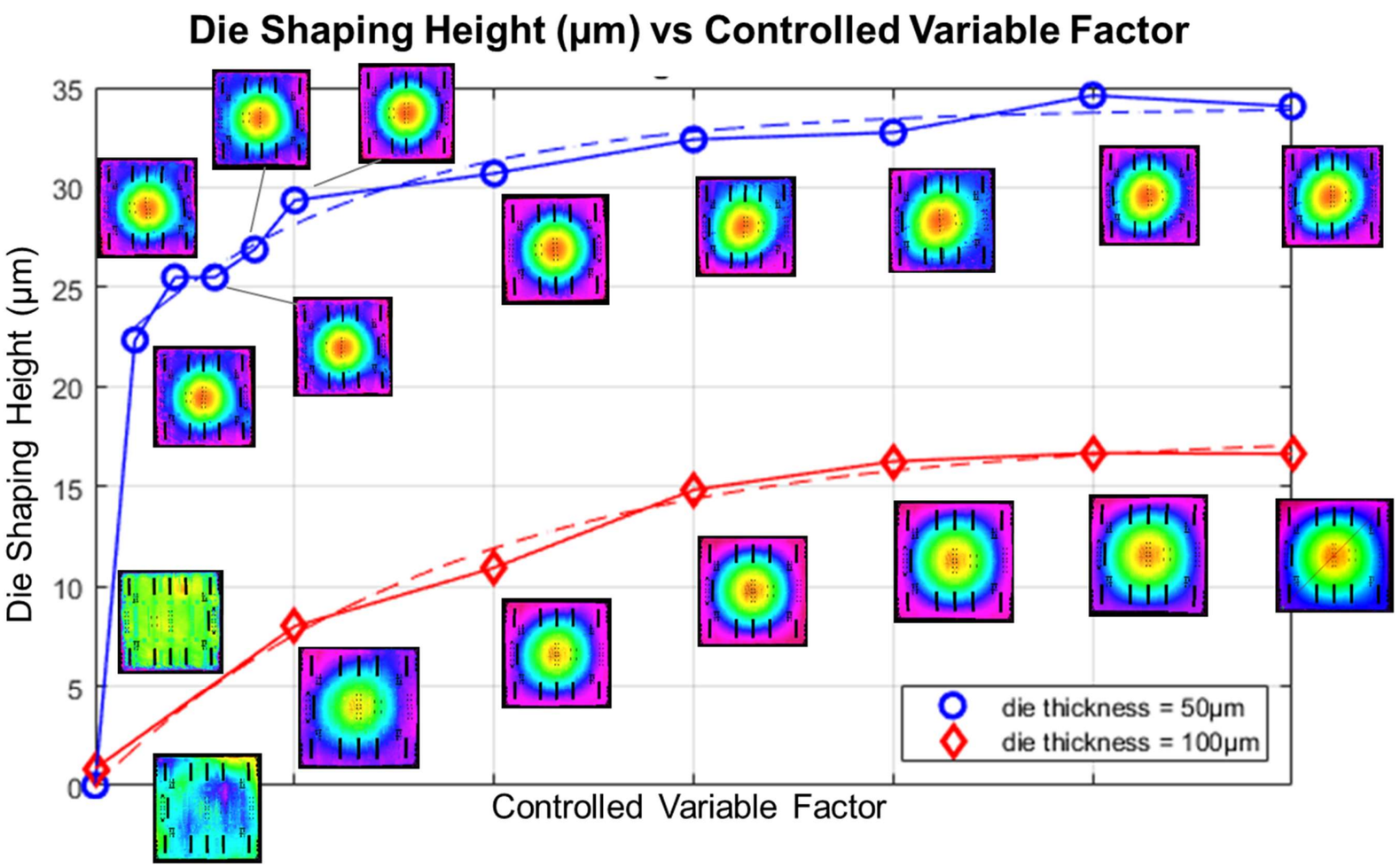




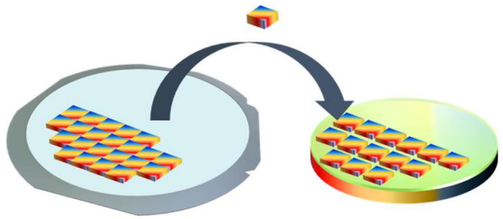
Top View (Pseudo Colour) of Shaped Die

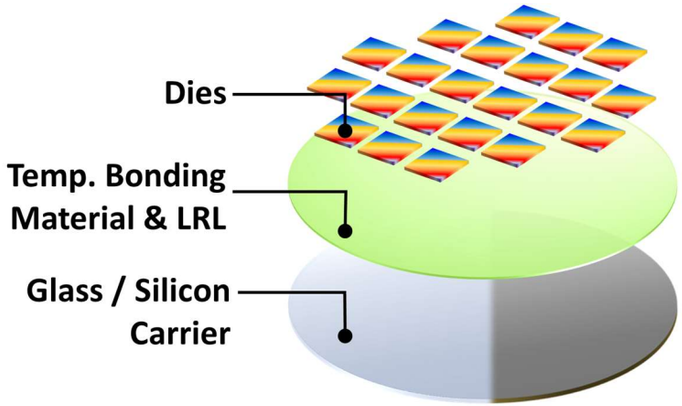
Die Shaping for Bond Front Propagation

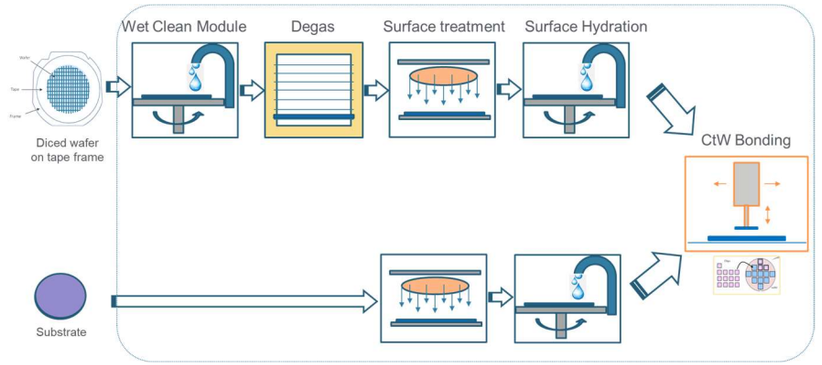
- For the 50µm thick die, **the change in shape occurs at a much lower value** for the controlled variable factor and that **the maximum height is also larger.**
- For the 100µm die, **no deformation for the first 4 values** of the controlled variable factor can be measured.
- **For 100µm, the maximum height is lower than the 50µm thick die**, but both exhibit a similar behaviour whereby the maximum die shape height flattens out.
- At all stages following the initial conditions however, **the first point of contact is always in the centre of the die.**

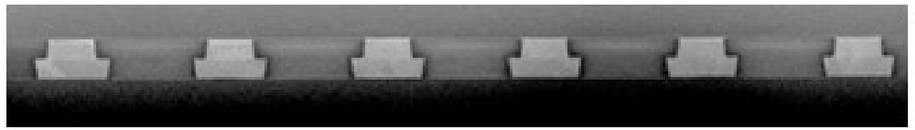


Die-to-Wafer Overlay Results

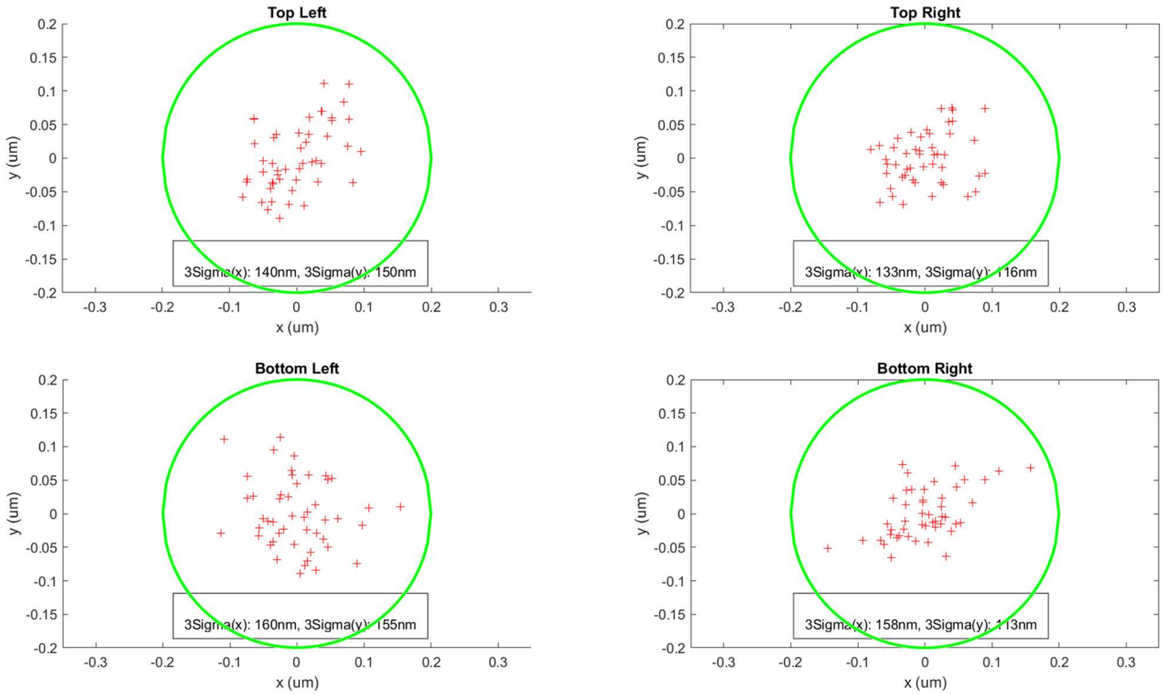




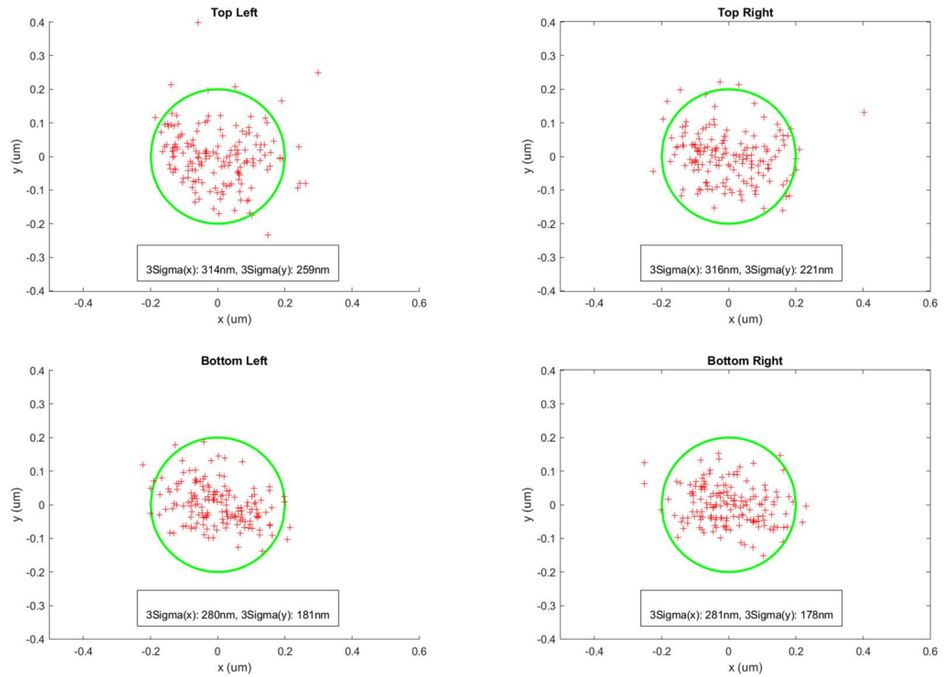




160nm @ 3s worst case corner on TBM



316nm @ 3s worst case corner Cu-Cu Hybrid Bonding



Conclusions

- A working process flow for Die to Wafer Hybrid Bonding has been presented
- Positive outcomes of an HVM-capable process heavily depend on the co-optimization of many pieces of a complex technical jigsaw
- Importance of cleanliness was clearly demonstrated via voids formations arising from particle entrapment
- The bonding dielectric needs to be controlled in terms of surface roughness, and needs to be properly activated without damage.
- Control of queue time along the whole process is critical to guarantee optimal yield.
- Bonding process itself was realized with advanced dynamic die shaping capabilities and a state of the art overlay (160nm @ 3σ).