



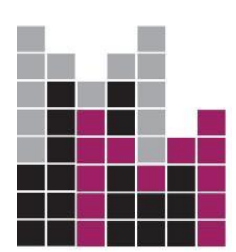
High-yield Fabrication of Thin Glass Interposers

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Mosaic Microsystems, LLC



19TH INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
FOUNTAIN HILLS, AZ • WWW.DEVICEPACKAGING.ORG • MARCH 13-16, 2023



Agenda

- About Glass: types & properties
- Through-glass via (TGV) formation
- Robust handling of thin glass
- Fabricating thin glass interposers
- Conclusion



Glass has excellent properties for interposers

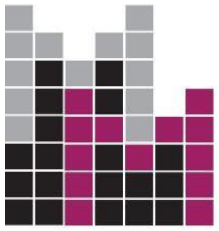
Electrical

Environmental

Physical / Mechanical

Manufacturable

Property	Glass	Silicon	Organic
Low RF loss	Green	Red	Green
High resistivity	Green	Yellow	Green
Mechanical Stability	Green	Green	Yellow
Thermal Stability	Green	Green	Yellow
Thin form factor	Green	Yellow	Yellow
Large area	Green	Yellow	Green
Smooth Surfaces	Green	Green	Yellow
Narrow vias	Green	Green	Yellow
High density interconnect	Green	Green	Yellow



Glass types span a range of properties

Focus here on thin glass of two types:

High purity versions of **FS**

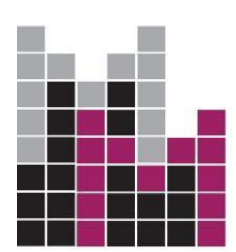
Fused silica → Pure SiO_2

- Excellent RF properties
- Extremely low CTE

ABS

Aluminoborosilicates →
Multicomponent glasses

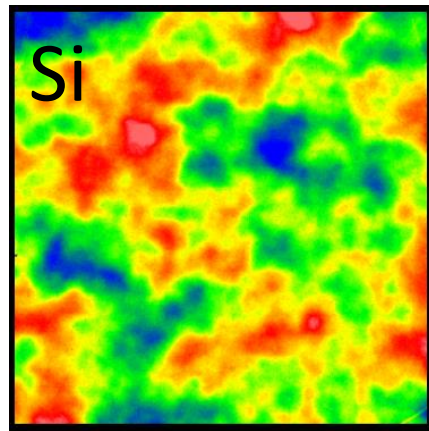
- Lower cost
- Available thin as manufactured
- CTE matched to silicon



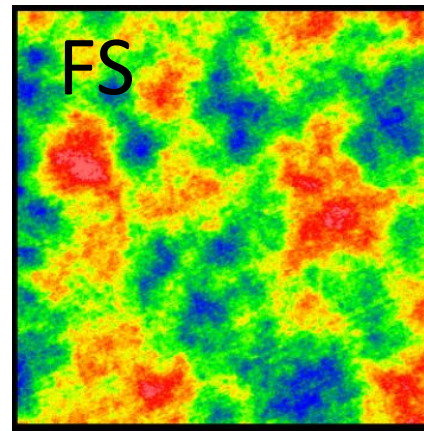
Glass Has Surface Properties Like Silicon

- Surface roughness affects patterning resolution, high- frequency loss
- FS (like Si wafers) are produced by grind + polish
- ABS glass can have comparable smoothness as manufactured (on both sides)

(spatial period < 50um)

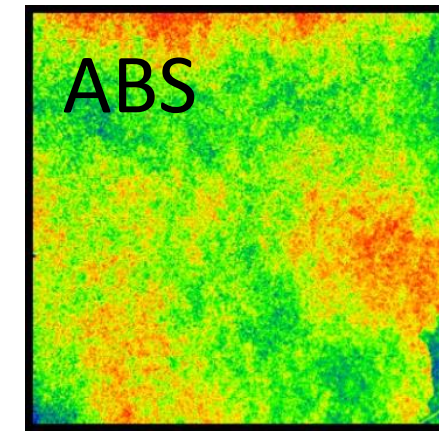


Sq = 0.25nm

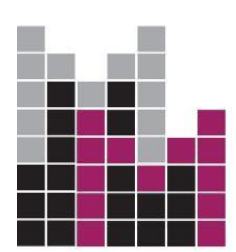


Sq = 0.43nm

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000751



Sq = 0.35nm

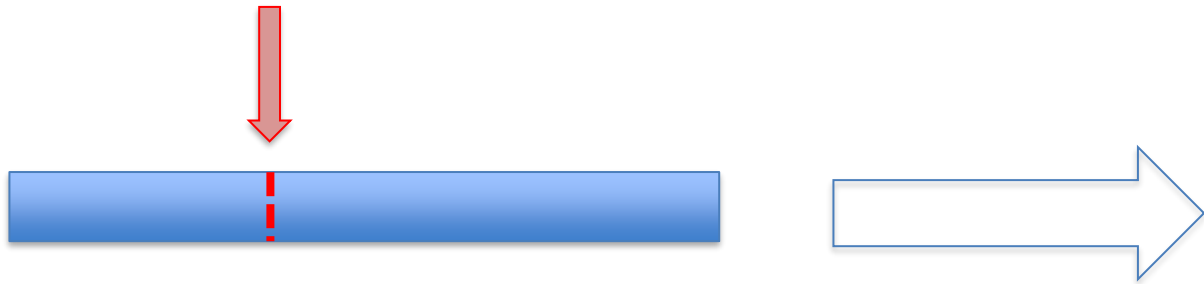


High precision TGVs are formed by laser/wet etch

Laser-damage of glass followed by wet etch

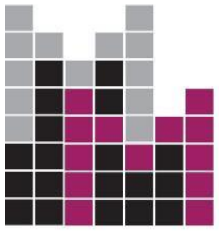
- Highly aligned via position registration
- Allows design of size and shape
- Efficient process

Single laser pulse per via



Batch wet etch for wafers

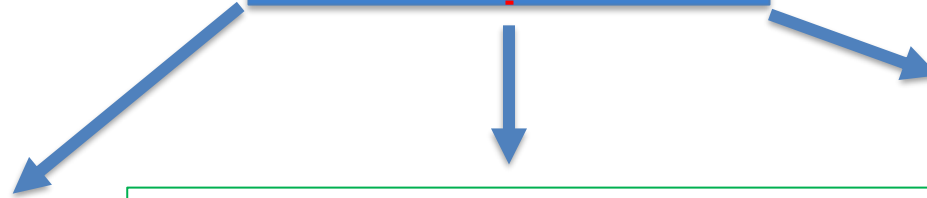
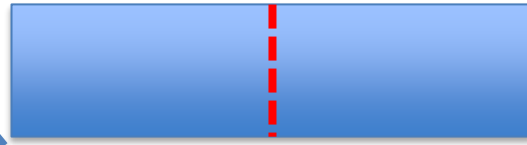




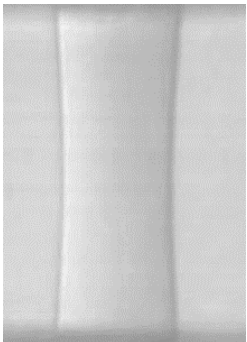
Via shape can be tuned to glass and to application



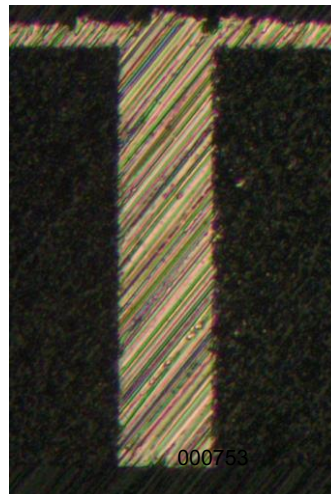
Single laser pulse



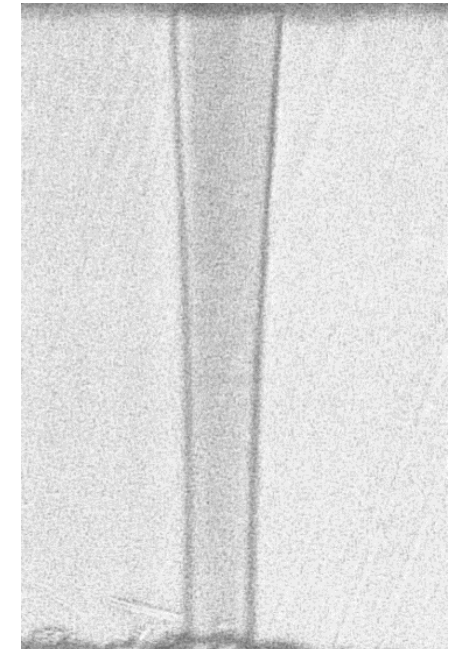
Hourglass via
(100 μ m-thick glass)



Columnar via
(150 μ m-thick glass)

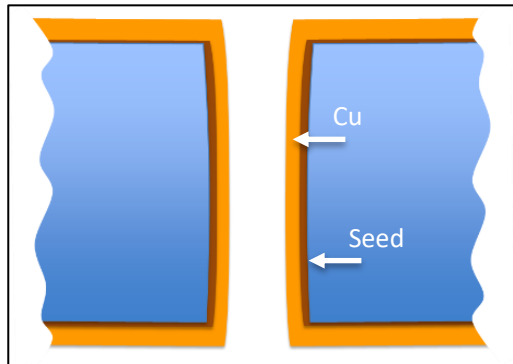
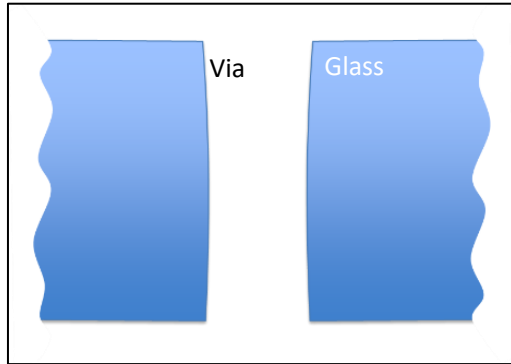


Tapered via
(170 μ m-thick glass)



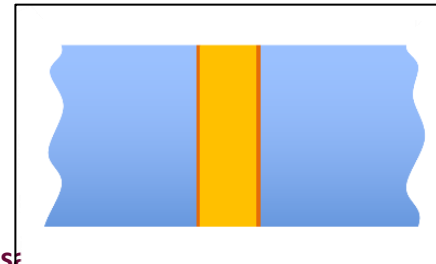
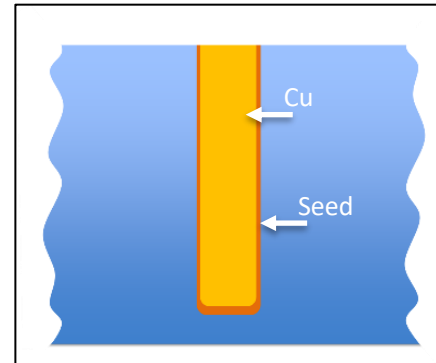
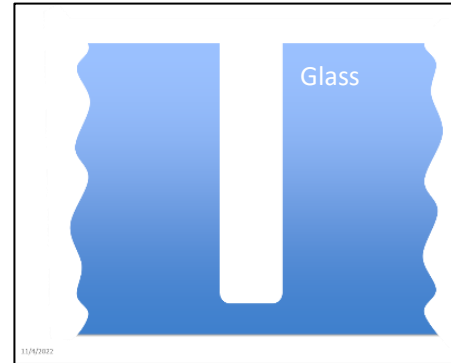
How are vias metallized in thick glass?

Conformal Plate



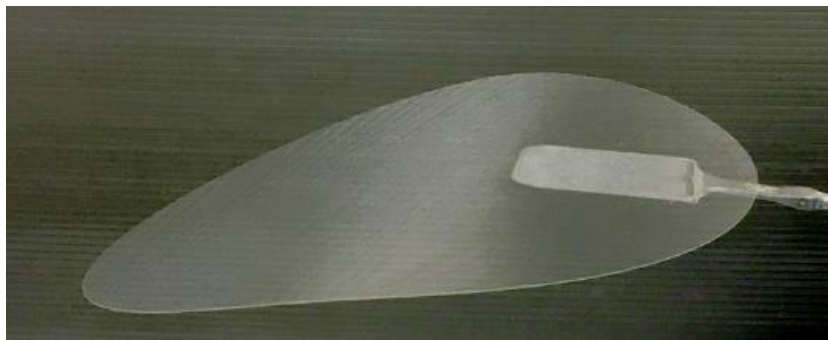
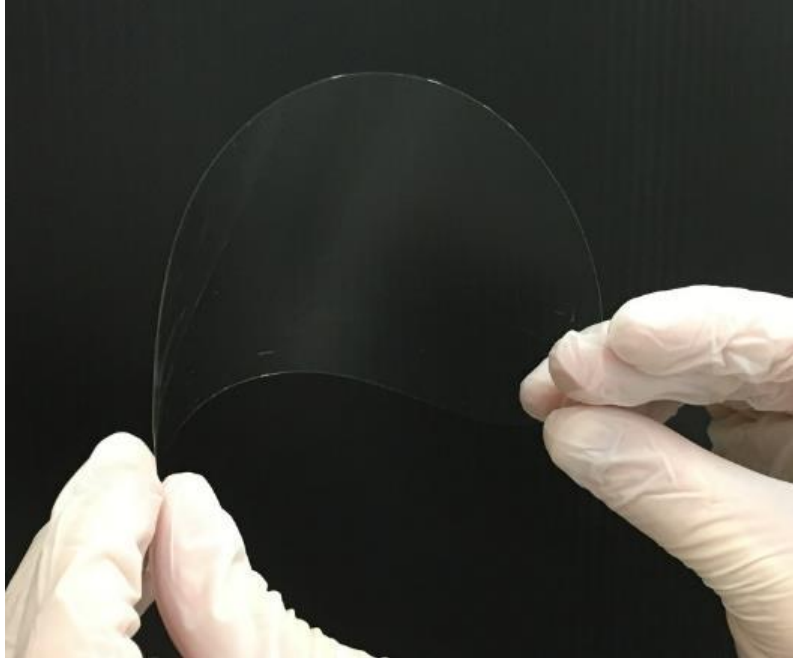
- Plating from both sides
- Thin wafer handling?
- Hermeticity?

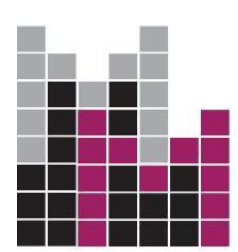
Blind Fill with Backgrind



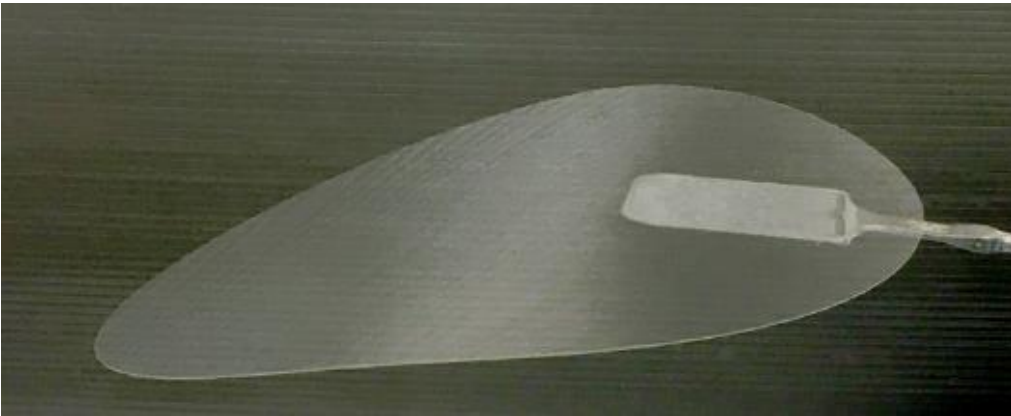
- Starts with thicker glass
- Leverages TSV plating infrastructure
- Good hermeticity
- Requires backgrind

Thin glass presents handling challenges at via-fill and downstream





Temporary bonding creates a robust thin glass wafer handling solution



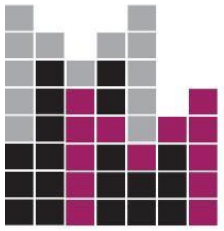
100 μm -thick glass with TGVs



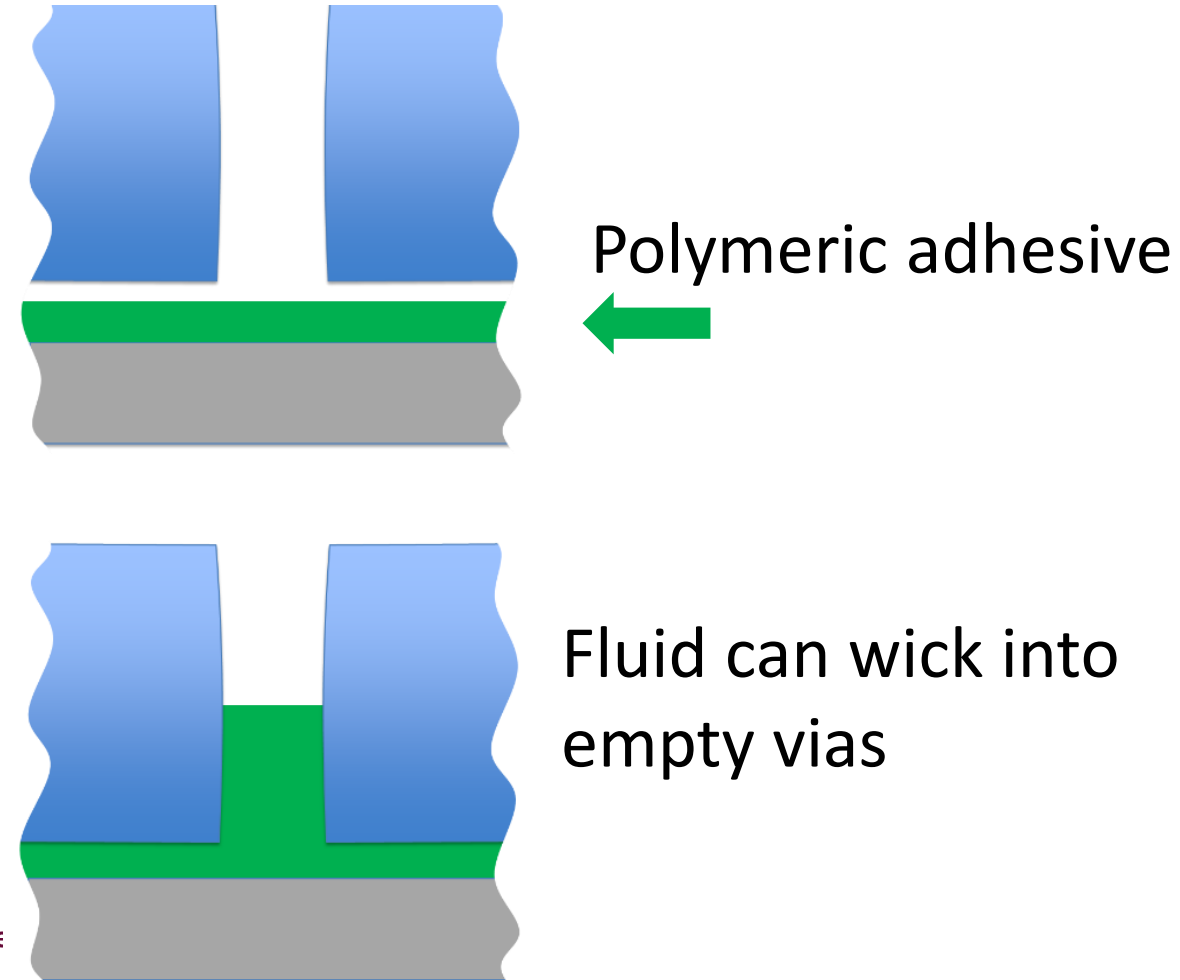
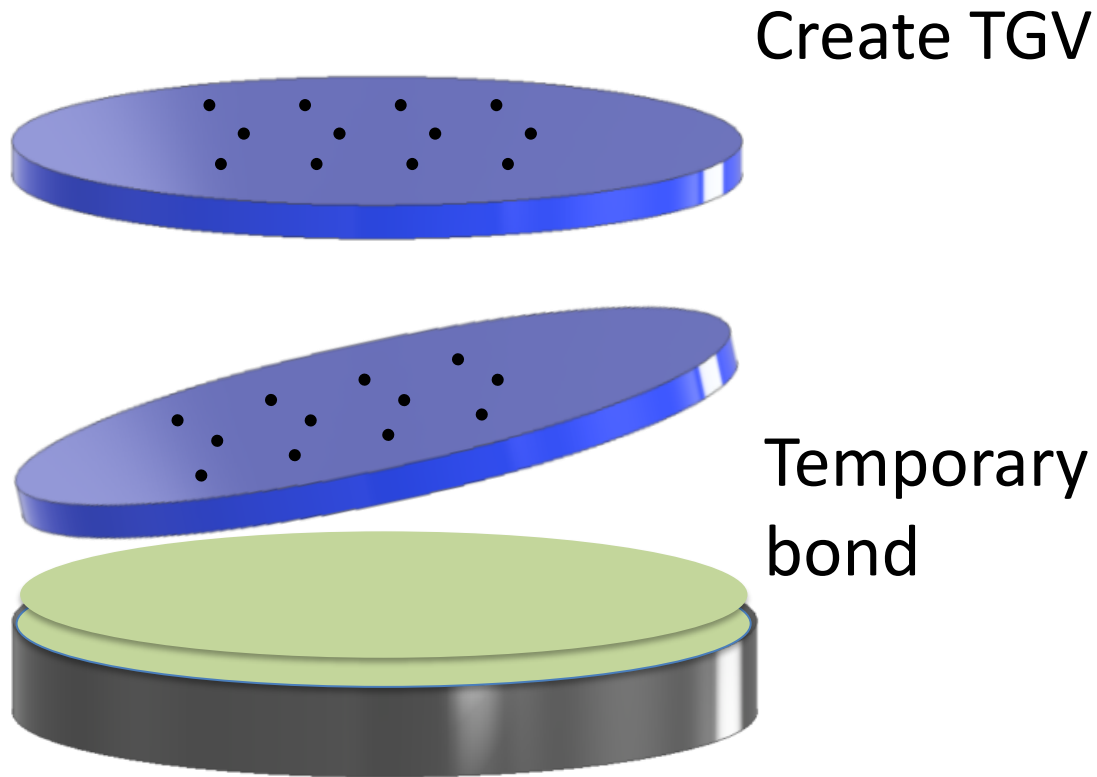
Thin glass temporarily bonded to handle
→ Si or glass handle (as preferred)

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Known solution in packaging industry for thin substrates



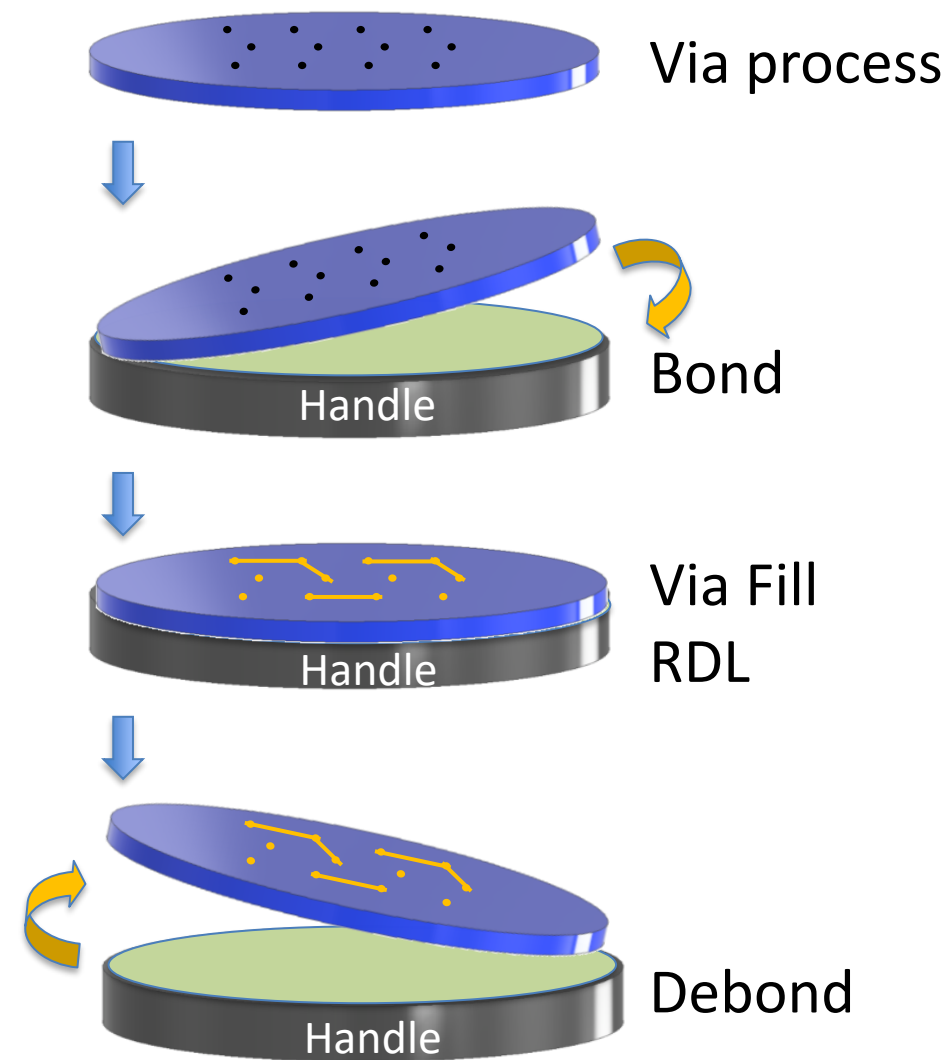
Temporary bond properties can adversely affect TGV metallization





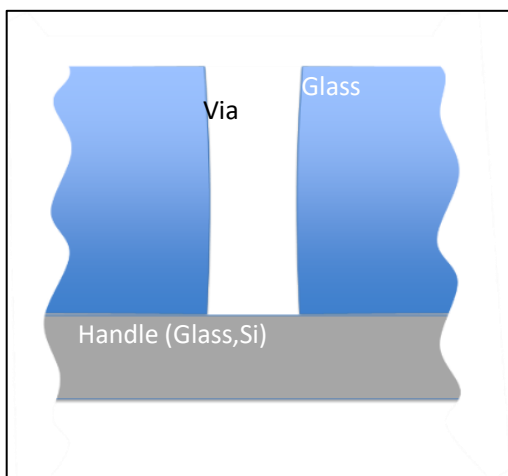
A thin inorganic temporary bond provides a via-fill solution

- Thin adhesion layer → Excellent flatness
- Extreme resistance to processing
- Chemically robust
 - *OK with Acids, Bases, Solvents*
- Thermally robust
 - *OK to 450°C*
- Vacuum-robust
 - *OK with plasma*

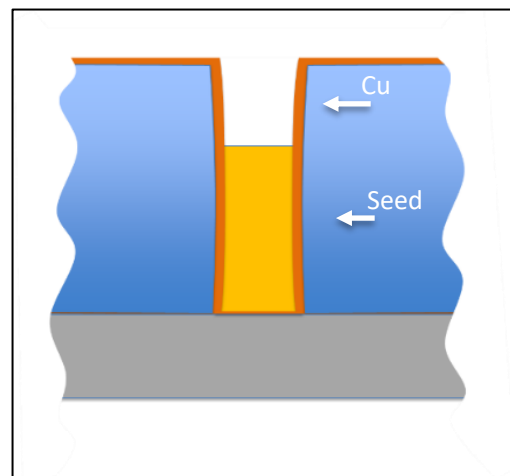




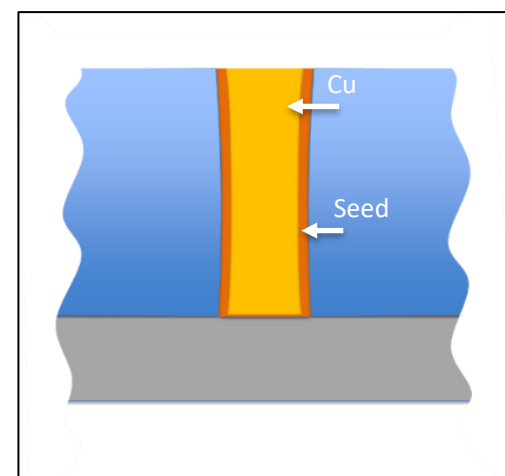
Thin glass “blind” via-fill approach is allowed by inorganic bond



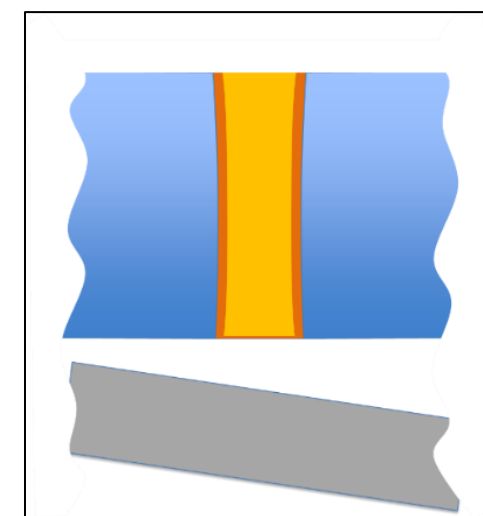
Blind via at bond to handle



Seed and bottom up fill



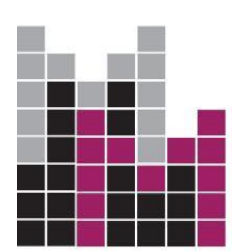
Robust to CMP



Debond reveal

Combines:

- Ease of handling thin glass with high yield
- Compatibility with industry TSV electroplating processes
- Backside reveal without grinding



Different via shapes can be filled with “Bottom Up” chemistry

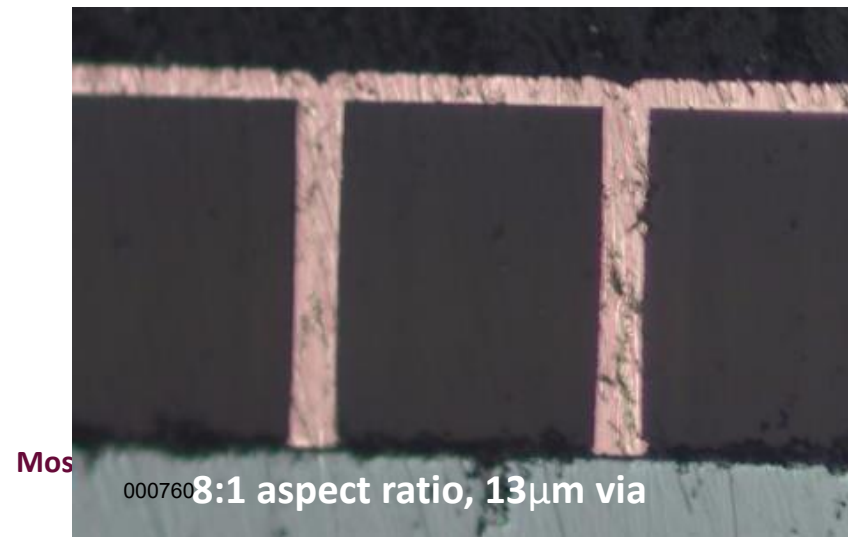
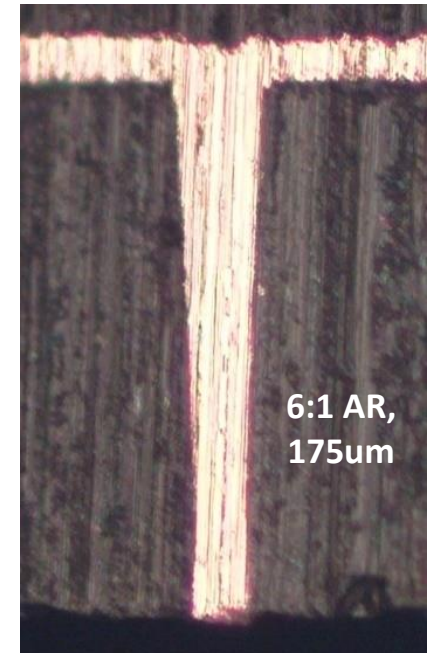
Process optimized across broad range:

- Glass thickness $\sim 70\text{ }\mu\text{m}$ – $200\text{ }\mu\text{m}$
 - 2.5: 1 aspect ratio
 - 8:1 aspect ratio
- Tapered or columnar



30 μm top diameter

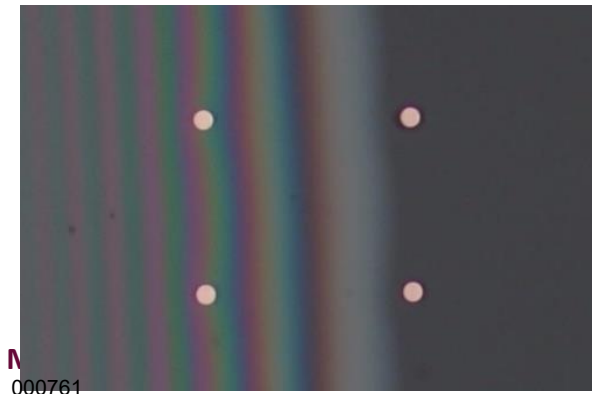
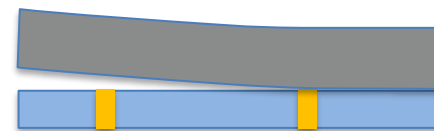
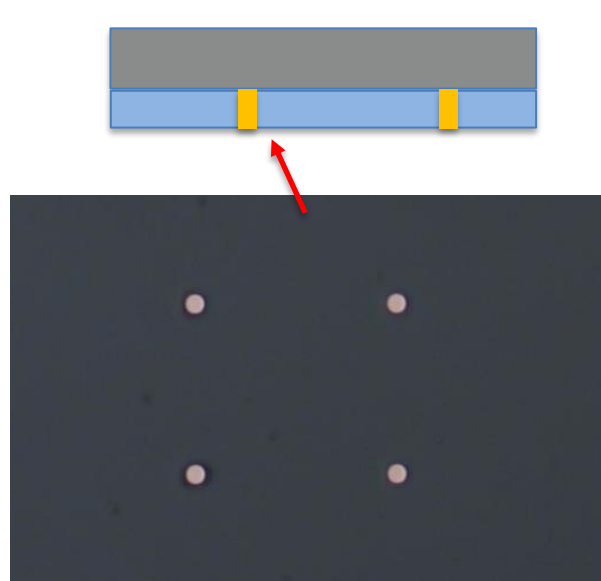
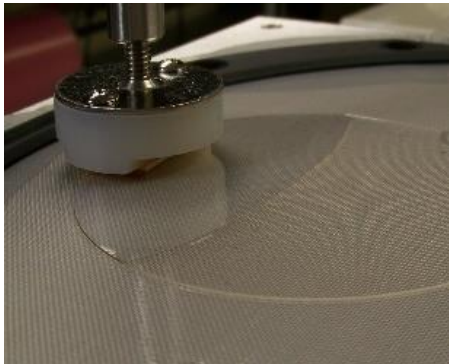
35 μm top diameter



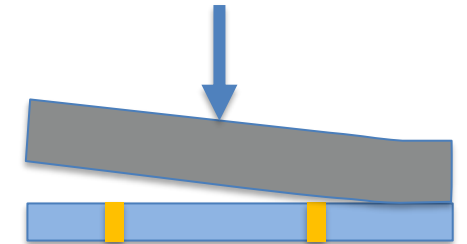
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Mechanical debond protects device wafer

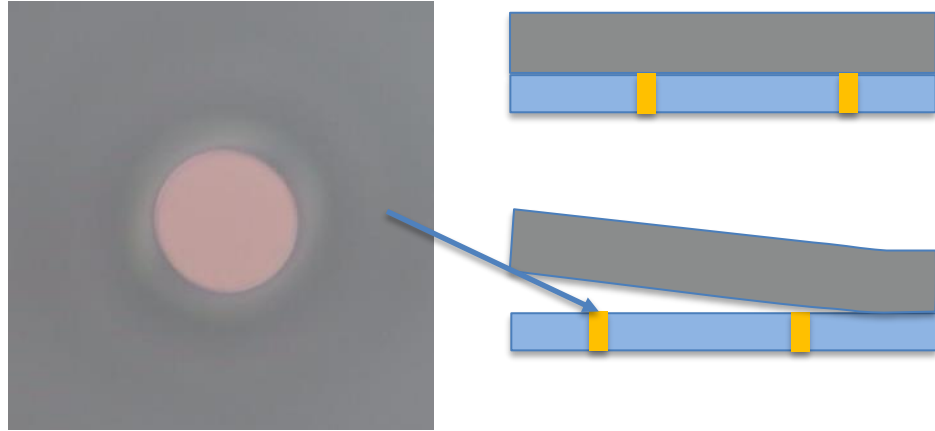
- Handle is pulled away from device
 - Commercial equipment exists for this mechanical debond
- Seed layer engineering
 - *Controls adhesion at via base*
- Filled vias peel off handle → simplified backside reveal!



**Viewed through
glass handle**

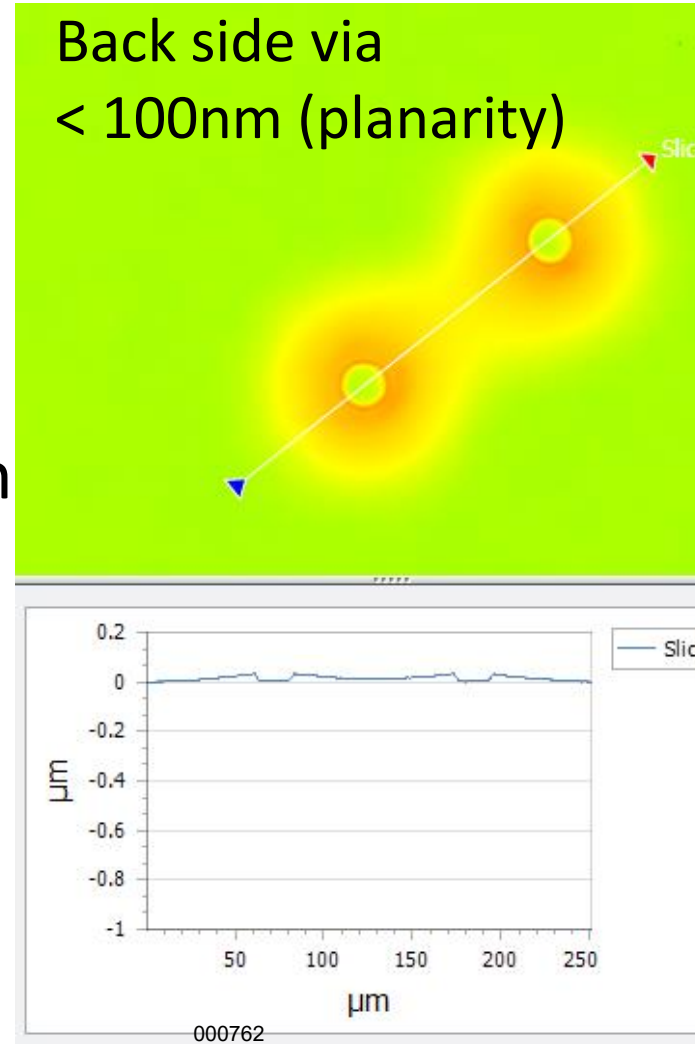


Mechanical debond yields a smooth via surface

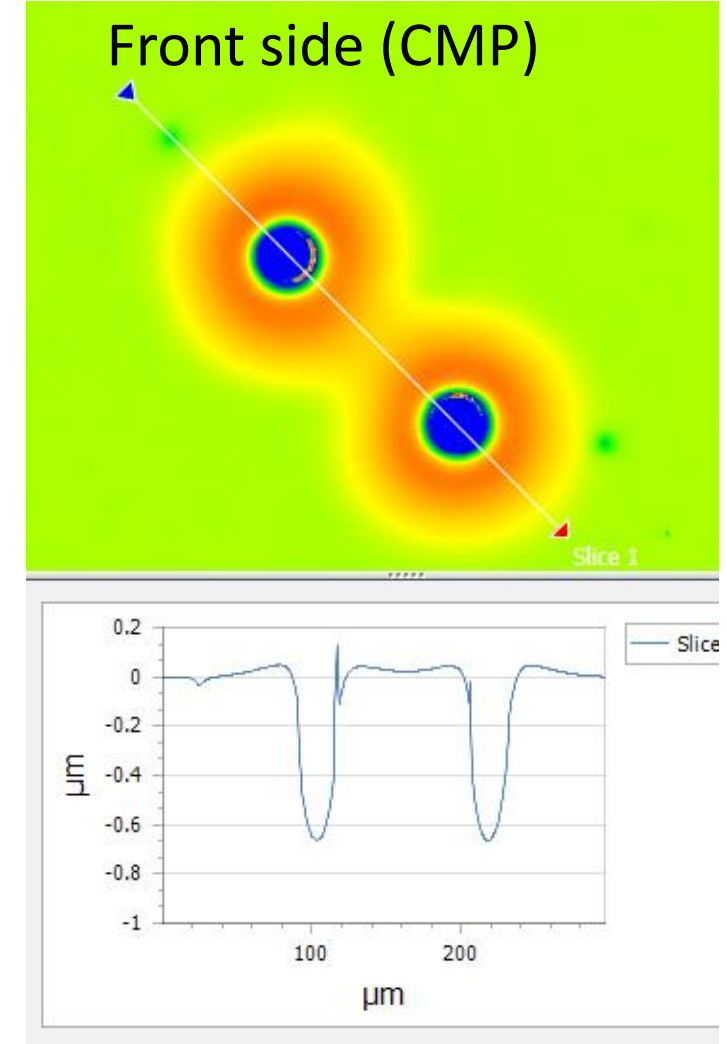


Optical profilometry:

Back side via
< 100nm (planarity)



Front side (CMP)



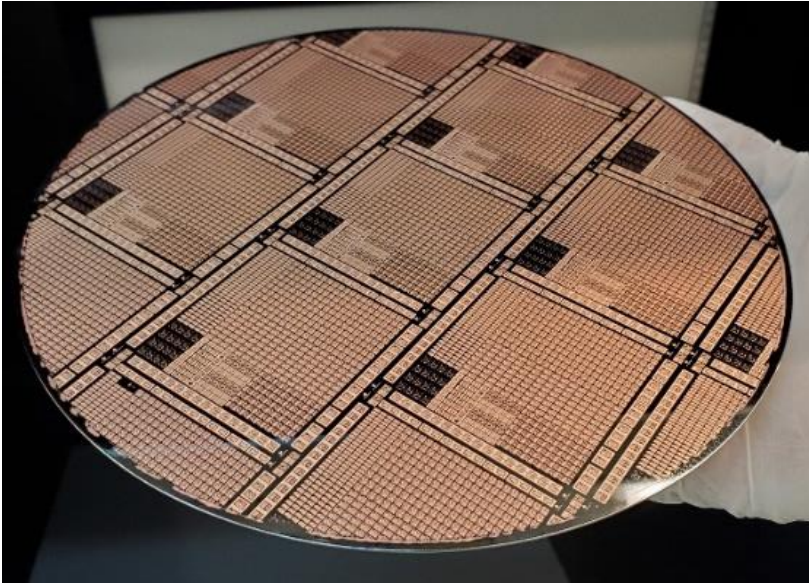
→ smooth surface is obtained with no additional processing

■ No residue (by XPS)

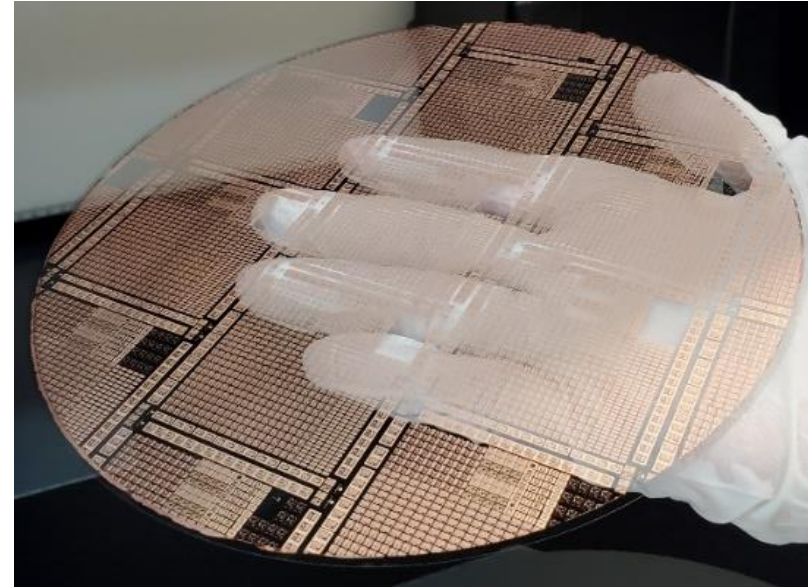


Debonded wafer can stay on dicing tape for singulation, or be removed for second-side processing

200mm wafer on handle



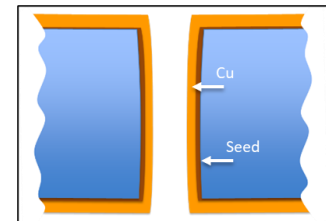
... and debonded



Through-glass vias can be very robust to temperature excursions

Coefficient of thermal expansion (CTE)

- CTE of ABS glass: $\sim 3.4 \text{ ppm}/^\circ\text{C}$
- CTE of Fused Silica: $\sim 0.5 \text{ ppm}/^\circ\text{C}$
- CTE of Copper: $\sim 16.7 \text{ ppm}/^\circ\text{C}$
- Mismatch in CTE must be managed
 - Simplest solution: Keep **via volume low** to keep **stress low**
- ABS will be more reliable than FS
- Conformal coatings can help (but this has other issues)



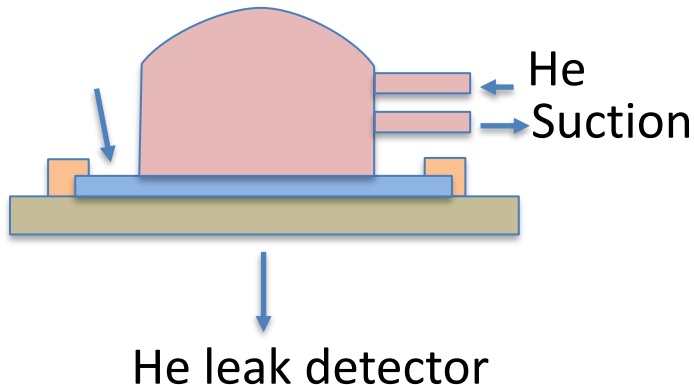
Wafer hermeticity is a good test of glass integrity

Sensitive test:

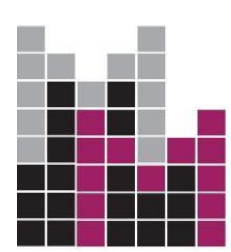
→ System detection limit: $\sim 1 \times 10^{-9}$ atm-cc/s

- Debonded wafer forms the seal between He gas inlet and He leak detector
- Thermally cycle wafer → retest

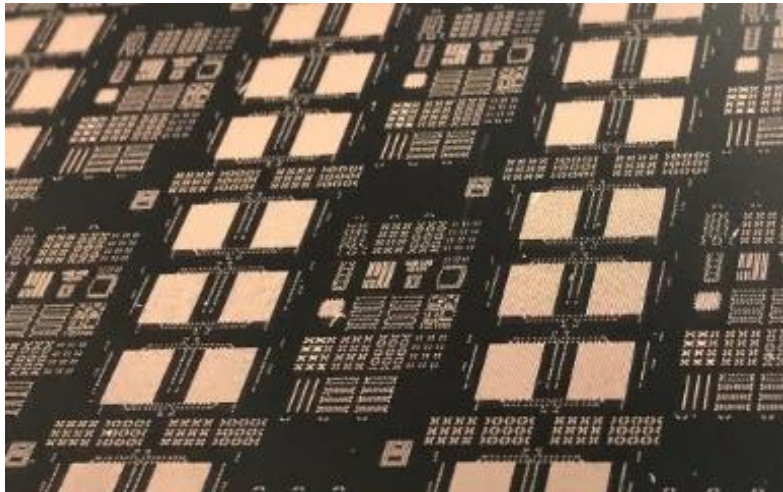
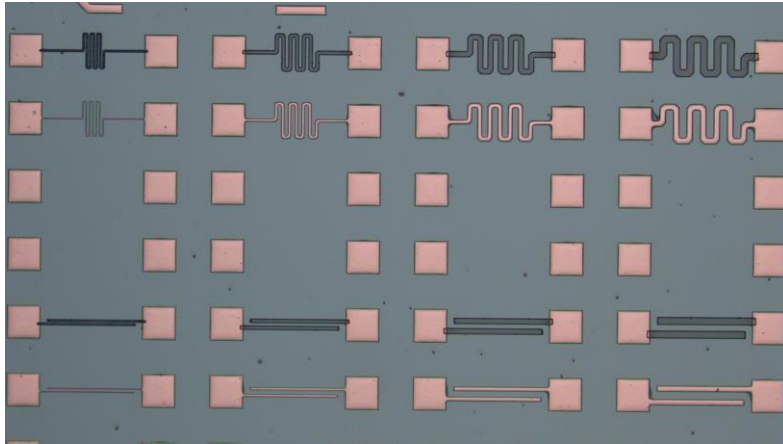
Test wafer



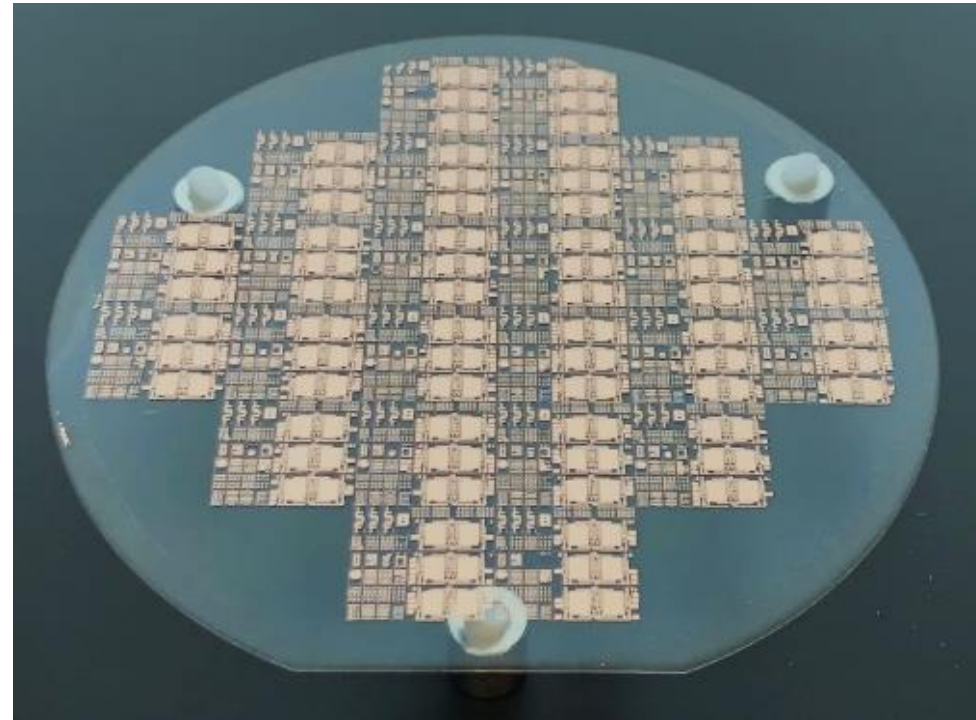
- ABS Hermeticity test (25um via):
 - Demonstrated full wafer ($\sim 30,000$ vias) at detection limit
 - Thermal cycle to 450°C (90 minute hold) x 2
 - Wafer remained at He detection limit
- High Purity FS Hermeticity test (35um via)
 - Demonstrated full wafer at detection limit
 - Thermal cycle to 260°C → remained at detection limit
 - Thermal cycle to 350°C → significant leaks = cracks

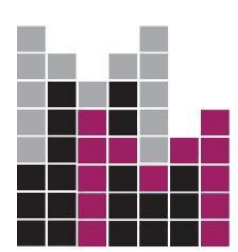


Wafer on handle can get full metallization for redistribution layers and passive devices



Ex. Copper metallization, with thin film resistor, and PBO passivation

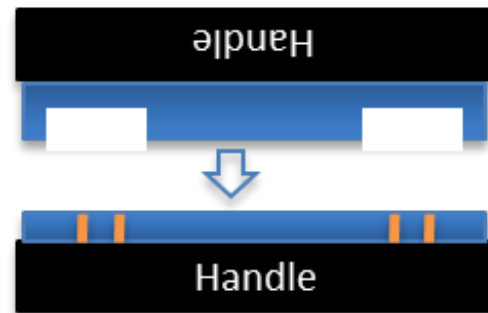




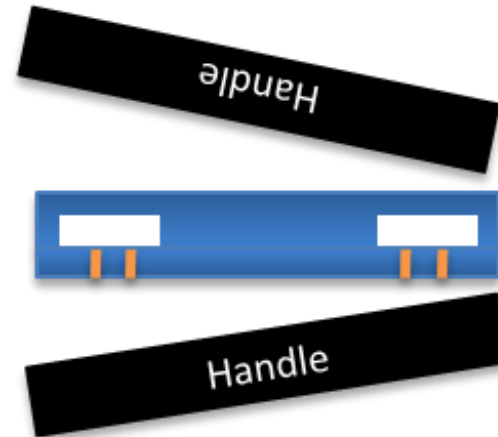
Temporary and permanent bonds allow complex stacks



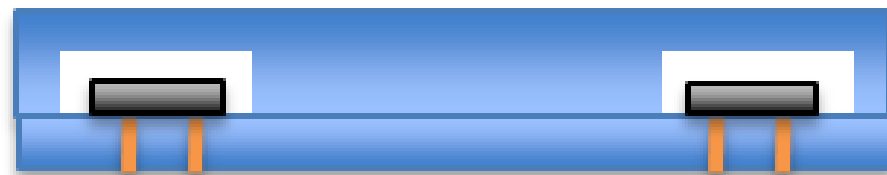
TGV wafer on temporary Handle



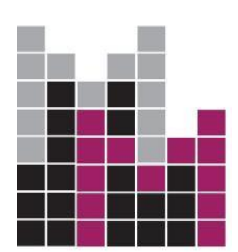
Permanently bond pocket glass to TGV wafer



Remove temporary Handles

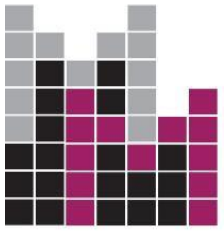


Example: Chips hermetically embedded in a thin glass package



Conclusions

- Precision via formation, void-free Cu fill are enabled by a robust, inorganic, thin-glass temporary bond
- This approach facilitates glass integration into packaging flows
- Complex structures are enabled by bond properties



Acknowledgements

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- Air Force Research Labs



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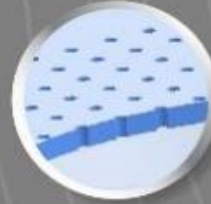


THE FUTURE is CLEAR

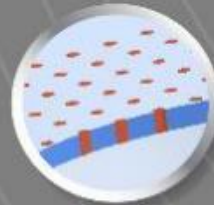
Packaging for 6G Wireless
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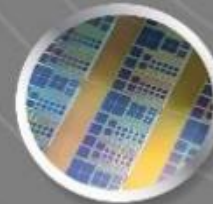
Thin Glass



Thin Glass with Custom
Through-Glass Vias



Thin Glass with Custom
Filled / Planar Vias



Metallized Thin
Glass Wafer

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