D2W Hybrid Bonding using high accuracy carrier solutions for 3D System Integration

EVG: Thomas Uhrmann, Jürgen Burggraf, Mariana Pires
ASMPT: Chun Ho Fan, Hoi Ping Ng, Ming Li
Outline

- Introduction
- Wafer-to-Wafer Bonding vs. Die-to-Wafer Bonding
- Collective Die-to-Wafer Bonding Process Flow
- Process Results – Hybrid Bonding and Multi die transfer
- Conclusion
# D2W vs W2W Hybrid Bonding

<table>
<thead>
<tr>
<th></th>
<th>Hybrid W2W Bonding</th>
<th>Hybrid D2W Bonding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maturity</strong></td>
<td>Wafer Bonding Equipment and Process are matured since 2010</td>
<td>Process and Equipment maturity is starting to yield but still many difficulties</td>
</tr>
<tr>
<td><strong>Contact Pitch</strong></td>
<td>&lt;1µm pitch in enabled in production</td>
<td>Currently 9µm pitch in production</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>Die Size and Grid Matching required</td>
<td>No limitations in die size and system segmentation</td>
</tr>
<tr>
<td><strong>Segmentation</strong></td>
<td>Each bonding layer consist of one node</td>
<td>Each chiplet can consist of a different node</td>
</tr>
<tr>
<td><strong>Yield</strong></td>
<td>Cummulative yield of each bonded layer</td>
<td>Cummulative yield can be avoided by testing</td>
</tr>
<tr>
<td><strong>Throughput</strong></td>
<td>&gt;25 bonds per hour possible</td>
<td>Related to chip size and amount of chiplets per system</td>
</tr>
</tbody>
</table>

## Diagram

1. **Annealing Process**
   - **Step 1:** Single Wafer Cleaning
   - **Step 2:** Wafer to Wafer Alignment
   - **Step 3:** Prebonding
   - **Step 4:** Thermal Annealing

2. **Dielectric Layer**
   - **Step 2:** Dielectric layer Annealing
Die Bonding Integration | Die-to-Wafer vs. Wafer-to-Wafer Bonding

Die-to-Wafer Bonding

High Performance Device

Require larger Die size

→ High system integration costs

→ Only the “Good” dies are bonded to the target wafer → High Yield

→ Allow stacking of different physical dimensions from arbitrary technologies and substrates sizes.

→ Integration of multiple dies onto a single base die of the substrate wafer.

Costs

Increase driven by increased Die size and lower yield

C2W / KGD integration is favorable for increased Die sizes

Source: IMEC – 2019 3D & systems summit
# D2W Bonding | Recent Announcements

<table>
<thead>
<tr>
<th>Transfer Method</th>
<th>Co-D2W</th>
<th>DP-D2W</th>
<th>SA-D2W</th>
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<tbody>
<tr>
<td><strong>Transfer Method</strong></td>
<td>Collective Die Transfer by Reconstituted Carrier</td>
<td>Direct placement of activated dies using Flip Chip Bonder</td>
<td>Self Assembly on hydrophilic guiding pads</td>
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<td><strong>Maturity</strong></td>
<td>Limited volume production proven for several years</td>
<td>Feasibility testing ongoing</td>
<td>Experimental results available, Feasibility testing required</td>
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</table>

**March 2, 2020**

**EV Group Establishes Heterogeneous Integration Competence Center**

New HIC Competence Center to help customers accelerate new product development fueled by heterogeneous integration and advanced packaging.

**March 29, 2021**

**EV Group Addresses Key Process Gap in Heterogeneous Integration with Collective Die-to-Wafer Hybrid and Fusion Bonding Demonstration**

Company successfully demonstrates end-to-end process flow for collective die-to-wafer bonding with sub-micron placement accuracy at EVG's Heterogeneous Integration Competence Center™

**October 19, 2020**

**EV Group Unveils Hybrid Die-to-Wafer Bonding Activation Solution to Speed Up Deployment of 3D Heterogeneous Integration**

EVG™120 D2W die preparation and activation system provides seamless integration with third party die bonders, completing EVG’s equipment portfolio for end-to-end hybrid bonding for 3D heterogeneous integration.

**December 10, 2020**

**ASM Pacific Technology and EV Group Join Forces to Enable Industry’s First Ultra Precision Die-to-Wafer Hybrid Bonding Solutions for 3D-IC Heterogeneous Integration**

Joint Development Program will offer highly configurable, ultra-precision end-to-end hybrid bonding solutions to suit various applications, with optimal line balancing and process requirements.
## Hybrid D2W Bonding | EVG Process Support Options

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<tr>
<th>Transfer Method</th>
<th>Co-D2W</th>
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</table>
| **Pro’s**       | • Proven technology  
                  • Die Activation and cleaning equivalent to W2W hybrid bonding  
                  • Oxide management  
                  • Rework on carrier feasible | • Versatile method  
                  • Die thickness invariant | • Avoids high precision flip chip bonder and potential cost saving  
                  • Die thickness invariant |
| **Con’s**       | • Error propagation of D2W + W2W alignment  
                  • Cost of carrier prep, utilization and clean  
                  • Die thickness needs to be in narrow range | • Bonding interface needs to be touched  
                  • Die handling especially for multi die stacks such as SRAM, DRAM  
                  • Particle management during die placement | • High precision die preparation using chemical treated zones  
                  • Dicing potentially affects placement  
                  • Die strain is affecting self alignment results |
| **Maturity**    | Limited volume production proven for several years | Feasibility testing required and ongoing | Experimental results available, Feasibility testing ongoing |
**Hybrid D2W Bonding | EVG Process Support Options**

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**Transfer Carrier Preparation**
- Glass or Silicon Carrier Wafer (non-patterned or with alignment marks)
- Carrier Wafer with Adhesive Layer

**Carrier Population**
- Co-D2W Bonding
- Reconstituted Wafer

**Wafer-to-Wafer Bonding**
- Plasma Activation Handler
- Plasma Activation Target Wafer
- Cleaning Handler
- Cleaning Target Wafer
- Carrier Flip
- SmartView Alignment
- Hybrid Bonding

**Carrier Separation**
- Slide-Off or Laser Deboning
- Surface Cleaning
# Hybrid D2W Bonding | EVG Process Support Options

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<th>Transfer Method</th>
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<td>• Die handling especially for multi die stacks such as SRAM, DRAM</td>
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<td>• Particle management during die placement</td>
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IR Laser Release | Reconstructed D2W Bonding

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<tbody>
<tr>
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<td>Collective Bonding (Die Level Bonding)</td>
<td>Direct placement of activated dies using Flip Chip Bonder</td>
<td>Self Assembly on hydrophilic guiding pads</td>
</tr>
</tbody>
</table>

**Pro’s**
- Proven technology
- Die Activation and cleaning equivalent to W2W hybrid bonding
- Oxide management
- Rework on carrier feasible
- Versatile method
- Die thickness invariant
- Avoids high precision flip chip bonder and potential cost saving
- Die thickness invariant

**Con’s**
- Error propagation of D2W + W2W alignment
- Cost of carrier prep, utilization and clean
- Die thickness needs to be in narrow range
- Bonding interface needs to be touched
- Die handling especially for multi die stacks such as SRAM, DRAM
- Particle management during die placement
- High precision die preparation using chemical treated zones
- Dicing potentially affects placement
- Die strain is affecting self alignment results

**Maturity**
- Limited volume production proven for several years
- Qualification and ramp up
- Experimental results available, Feasibility testing ongoing

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Combination of known good dies on carrier with anorganic wafer level pre processing, post processing and W2W bonding
## IR Laser Release | Reconstructed D2W Bonding

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<td><strong>Transfer Method</strong></td>
<td>Collective Bonding (Die Level Bonding)</td>
<td>Reconstructed W2W (Anorganic Fill Process)</td>
<td>Direct placement of activated dies using Flip Chip Bonder</td>
<td>Self Assembly on hydrophilic guiding pads</td>
</tr>
<tr>
<td><strong>Pro’s</strong></td>
<td>• Proven technology</td>
<td>• Proven process</td>
<td>• Versatile method</td>
<td>• Avoids high precision flip chip bonder and potential cost saving</td>
</tr>
<tr>
<td></td>
<td>• Die Activation and cleaning</td>
<td>• High yield, clean process</td>
<td>• Die thickness invariant</td>
<td>• Die thickness invariant</td>
</tr>
<tr>
<td></td>
<td>equivalent to W2W hybrid bonding</td>
<td>• All based on standardized wafer-based</td>
<td></td>
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<tr>
<td></td>
<td>• Oxide management</td>
<td>manufacturing equipment</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Rework on carrier feasible</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Con’s</strong></td>
<td>• Error propagation of D2W + W2W</td>
<td>• W2W bonding process is heavily impacted by</td>
<td>• Bonding interface needs to be touched</td>
<td>• High precision die preparation using chemical treated zones</td>
</tr>
<tr>
<td></td>
<td>alignment</td>
<td>die grid and filling factor between dies</td>
<td>• Die handling especially for multi die stacks such as SRAM, DRAM</td>
<td>• Dicing potentially affects placement</td>
</tr>
<tr>
<td></td>
<td>• Cost of carrier prep, utilization</td>
<td></td>
<td>• Particle management during die placement</td>
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<tr>
<td></td>
<td>and clean</td>
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</tr>
<tr>
<td></td>
<td>• Die thickness needs to be in</td>
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<tr>
<td></td>
<td>narrow range</td>
<td></td>
<td></td>
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<tr>
<td><strong>Maturity</strong></td>
<td>Limited volume production proven for several years</td>
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**Combination of known good dies on carrier with anorganic wafer level pre processing, post processing and W2W bonding**
## Reconstituted W2W (Anorganic Fill Process)

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<th><strong>Transfer Method</strong></th>
<th>Reconstituted W2W (Anorganic Fill Process)</th>
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</table>

### Pro’s
- Proven technology
- Die Activation and cleaning equivalent to W2W hybrid bonding
- Oxide management
- Rework on carrier feasible

### Con’s
- Error propagation of D2W + W2W alignment
- Cost of carrier prep, utilization and clean
- Die thickness needs to be in narrow range

### Maturity
- Limited volume production proven for several years

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**Silicon carrier with IR release layers**
- Glass or Silicon Carrier Wafer (with alignment marks)
- D2W Placement
- Low-Temp Inter Die Fill Process
- Patterning, Filling and CMP of Bond Pads on Wafer Level

**Wafer-to-Wafer Bonding**
- Plasma Activation Handler
- Plasma Activation Target Wafer
- Cleaning Handler
- Cleaning Target Wafer
- Carrier Flip
- SmartView W2W Alignment
- Hybrid Bonding

**EVG Nanocleave IR Laser Release**
- Carrier Release or Removal
- Surface Cleaning

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**IMAPS 19th Conference on DEVICE PACKAGING | March 13-16, 2023 | Fountain Hills, AZ USA**
D2W Bonding – Process Results
Die-to-Wafer Bonding | Die Transfer Capabilities

- Die placement accuracy 1 µm → 500 nm upcoming

- Die Size
  600 µm x 600 µm up to 40 mm x 40 mm

- Materials
  InP, GaAs, Si, GaN, SiC

- Carrier Size:
  200 mm & 300 mm

- Bonding Processes
  Direct, Metal, Adhesive bonding, Hybrid bonding

- Debonding Technology
  Thermal Slide off or Laser debonding
Direct Placement (DP-D2W) Bonding | Process Flow

**Transfer Method** | **Pro’s** | **Con’s** | **Maturity**
--- | --- | --- | ---
**DP-D2W**
Direct placement of activated dies using Flip Chip Bonder | • Versatile method  
• Die thickness variation | • Die handling especially for multi die stacks such as SRAM, DRAM  
• Particle management during die placement | • Feasibility testing required and ongoing

Customers would prefer direct placement → Particle / yield issue
Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

**Alignment Strategy**
- a. Local alignment key for every die
- b. Global alignment key for wafer to wafer alignment

<table>
<thead>
<tr>
<th>Transfer Method</th>
<th>Pro’s</th>
<th>Con’s</th>
<th>Maturity Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collective Die Transfer by</td>
<td>• Proven technology</td>
<td>• Error propagation of D2W + W2W alignment</td>
<td>High</td>
</tr>
<tr>
<td>Reconstituted Carrier</td>
<td>• Die activation and cleaning equivalent to W2W hybrid bonding</td>
<td>• Cost of carrier prep, utilization and clean</td>
<td>Volume production proven for several years</td>
</tr>
<tr>
<td></td>
<td>• Oxide management</td>
<td>• Die thickness needs to be in narrow range</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Reuse of carrier feasible</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
A protective layer is applied on top of the dies to prevent the contamination of the die surface during the dicing and carrier population processes.

Courtesy of IMEC
• The D2W bonding is performed at wafer level using the same W2W bonding systems.
Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

**Carrier Separation**
- Slide-Off or Laser Debonding
- Surface Cleaning

**Alignment Strategy**
1. Local alignment key for every die
2. Global alignment key for wafer to wafer alignment
Collective Die-to-Wafer (Co-D2W) Bonding | Carrier Separation

Lift-Off Debond

- Process compatible with thermoplastic material and thermo release tapes.
- Debond process < 210°C.
- No specific carrier type is required.

UV Laser Debond

**EVG®850DB**

- RT debond process
- Glass carrier is required.
- Process compatible with adhesive and UV tape

Adhesive Cleaning – Target wafer with dies

**EVG301®**

- Solvent cleaning process.
- Chemistry used for Co-D2W bonding:
  - Mesitylen (EVG POR)
  - STW32
  - MEK
  - IPA (EVG POR)
**Collective Die-to-Wafer (Co-D2W) Bonding | Metrology**

**Metrology // Co-D2W Bonding**

- Post Co-D2W Bonding inspection:
  - EVG50® - Die transfer rate
  - EVG40®NT (2) – D2W alignment verification
  - C-SAM – Bond quality

**D2W Bonding interface:**

![Picture – C-SAM inspection post D2W bonding.](image)

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**D2W alignment verification**

- Bond alignment with transmitted IR
- Bond alignment with reflected IR

D2W + W2W alignment accuracy can be checked by TIR or RIR.

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**Post Bond Alignment accuracy Cumulative Plot**

![Image of cumulative plot](image)
Co-D2W Bonding | **Process Results – Hybrid Bonding**

**Demonstrator A - 300mm**
Hybrid Bonding, 5 mm x 7 mm

**Demonstrator B - 300mm**
Hybrid Bonding, 10 mm x 14 mm

→ Pad Size 4 μm – 1 μm

→ Pitch 10 μm – 2 μm

*Substrates provided under IRT Nanoelec program*
Co-D2W Bonding | Process Results – Hybrid Bonding

<table>
<thead>
<tr>
<th>Demonstrator</th>
<th>Die Dimension</th>
<th>Placement accuracy $x \ 3\sigma$</th>
<th>Placement accuracy $Y \ 3\sigma$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>5mm x 7mm</td>
<td>&lt; 2 $\mu$m</td>
<td>&lt; 2 $\mu$m</td>
</tr>
<tr>
<td>B</td>
<td>10mm x 14mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Co-D2W Bonding | Process Results – Hybrid Bonding

→ High Die transfer rate and alignment accuracy < 2µm

→ TEM evaluation of mechanical contact of the bonding pads and Cu grain growth across the bonding interface
Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

2D and 3D Multi Die transfer

C2W Hybrid bonding capability
Overlay <500nm

2D Multi Die Transfer to substrate

3D Multi Die Transfer to substrate

Demonstrator A

Target wafer: 200mm Thermal Oxide wafer

Collective carrier wafer: 200mm Bare Silicon wafer

Die sizes:
- 1x1mm x 350µm dies
- 3x3mm x 350µm dies
- 7x9mm x 350µm dies

Picture – Collective die carrier wafer map.

Picture – Collective die carrier wafer map – die detail.
Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

Post collective carrier preparation inspection

- A high-resolution die height variation (DHV) measurement was performed on the collective carrier with dies after placement using a chromatography sensor to evaluate the die uniformity / distribution.

- A die height variation < 3µm could be observed after collective die carrier preparation.

![Picture – Collective die carrier wafers after die placement process.](image1)

**Die Height variation Measurement**

- a): Full scan – 2D collective carrier map; b): Detail scan – 3D collective carrier map.

- c): Detail scan – 2D collective carrier map

- d): Detail scan – DHV across the blue line.

![Die Height variation Measurement](image2)
Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

- High transfer yield including high bonding quality based on Scanning Acoustic microscope images (C-SAM) could be achieved.

Picture – Target wafer with dies after die transfer process.

Picture – Target wafer with dies after die-to-wafer bonding process – die detail.

C-SAM inspection – Post annealing inspection – detail scan.

C-SAM inspection – Post annealing inspection – full scan.
### Collective Die Transfer | Direct Bonding - ComBond

<table>
<thead>
<tr>
<th>Bonding Process</th>
<th>Die Substrate Material</th>
<th>Die Dimension</th>
<th>Target Substrate Material</th>
<th>Bonding Interface</th>
<th>Bonding Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide free direct bonding</td>
<td>Si</td>
<td>5 mm x 5 mm</td>
<td>Silicon</td>
<td>SiSi</td>
<td>RT</td>
</tr>
</tbody>
</table>

High transfer yield and high bonding quality based on Scanning Acoustic microscope image and TEM could be demonstrated for collective D2W bonding in Combond.

Expand collective Die to wafer bonding to high Vacuum ComBond technology.
Summary

W2W Hybrid Bonding

EVG is market leader for W2W hybrid bonding equipment with more than 80% market share over the last 2 years.

EVG fusion and hybrid bonding equipment in W2W bonding is standard process in major IDM and Foundries.

Sub 100nm W2W overlay accuracy developed and currently moved in high volume production.

D2W Hybrid Bonding

Several Process Integration schemes are present in the market today with application specific pros and cons.

Enabling wafer based cleaning, activation and processing equipment for D2W hybrid bonding for full process transferability from W2W.

EVG320D2W Fully integrated system solution with standardized process modules.

IR Laser Release – EVG Nanocleave

Novel & universal IR release technology through silicon wafers.

Precisely controlled cleaving without IR transmission or risk for product.

Inorganic IR release layers with nanometer precision separation trigger.
EV GROUP (EVG)

Get in touch to discuss your high volume manufacturing needs!

THANK YOU!