Glass Core Substrates
Opportunities for CHIPS and MMI - from Research to Manufacturing

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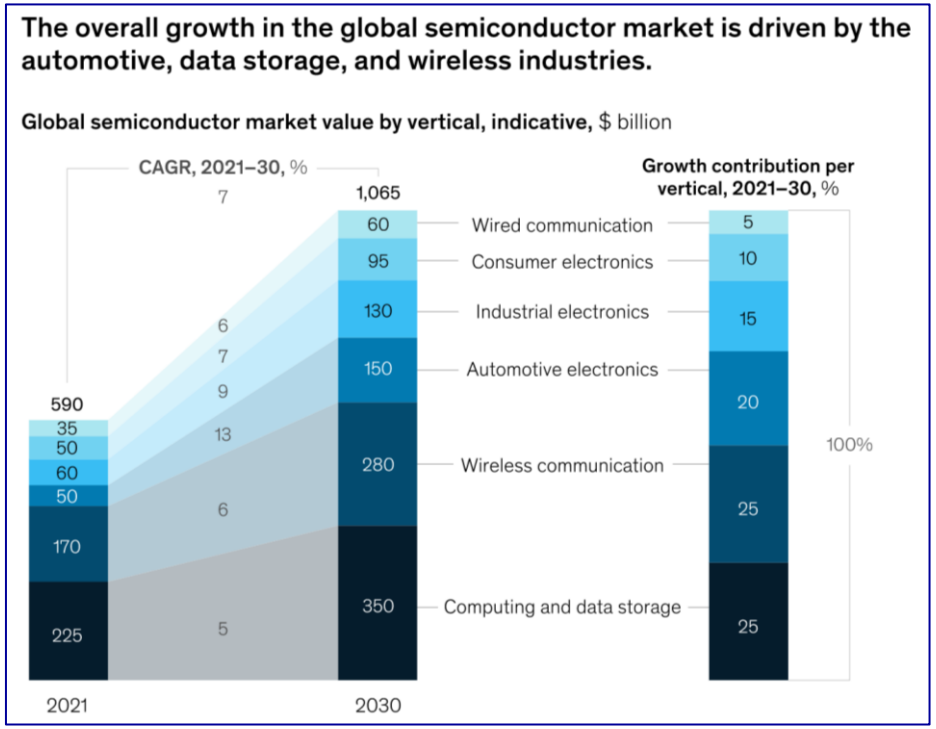
Why is Packaging of National Importance to US?

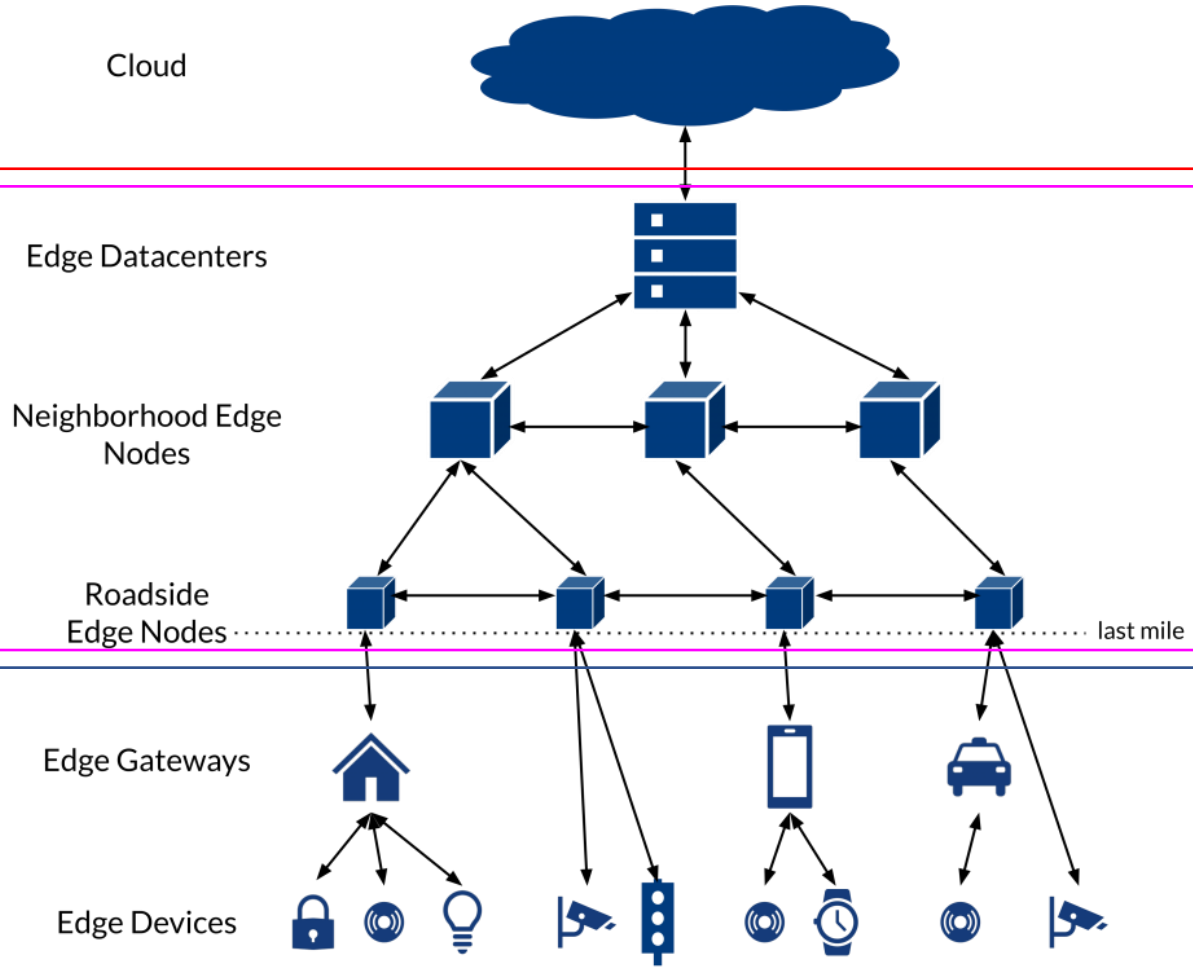
- Global semiconductor industry projected to become a trillion-dollar industry by 2030 (Source: McKinsey & Company)
  - 55 years to become a 0.5T industry
  - Expected to double in the next 10 years
  - Drivers: Computing/Storage, Wireless, Automotive, ….

- US losing Leadership
  - Chip
    - Less than 12% of Semiconductor Manuf. in USA
  - **Packaging**
    - **Less than 2% of Substrate Manuf. in USA**
    - **Less than 6.5% of Flip-Chip bumping in USA**

- 2022: CHIPS for America Act
  - Establish Onshoring Capabilities and U.S. Leadership
  - $52B Investment **($11B for R&D & Workforce Development)**



Emerging Distributed & Edge Computing



- Storage, Coordinator of lower levels
- Limitless Compute Power
- ~8000

- Base stations, Routers, Switches
- High Compute Power
- 10-100 million devices

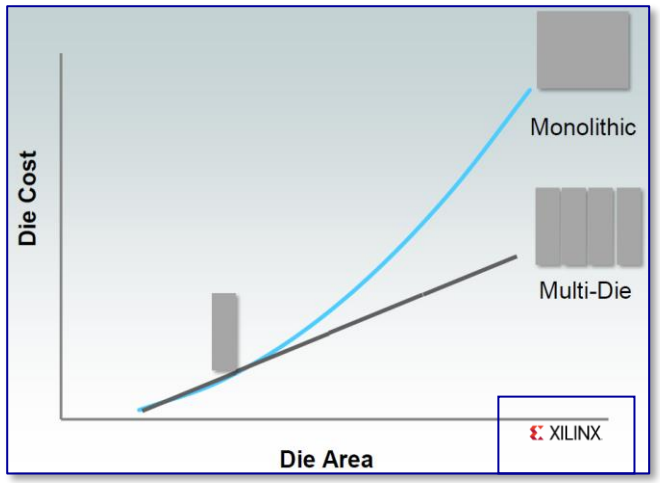
- Sensors, Smart Phones, Automobiles
- Billions of devices

Ref: Jeff Burns, "Systems and Architectures for Distributed Compute", SRC Workshop, 2022.

https://www.inovex.de/de/blog/edge-computing-introduction/

Need for Chiplets & Heterogeneous Integration

1



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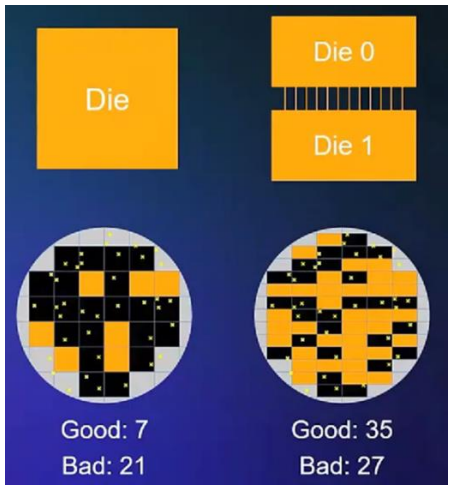
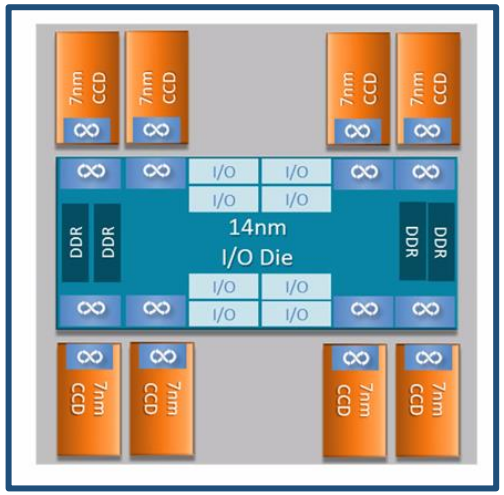
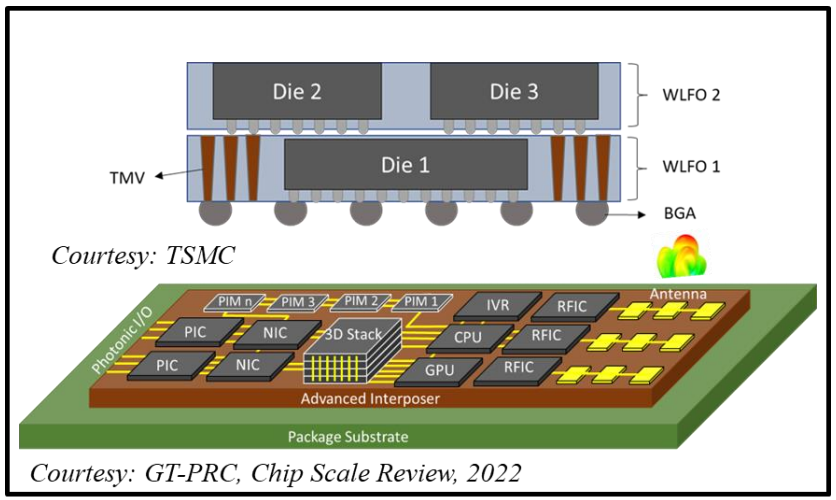


Source: EDAPS Keynote, 2021



Source: AMD

3



1. Higher yield using smaller dies in advanced nodes (dis-aggregation & re-aggregation)
2. Shorter time to design with smaller dies from optimized legacy technology nodes with enhanced functionality.
3. Move towards **HETEROGENEOUS INTEGRATION**.

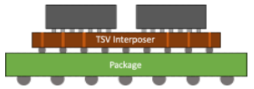
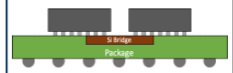
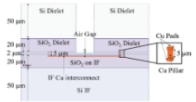
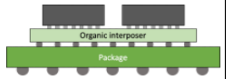
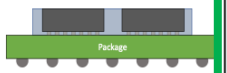
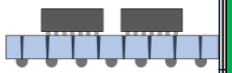
Packaging Landscape

Heterogeneous Architectures

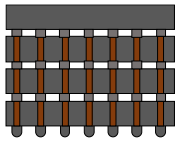
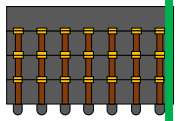
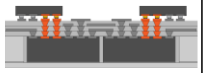
- 2D
  - Silicon
    - 2.5D TSV Interposer
    - Embedded Silicon Bridge
  - Organic
    - 2.5D Organic Interposer
    - 2.1D Organic Interposer
    - Wafer/Panel Fanout
  - Glass
    - 2.5D Glass Interposer (Chip Last)
    - 2.5D Glass Embedded (Chip First)
    - Our Focus
  - Others
    - LTCC
    - Si Micromachining
- 3D
  - TSV Based
    - 3D Stacking with Microbumps
    - 3D Stacking with Hybrid Bonding
    - IC Foundry only technologies 2-16 High Stacks
  - Non-TSV Based
    - 3D Glass Embedding
    - Package Foundry F2F through RDL
    - Our Focus

S. Ravichandran & M. Swaminathan, Heterogeneous Integration for AI Applications: Status & Future Needs, Chip Scale Review, 2022

Heterogeneous Integration Comparison

	2D/2.5D integration					
	Silicon			Organic		Glass
	TSV Interposer (Martwick, et al, 2016)	Si Bridge (EMIB) (Mahajan, et al, 2019)	Silicon IF (Jangam, et al, 2018)	Organic Interposer (Turner, et al, 18)	Chip-last Fanout (Wang, et al 2019)	Glass Interposer (Mukhopadhyay, et al. '19)
						
Status	Commercial	Commercial	Research	Commercial	Development	Research
Dielectric constant	3.9	3.9*	3.9	3.0*	3.2	2.5-3.0
IO pitch	50 µm	45 µm	10 µm	55 µm	40	55 µm
Interconnect length	5 mm	5 mm	0.5 mm	6 mm	1 mm	2.5 mm
Interconnect density	250 IO/mm/layer	300 IO/mm/layer	n/a	25 IO/mm/layer	500 IO/mm/layer	250 IO/mm/layer
V_{swing}	1.2 V	1 V	1 V	0.15 V	1 V	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	39/0.4p/0.4p	50/0.5p/0.5p	30/50f/50f	n/a	50/0.4pF/0.4pF	30/0.3pF/0.3pF
Data rate/IO	2 Gbps	5 Gbps	4.21 Gbps	20 Gbps	9.5 Gbps	9.2 Gbps
Bandwidth density	500 Gbps/mm	1500 Gbps/mm	1300 Gbps/mm	500 Gbps/mm*	4750 Gbps/mm	2300 Gbps/mm
Energy-per-bit	1.025 pJ/bit*	1.2* pJ/bit	0.4 pJ/bit	0.58 pJ/bit	0.78 pJ/bit*	0.36 pJ/bit

** Derived metric*

3D Integration	TSV-based		Non-TSV
	3D IC /w TSV [Zhang, et al. '18]	Hybrid Bonding [Chen, et al, '19]	3D Glass Embedding [Ravichandran, et al, '19]
			
Status	Commercial	Commercial	Research
Dielectric Constant	3.9*	3.9*	2.5-3
IO pitch	40 µm	10 µm	20 µm
Interconnect length	75 µm*	50 µm*	35-50 µm
Interconnect density (IO/mm^2)	625	10000	2500
V_{swing}	0.7 V*	1 V*	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	n/a	n/a	50/50f/50f
Data rate/IO	1.69 Gbps	n/a	1.86 Gbps
Bandwidth density	1.76 $Tbps/mm^2$*	n/a	4.65 $Tbps/mm^2$
Energy-per-bit	76.2 fJ/bit	7 fJ/bit*	11.2 fJ/bit

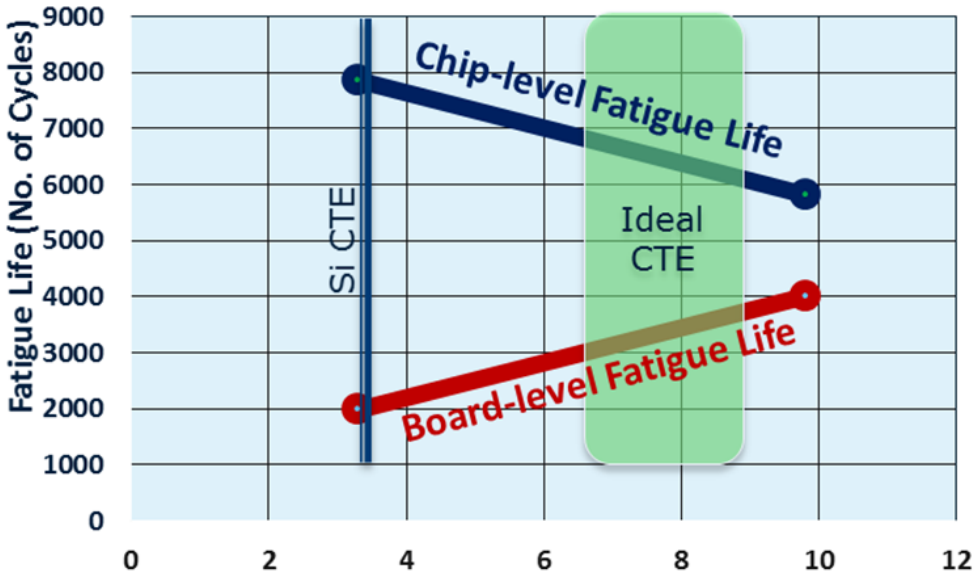
** Derived metric*

- ❑ 3D Integration necessary to reach fJ/bit.
- ❑ Bandwidth density much higher with 3D integration.
- ❑ Enables disaggregation and reaggregation of memory.

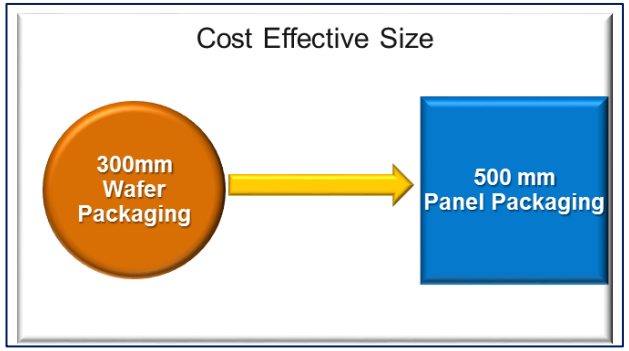
S. Ravichandran and M. Swaminathan, Chip Scale Review (2022)

Why Glass?

Substrate Core	Silicon	Organic		Glass
		Laminates	Fanout (Epoxy Mold Compound)	
Material properties				
Surface roughness (nm)	<10	400-600	> 1000	<10
CTE (ppm/K)	2.9-4	3-17	16-30	3-9
Young's modulus (GPa)	165	10-40	22	50-90
Moisture absorption	0	0.04%	1-2.5%	0
Thermal conductivity (W/m.K)	148	0.9	0.5-0.75	1.1
Physical Dimensions				
Package size (mm)	35x35	70x70	50x50	100x100
Panel/Wafer size	300 mm	710 mm^2	300 mm / 510 mm^2	710 mm^2

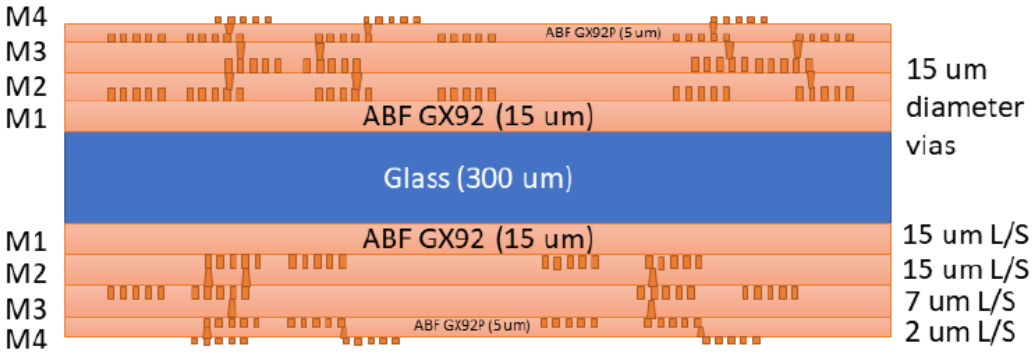


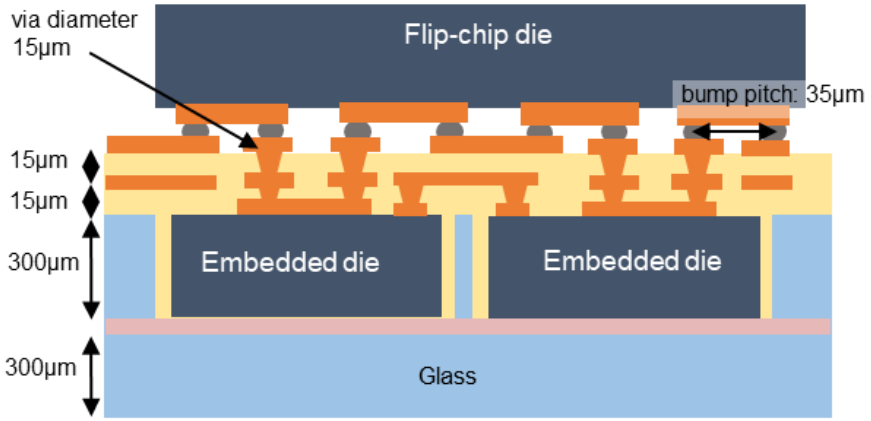
- Smoothness enables dense connectivity between chips
- Tailorable thermal expansion improves reliability
- Stiffness eases manufacturability
- Zero moisture absorption improves stability
- Low thermal conductivity isolates hotspots
- Dielectric insulation improves performance
- Large area panel processing which reduces cost



S. Ravichandran & M. Swaminathan, Heterogeneous Integration for AI Applications: Status & Future Needs, Chip Scale Review, 2022

Glass Interposer for Computing: Recent Research Results





Cross section of the 3D embedded die with die-to-die interconnects

Christopher Blancher, Mohanalingam Kathaperumal, Fuhan Liu, and Madhavan Swaminathan, ECTC 2023

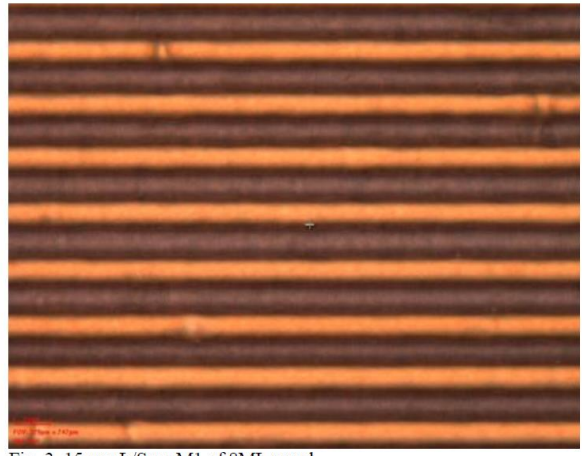


Fig. 3. 15 µm L/S on M1 of 8ML panel

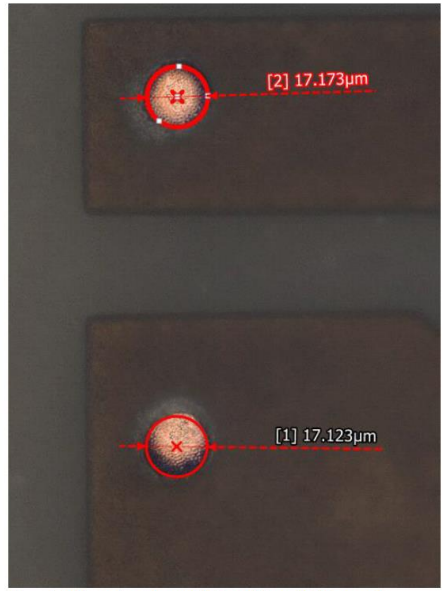


Fig. 4. Microvias from M2 to M1 on 8ML panel

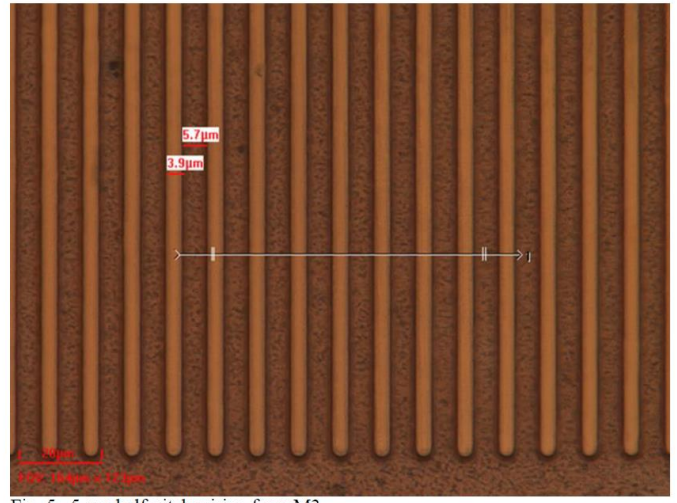
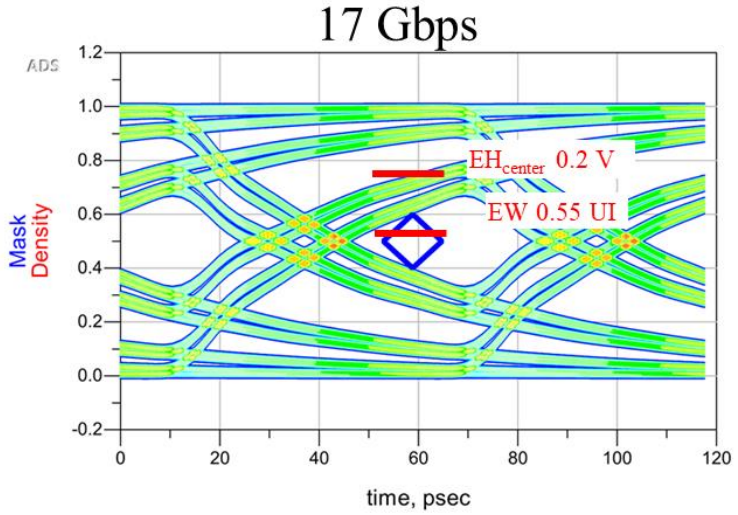


Fig. 5. 5 µm half-pitch wiring from M3



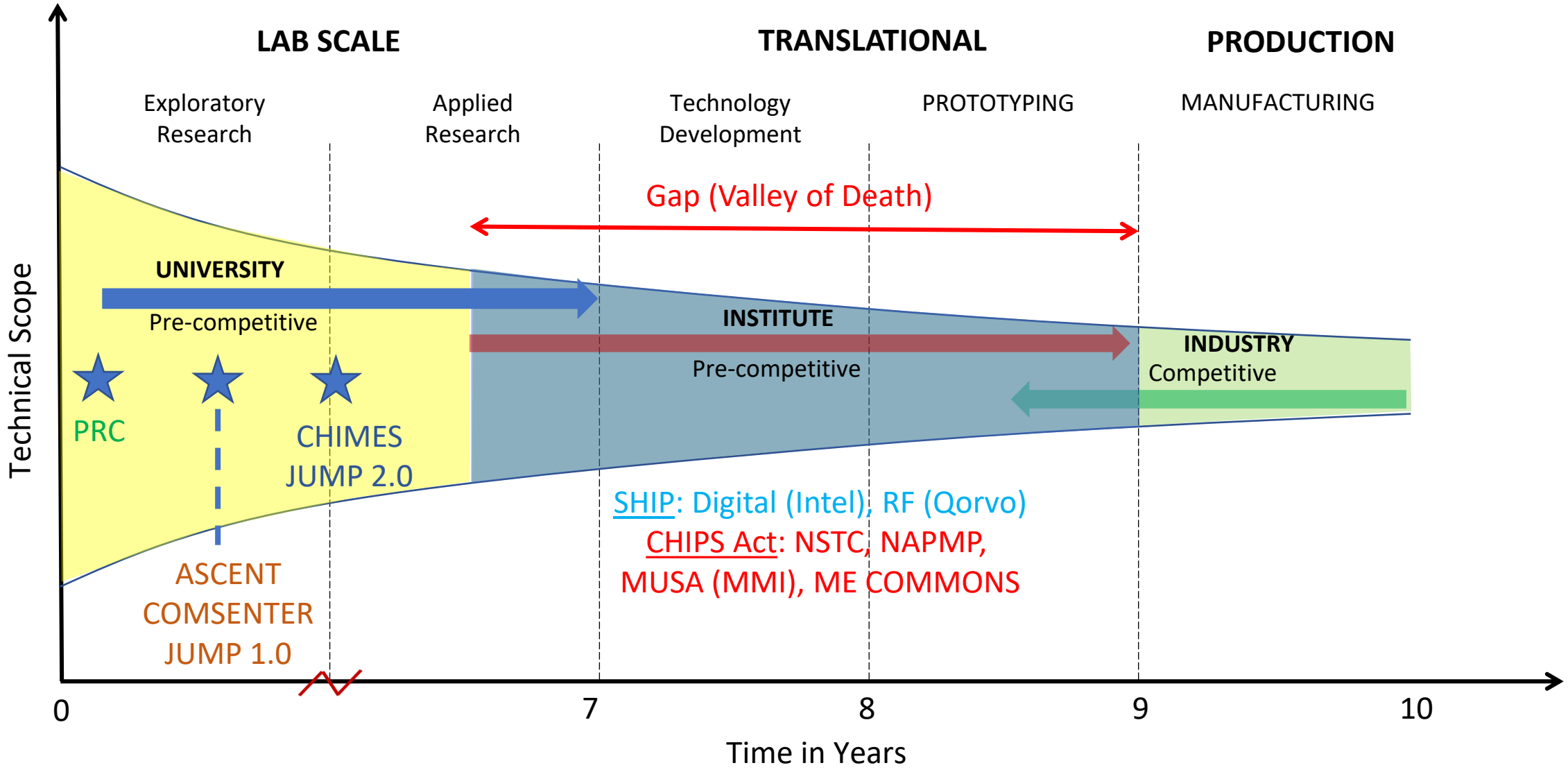
Courtesy: Serhat Erdogan, Ph.D. Student, GT

Georgia Tech PACKAGING RESEARCH CENTER

PennState College of Engineering | ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

CHIMES Center for Heterogeneous Integration of Micro Electronic Systems

Lab – to – Fab Funnel

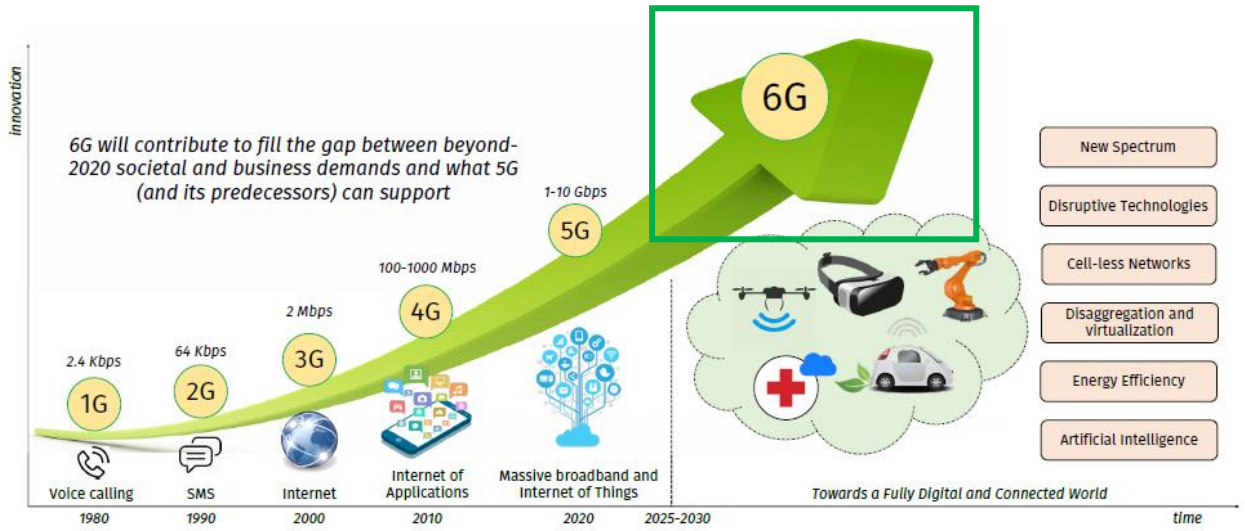


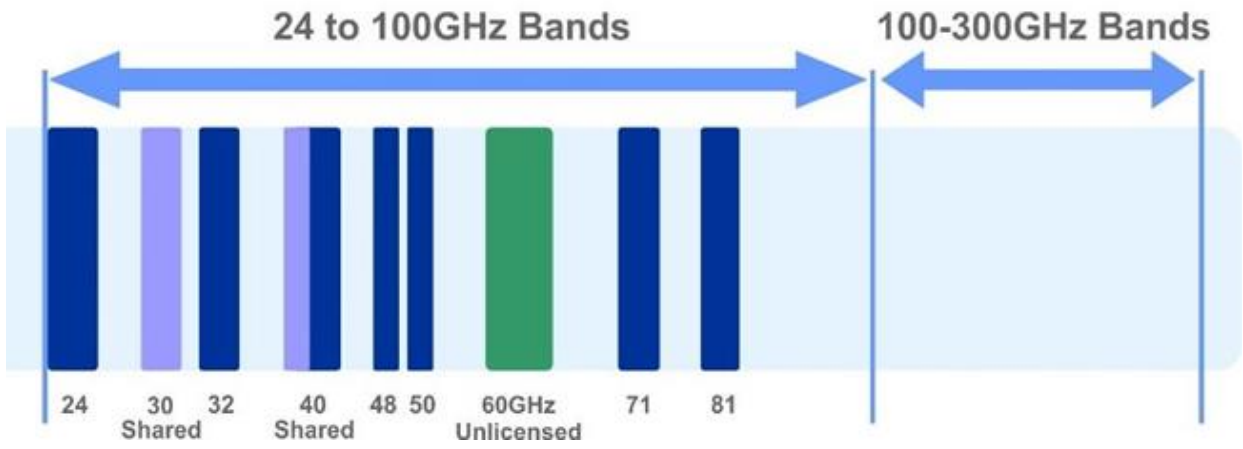
Tech Transfer to High Volume Manufacturing for Computing

- ❑ SK Group to Locate First of its Kind Glass-based Semiconductor-part Venture in Covington, GA (Absolics) **Interactions with GT-PRC**
- ❑ Announcement by Governor Brian P. Kemp (Atlanta, GA – October 28, 2021)
- ❑ Company will invest more than $473 million in this unprecedented venture and will create more than 400 new jobs in Newton County
- ❑ Groundbreaking Nov ‘22
- ❑ Low Volume 2024; High Volume 2025

https://www.georgia.org/press-release/sk-group-locate-first-its-kind-glass-based-semiconductor-part-venture-covington

Wireless Communication: 6G & Beyond

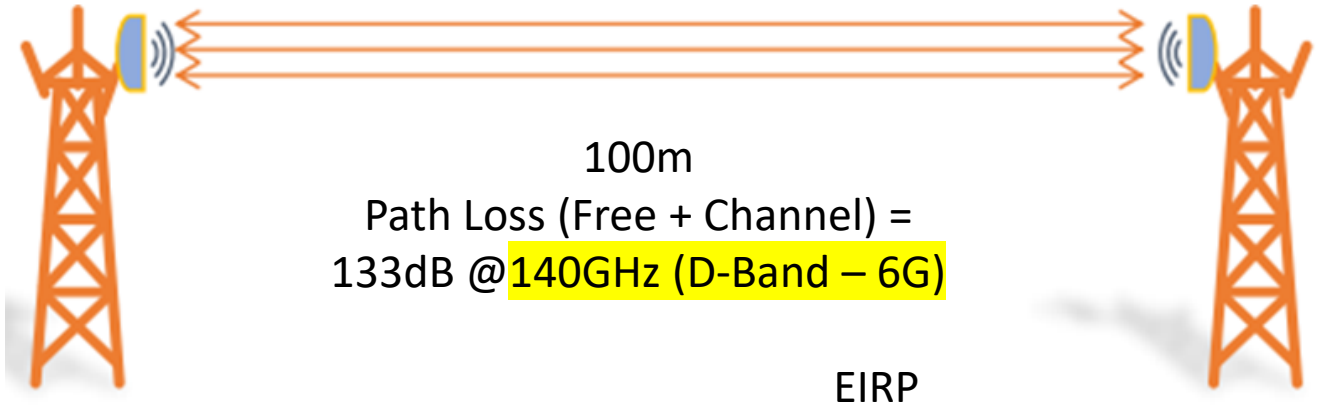




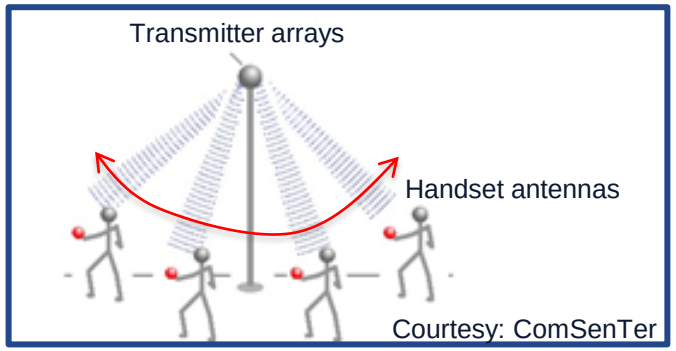
- ❑ Applications emerging in Augmented Reality, Virtual Reality, Teleportation, eHealth ….
- ❑ Pervasive Connectivity: 10^6 devices/km^2 (5G) to 10^7 devices/km^2 (6G)
- ❑ Capacity: 20Gbps (5G) to 1Tbps (6G)
- ❑ Unmanned mobility: Autonomous transportation with high reliability & low latency
- ❑ Intelligent Communications!

Marco Giordani, Michele Polese, Marco Mezzavilla, Sundeep Rangan, and Michele Zorzi, "Towards 6G Networks: Use Cases and Technologies", IEEE Communications Magazine 2020
Rappaport et. al Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!

Backhaul Link & Access point Requirements



100m
Path Loss (Free + Channel) =
133dB @140GHz (D-Band – 6G)



EIRP
+72dBm

AiP

1

Heat
Removal

3

Loss

2

Ant. Gain
+36dBm

Free space
Channel Loss
-133dB

Ant. Gain
+36dBm

128-QAM
SINR 30dB (BW=8GHz)

Rx Power
-26dBm

Link Margin
11dB

-37dBm

Tx Radio | Package | Package | Rx Radio

Tx P_{sat}
37dBm
150 W/cm^2

Loss
1dB

Tx Power
+36dBm

Signal
-61dBm

Rx Power
-25dBm

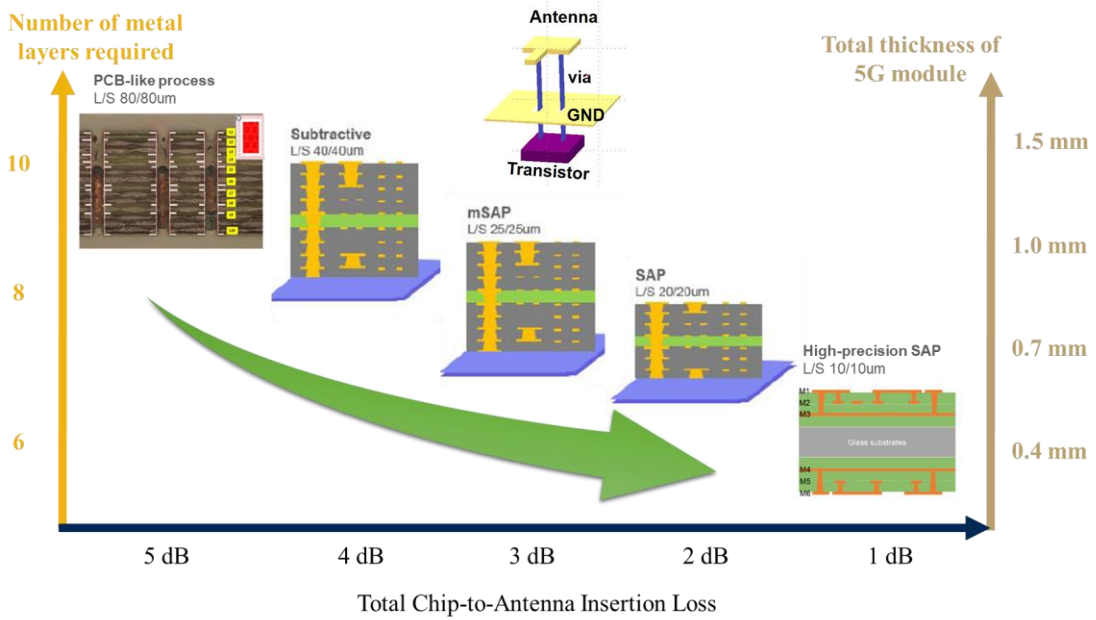
Loss
1dB

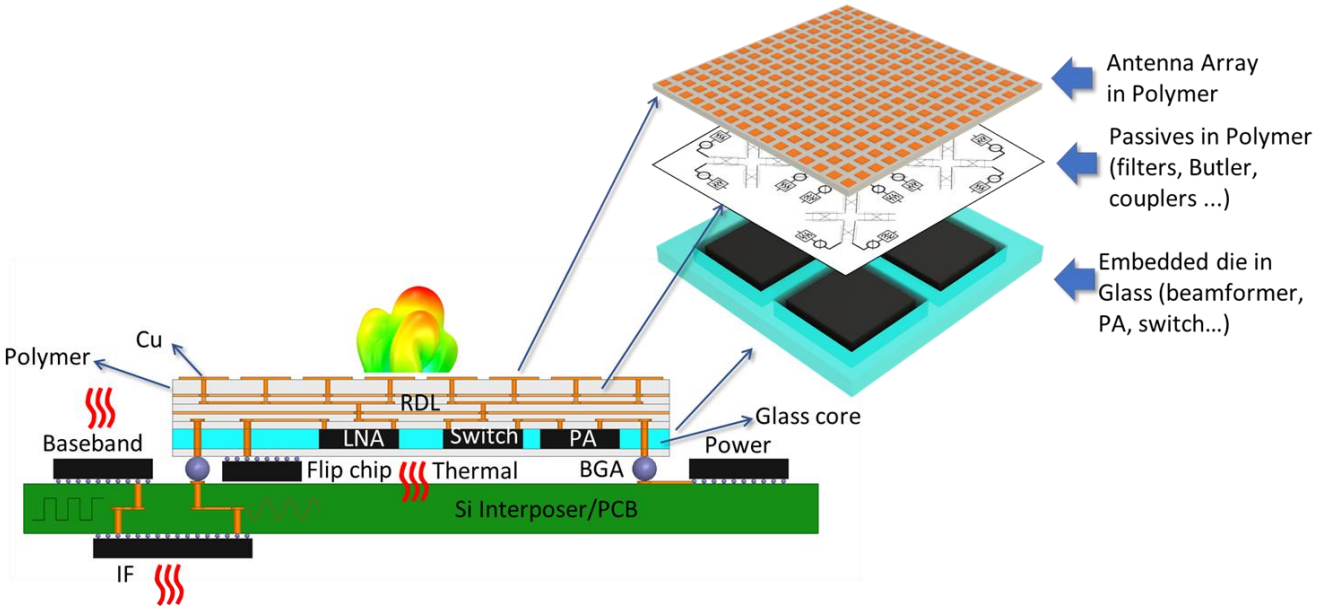
Rx NF
8dB

Courtesy: Adapted from Shahriar Shahramian, Bell Labs – Nokia

Enabling Connectivity @ sub-THz Frequencies

Scalable Antenna Array

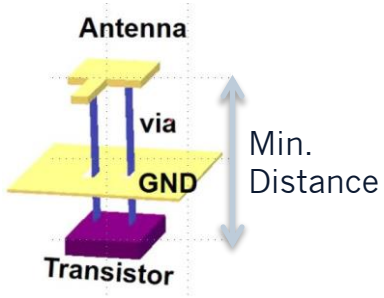


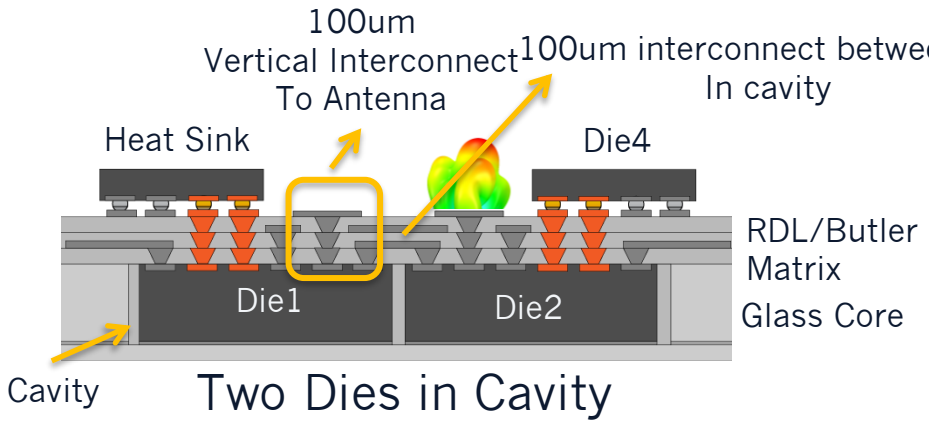


- ❑ λ/2 lattice for Antenna Array and interconnects (AiP)
- ❑ Enough elements to achieve appreciable gain
- ❑ 1dB or less loss between PA output and Antenna Array
- ❑ Efficient heat removal

Panel/Wafer Scale Packaging

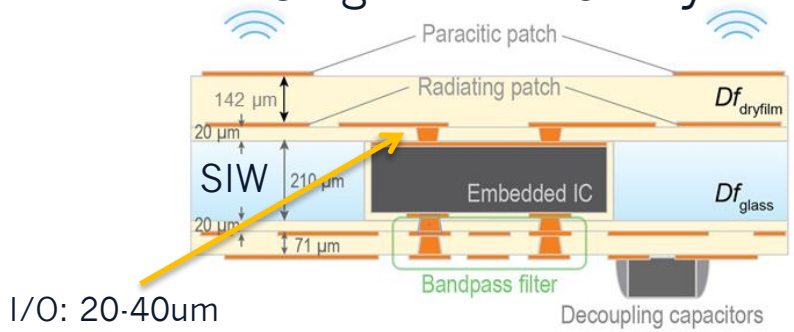
Goal: Ultra-thin 0.5mm-1mm
Thermal 100-200W/cm^2





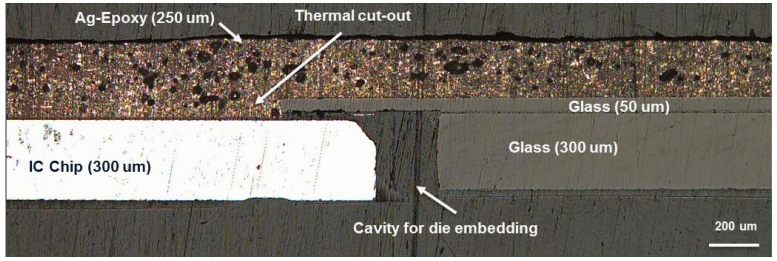
Two Dies in Cavity

Single Die in Cavity

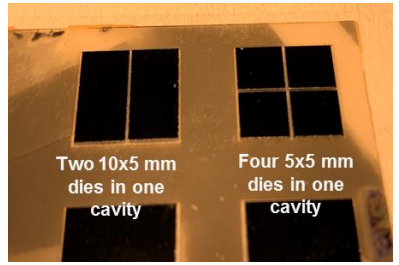


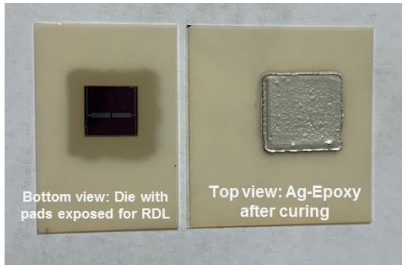
Fan-Out Wafer Level Packaging Comparison

Substrate	eSiFO (Silicon)	TSMC InFO (Epoxy Mold)	This approach (Glass)
Material properties			
Relative dielectric constant (ε_r)	3.9	2.8-3.2	2.5–3.2
Loss tangent × 10^4 (tanδ @ GHz)	10 @ 10	80 @ 58	3-50 @ 10
Surface roughness (nm)	<1	> 1000	<1
CTE (ppm/K)	2.9-4	16-30	3-9
Young's modulus (GPa)	165	22	50-90
Moisture absorption	0	1-2.5%	0
Thermal conductivity (W/m.K)	148	0.5-0.75	1.1



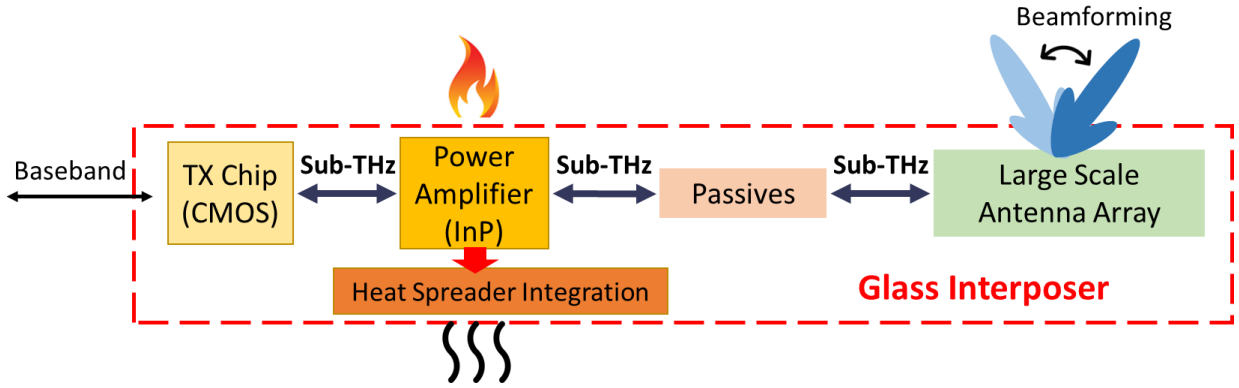
Package parameters			
Interconnect density (IO/mm/layer)	750	125	500
Package size (mm)	35x35	20x20	100x100
Substrate thickness	Thinning	Thinning	Handling
Reliability	Additional PKG	Warpage	CTE Tailored
Panel/Wafer size	300 mm	500 mm^2	710 mm^2

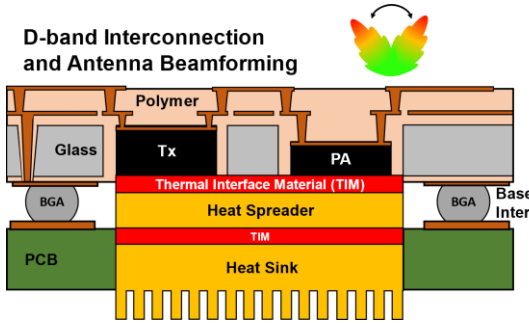


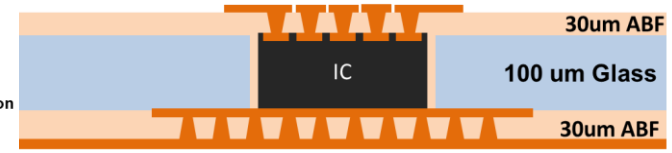


- ❑ Single die or Multiple dies in cavity
- ❑ Minimum Die Shift (2um)
- ❑ No Assembly w/ Fine I/O Pitch (20-40um)
- ❑ Double Sided

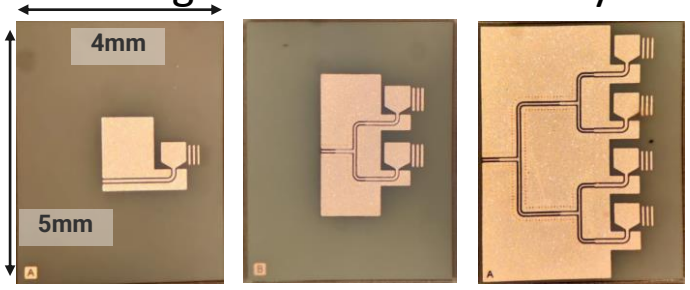
Glass Packaging for 6G Wireless (140GHz): Recent Research Results



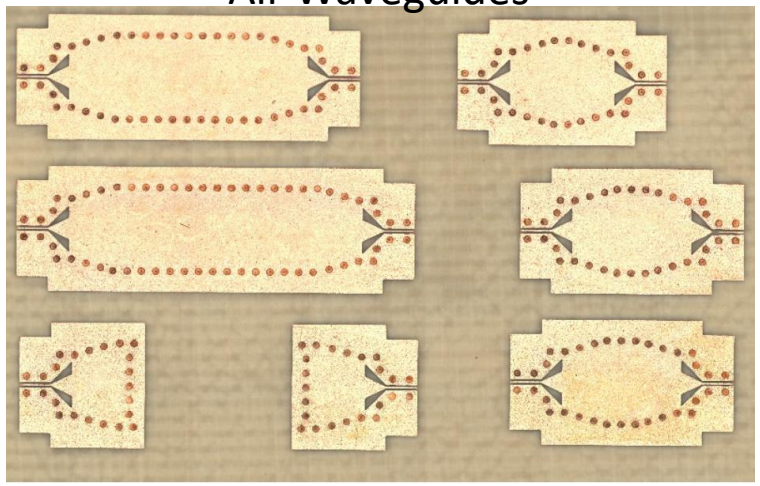




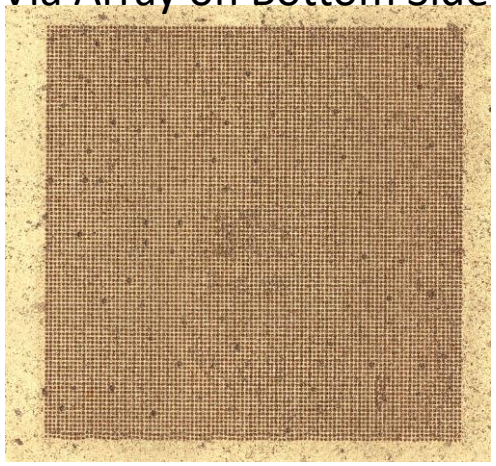
High Gain Antenna Arrays



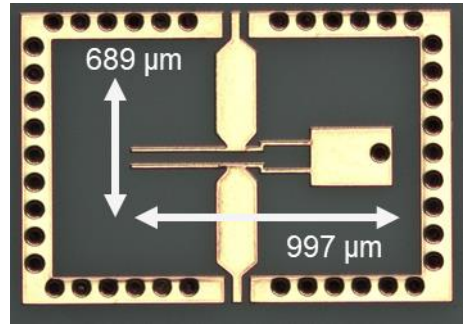
Air Waveguides

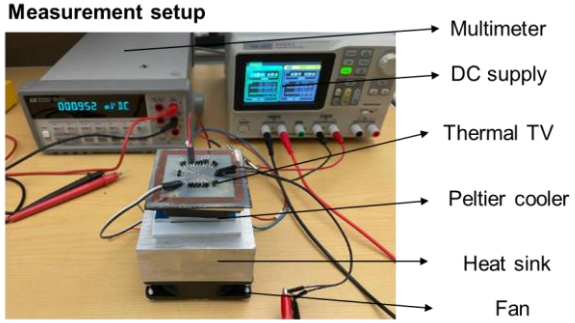


Via Array on Bottom Side



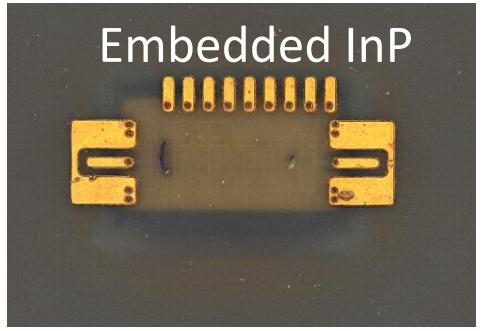
Filters





Thermal

Antenna Array with Embedded CMOS



Translational Research on Glass Packaging - SHIP

Qorvo® Wins U.S. Government Project to Create Advanced, State-of-the-Art, RF Semiconductor Packaging Center

GREENSBORO, NC – November 5, 2020 – Qorvo® (Nasdaq:QRVO), a leading provider of innovative RF solutions that connect the world, has been selected by the U.S. government to create a State-of-the-Art (SOTA) Heterogeneous Integrated Packaging (SHIP) RF production and prototyping center. The SHIP program will ensure that microelectronics packaging expertise and leadership is available for both U.S. defense contractors and commercial clients that require design, validation, assembly, test and manufacturing of next-generation RF components.

The exclusive SHIP Other Transaction Agreement (OTA), worth up to $75 million, was awarded to Qorvo by the Naval Surface Warfare Center (NSWC), Crane Division. This program is funded by the Office of the Undersecretary of Defense for Research and Engineering's (OUSD R&E) Trusted and Assured Microelectronics Program (T&AM), and is administered by the Strategic & Spectrum Missions Advanced Resilient Trusted System (S²MARTS) Other Transaction Agreement (OTA), managed by National Security Technology Accelerator (NSTXL).

Under the SHIP program, Qorvo will design and deliver the highest levels of heterogeneous packaging integration. This is essential to meet the size, weight, power and cost (SWAP-C) requirements for next-generation phased array radar systems, unmanned vehicles, electronic warfare platforms and satellite communications.

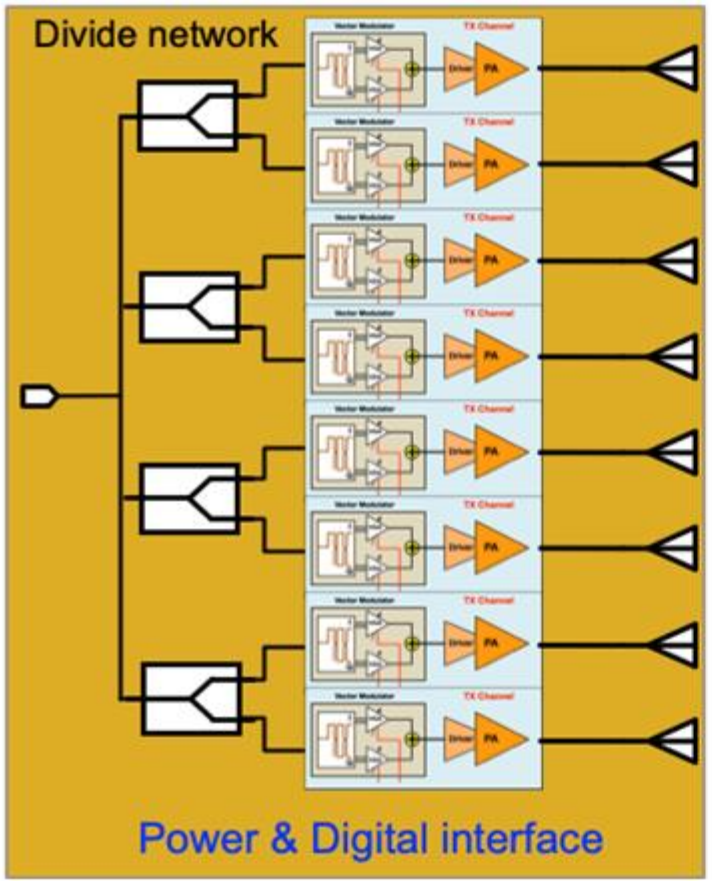
James Klein, president of Qorvo Infrastructure and Defense Products, said, "We are honored to be selected to establish state-of-the-art RF packaging capability for the U.S. Department of Defense (DoD). This award reflects Qorvo's proven track record as a global leader in RF technology with over 35 years of experience. As part of this collaboration, Qorvo will expand its proven capabilities in Texas to create a SOTA facility that best serves the needs of the U.S. government and commercial customers."

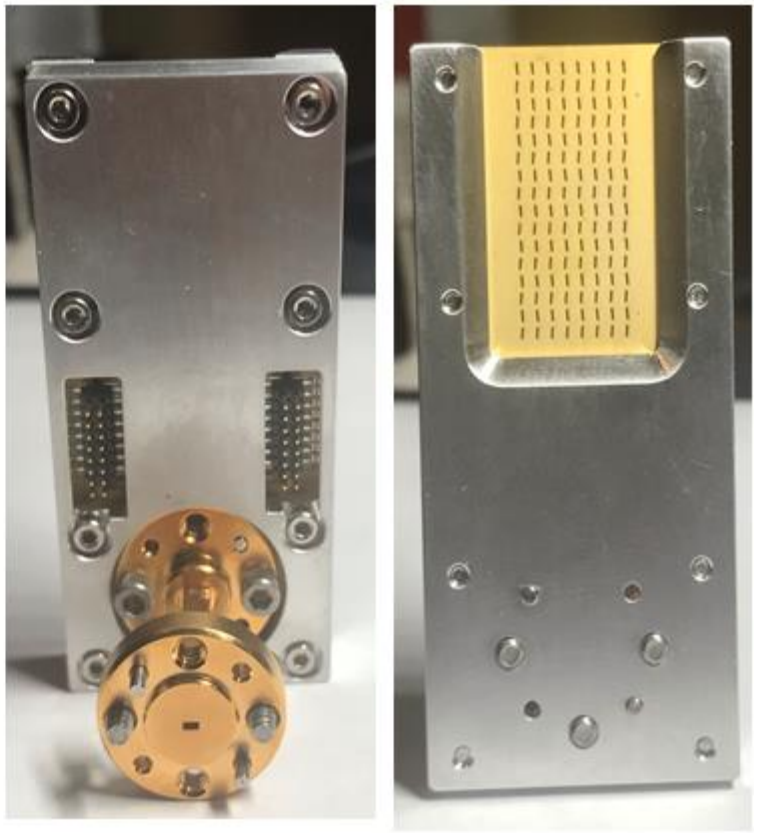
Qorvo's U.S.-based capabilities include advanced manufacturing, packaging and testing for both high- and low-power applications ranging from DC to

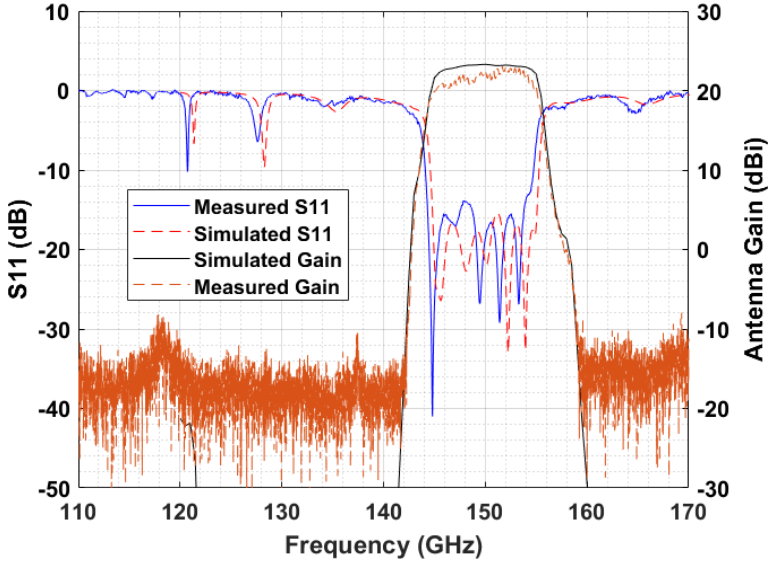
- Qorvo wins SHIP RF Center
  - $75M from US Government
  - GT-PRC will focus on **Glass Based Advanced Packaging** for RF (Dates: June 2022 – May 2024)

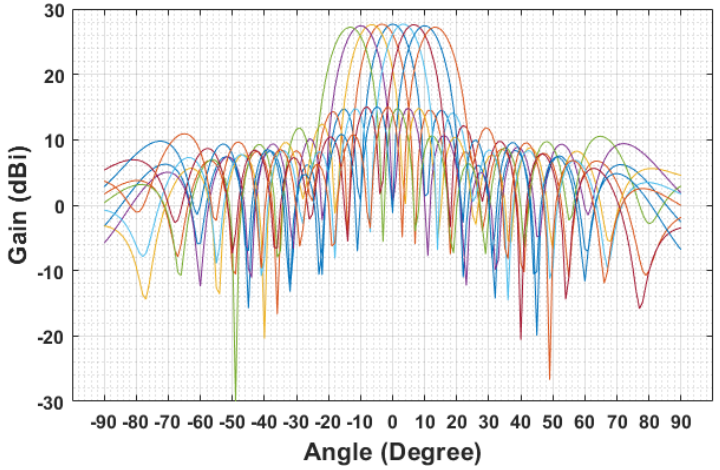
https://www.qorvo.com/newsroom/news/2020/qorvo-wins-us-gov-project-to-create-advanced-state-of-the-art-rf-semiconductor-packaging-center

Radio on Glass Module Prototype (128 Element Linear Array)







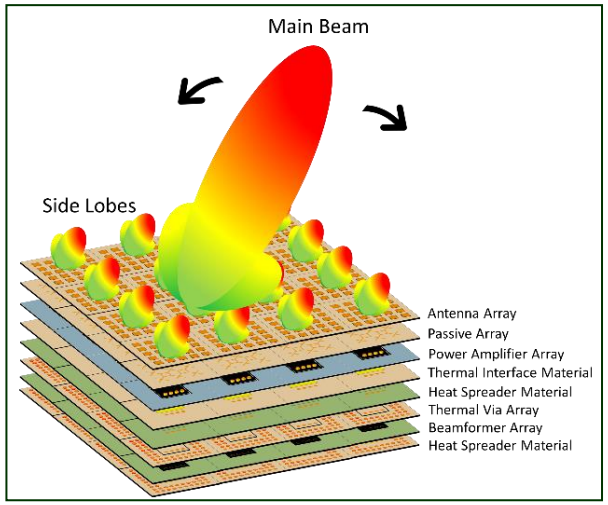


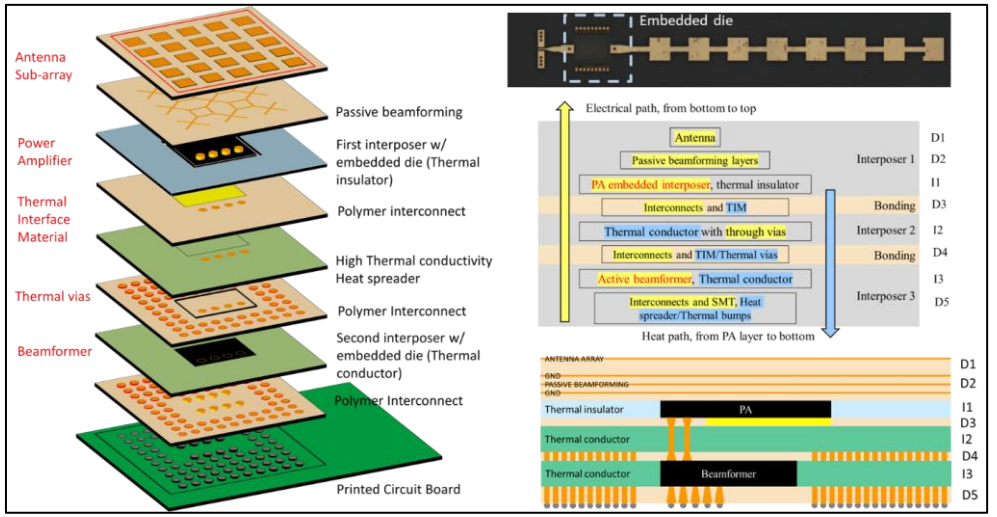
- ❑ 16 Slot Antenna Array w/ WR-6 Waveguide Interface
- ❑ 3D Glass Solutions & Nokia Wireless

M. Elkhouly et al. RFIC 2020

10 Year Metric Vs SOTA

Metric & Drivers	Metric (10 Years)	State of the Art (SOTA)
Electrical IC Parallelism & Volume Scaling (AI, DC, M)	IO density 16M/mm^2	IO density 10K/mm^2
	BW Density > 500Tbps/mm^2; <0.01 pJ/bit	BW density 28Tbps/mm^2; 0.021 pJ/bit (ARM/GT IEDM 2020)
Cooling & Power Delivery (S, C, H, AI)	Power 1000W; Current density 2–5A/mm^2; Efficiency >80% (HIR 10 year)	Power 400W; Current Density 1A/mm2; Efficiency <70%
	Current 50 KAmps; Power 50kW; PDN Power <1KW (2%); Efficiency>80%	Current 18 KAmps; Power 10KW; PDN 5KW (33%); η <67% (Tesla Dojo)
Wireless IC & I/O (C, S, H)	Insertion Loss <1dB (PA output to Antenna input) @ 0.3 – 1THz; DARPA ELGAR 1dB	Insertion Loss >5dB in D-Band (110-170 GHz) (ComSenTer)
	Antenna efficiency >90% @ 0.3–1THz	Antenna efficiency >90% (< 100GHz)
	SNR 30dB (128 QAM)	SNR 20dB (128 QAM) D-Band
Photonic/Optic IC and Chiplet Communication (AI, C, DC)	Coupling loss < 0.9dB; Misalignment; +/−1mm	Coupling Loss ~ 1dB (O-Band)
	100 (Tbps/mm)/(pJ/bit) (link-level)	1 (Tbps/mm)/(pJ/bit) (DARPA PIPES)
	Bandwidth (BW) Reconfigurable ICs between chiplets; 0.5-5Tbps aggregated BW	NA
	Optical gain/laser integration via photonic wire bonds (PWB) and/or mono-int. (DARPA LUMOS)	Laser is off-chip → requiring packaging (costly & not reliable)
Reconfigurable Circuits & Modules (AI, S, DC)	100 TOP/J, 1ns latency, infinite bit-resolution MAC ops (DOD Labs e.g., AFRL, ARL)	<5 TOP/J, 1000+ns latency, 4-12 bit
	AI accelerator: 10–100 fJ/MAC, 1–50 TMACs/mm^2, 1ns–25 ps operation (Google X)	0.5–1 pJ/MAC, 0.5–1 TMAC/s/mm^2, 0.5–1 GMVM/s, and 1–2 us per MVM
Active & Passive Devices for Heterogeneous Integration (C, S, DC)	EO Modulator: ER > 12dB; BW > 15GHz per channel; (next Gen AIM Photonics components)	NA
	Interposer Waveguides; losses < 0.1dB/cm	1.5dB/cm
	Interposer Filters for WDM: filter sharpness > 15dB over < 0.2nm BW (AIM Photonics Foundry)	NA

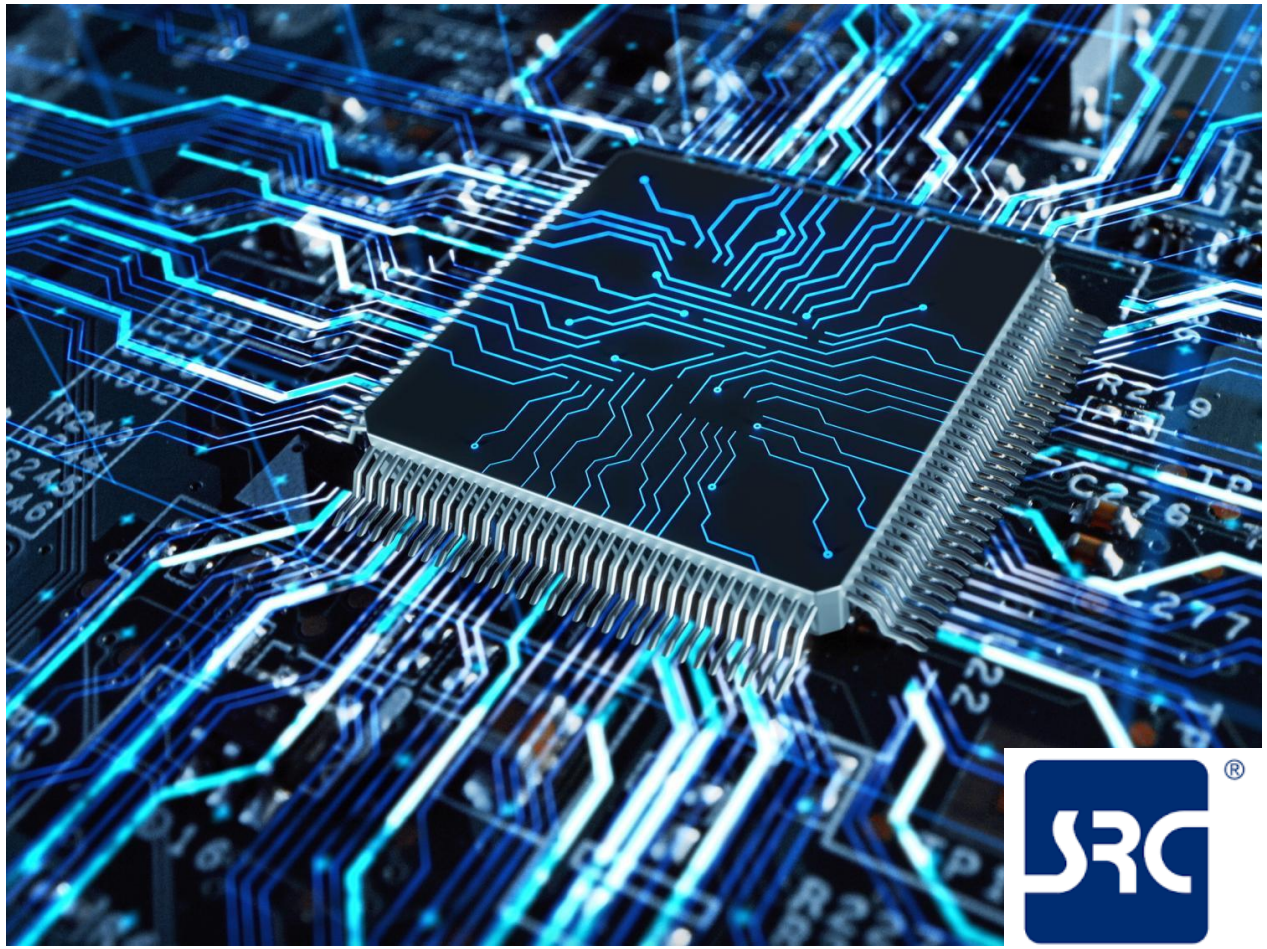




www.chimes.psu.edu

JUMP 2.0 Center @ Penn State (14 Univ. Partners)

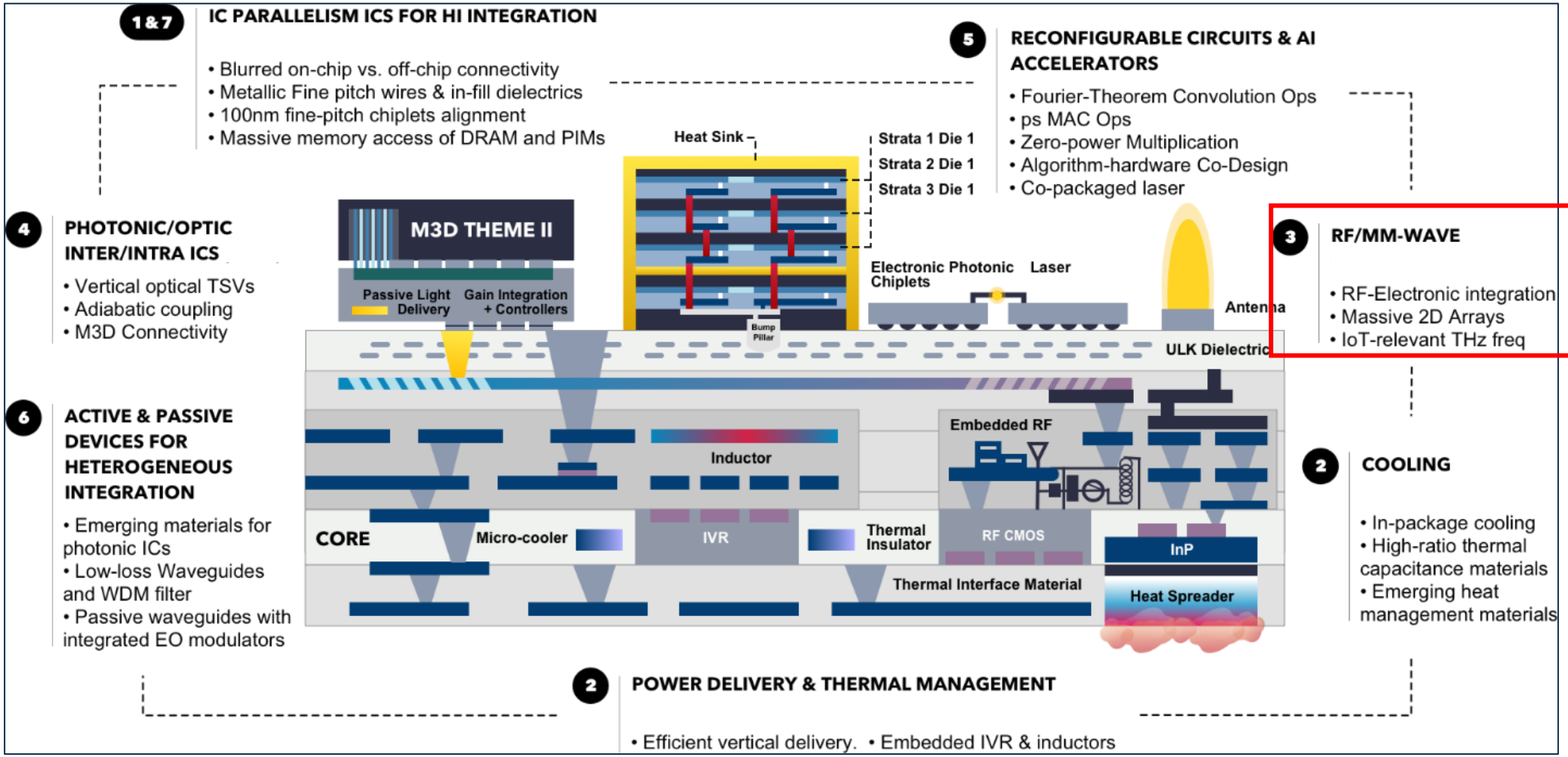
Penn State leads semiconductor packaging, heterogeneous integration center



- Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES)
- Supported by the Semiconductor Research Corporation (SRC)'s Joint University Microelectronics Program 2.0 (JUMP 2.0), a consortium of industrial partners in cooperation with the Defense Advanced Research Projects Agency (DARPA)

https://www.psu.edu/news/engineering/story/penn-state-leads-semiconductor-packaging-heterogeneous-integration-center/

Ultra-dense Heterogeneous Integration Platform – Next 10 Years



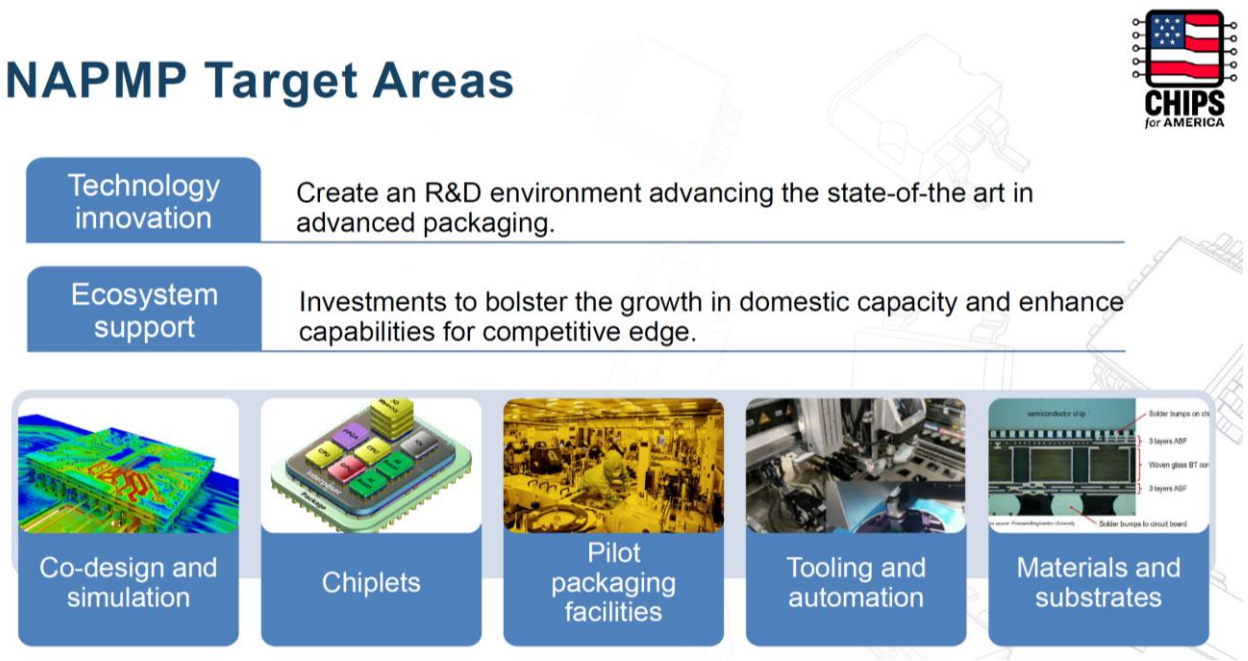
CHIPS Act ….

- Opportunities for packaging through CHIPS Act:
  - National Semiconductor Technology Center (NSTC)
    - Includes packaging but unclear up to what extent.
  - **National Advanced Packaging Manufacturing Program (NAPMP)**
  - **Manufacturing USA Institutes** (3 Institutes)

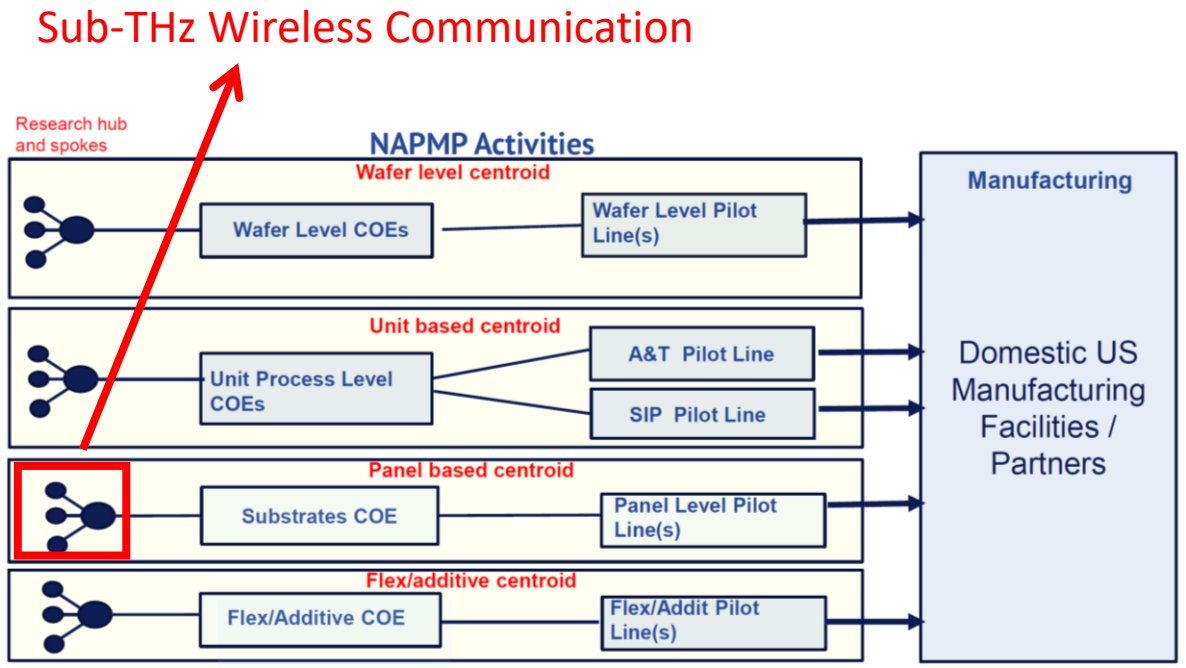
		YEAR 1	YEAR 2	YEAR 3	YEAR 4	YEAR 5	
9906(c)	NSTC	$2B	$2B	$1.3B	$1.1B	1.6B	-
9906(d)	NAPMP	$2.5B					
9906(e)	NIST Metrology	$500M					
9906(f)	Manufacturing USA Institute						

National Advanced Packaging Manufacturing Program (NAPMP)

1. IBM (www.asicoalition.org) is expected to lead a major coalition
   - Hub & Spoke model being proposed feeding into pilot lines and manufacturing facilities
2. Possible University Center of Excellence (UCE) hub on Panel Scale Packaging (TRL 1-3)
   - Sub-THz Advanced Communication



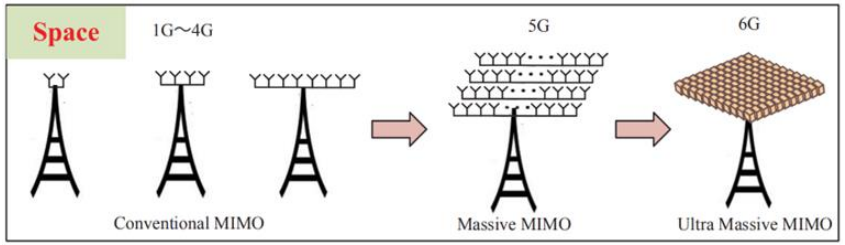
Source: Eric Lin, Interim Director, CHIPS Research and Development Office, NIST

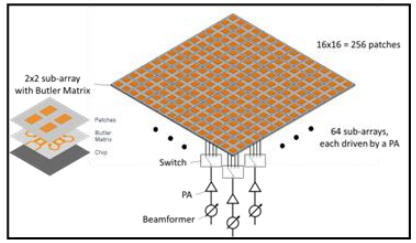


www.asicoalition.org *Courtesy: Scott Sikorski, IBM*

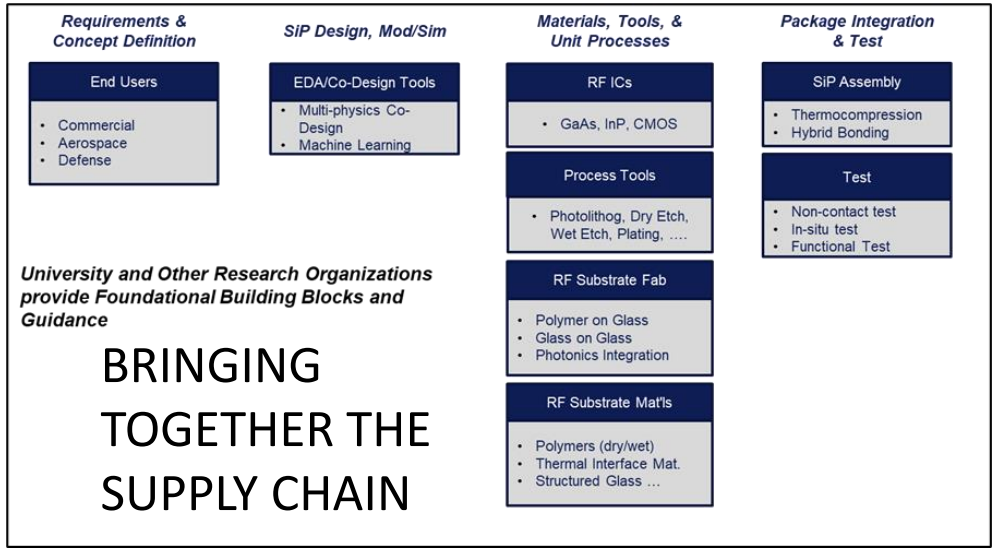
Manufacturing USA Institute on Glass Packaging

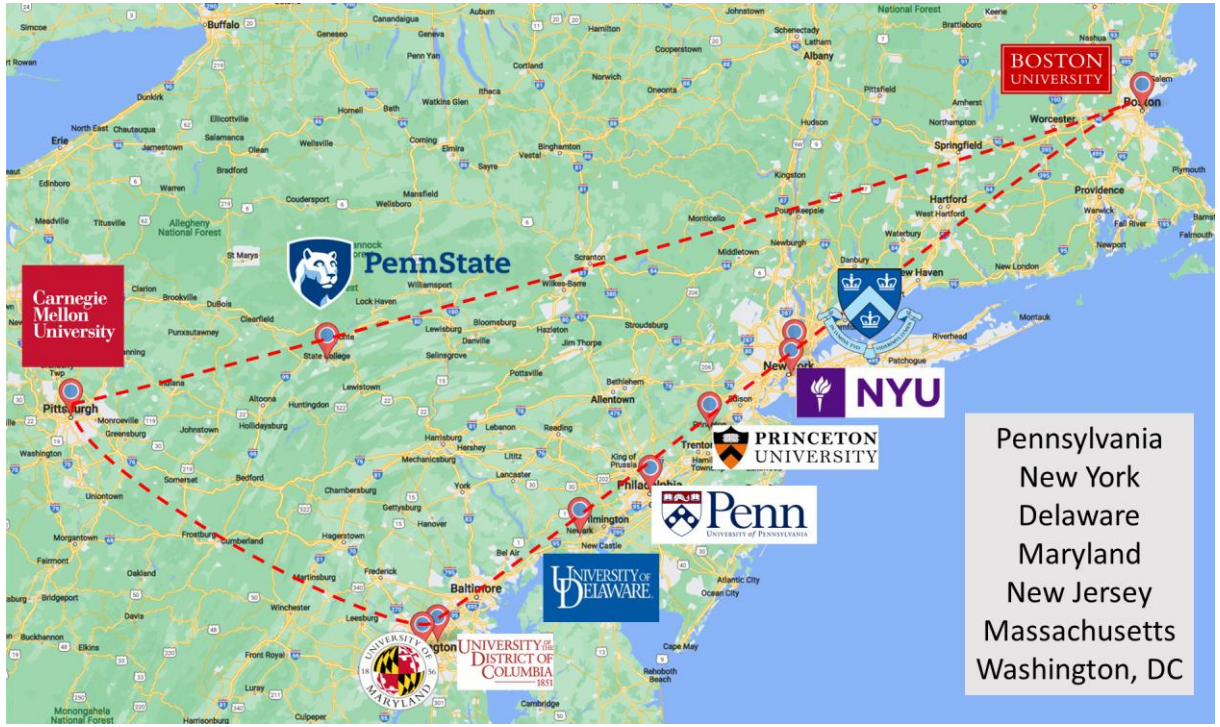
- ❑ Institute Focused on Advanced Packaging for Advanced Communications (TRL 4-7)
- ❑ Request for Information (RFI) submitted to NIST (https://www.regulations.gov/comment/NIST-2022-0002-0069 Total submissions=94)
- ❑ Partner universities from the Mid-Atlantic HUB
- ❑ Focus on Wafer Level Glass Packaging (Research from UCE transitioned into prototyping)





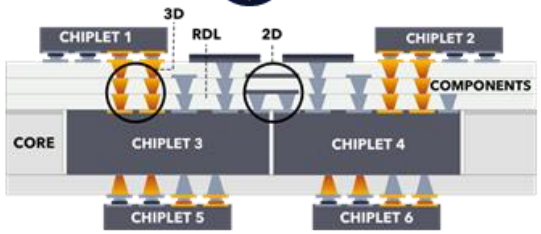
- Penn State
- GaTech
- Qorvo
- 3DGS
- AMAT
- Schott
- Menlo
- Corning
- Synopsys
- iNEMI
- Boeing
- Absolics
- GWU





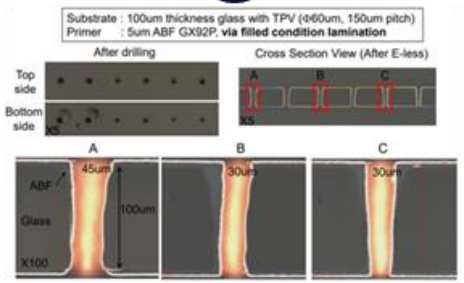
Manf. USA Institute – What needs to happen ….

1



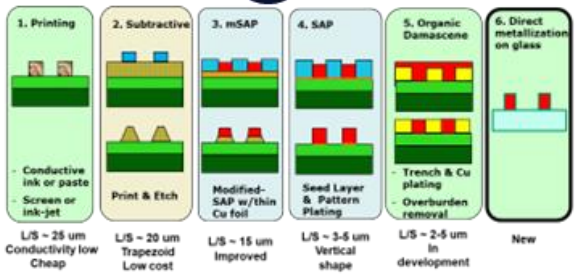
- Glass core substrates: Surface roughness, CTE, modulus, moisture absorption like Si but dielectric insulator and large area (500mm) to reduce cost.

2



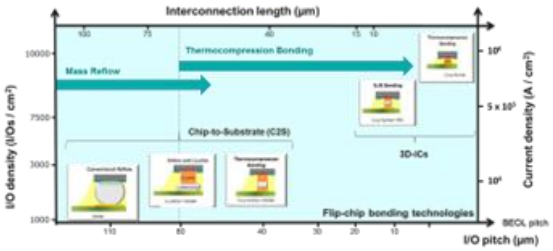
- 10um/20um pitch through core vias with 20:1 aspect ratio

3



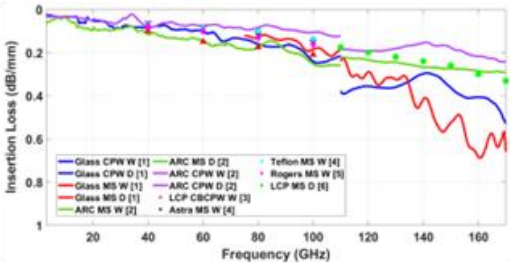
- 10um L/S (mmWave)
- 8+ Metal Layers
- 1um L/S with good adhesion (mixed signal)

4



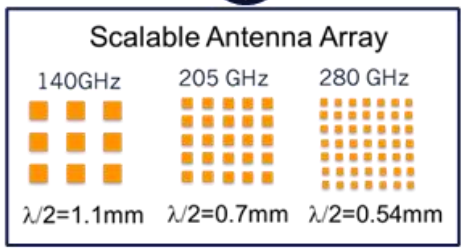
- 35um C2S (mmWave)
- <10um assembly pitch C2S (mixed signal)
- No cracking or delamination

5



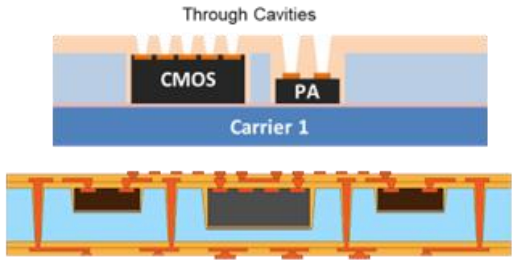
- Low Dk (3.0), Low Df (10^{-4}) dielectrics; 5-100 um thick
- Air Dielectrics

6



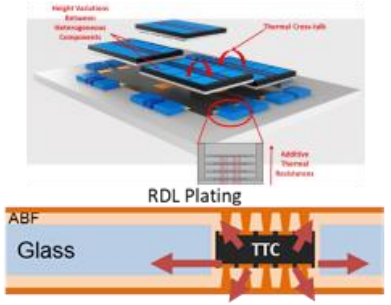
- Antenna in Package
- Patch/Slot antennas
- Base station / Handset

7



- Through & Blind Cavities
- CMOS/InP 75-150um die thickness
- <1dB loss

8



- Thermal Insulator (1W/mK)
- Thermal Mgmt (>400W/mK)

9

End User
EDA Optimization
Substrate
Assembly & Test
Equipment Manf.
Materials

- Supply Chain Eco-system needs to come together

Courtesy: SIP RF Team, ASIC


Thank
You
Merci
Obrigado
Asante
Multumesc
Arigato
Vinaka
Spasibo
Maake
Grazie
Kiitos
Welalin
Matondo
Juspaxar
Mamana
Dank Je
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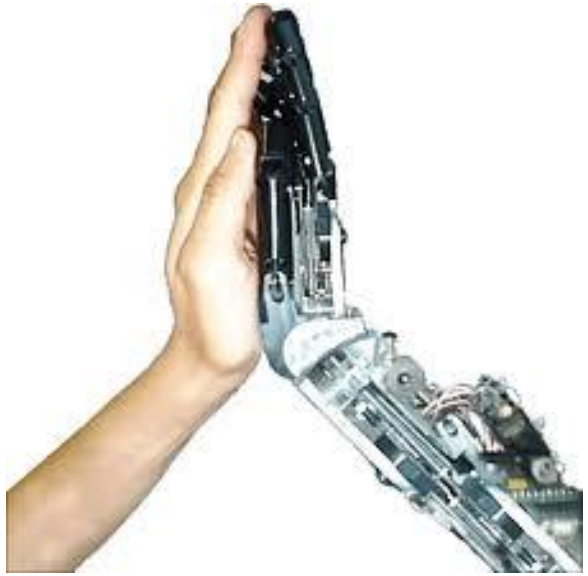
Chokrane
Cam on ban
Terma Kasih
Mochchakkeram
Ua Tsaug Rau Koj



NAMASTÉ