Advanced Packaging Materials and Open Innovation at Resonac

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Resonac Corporation

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Today's Presentation

RESONAC

1. Corporate Introduction
2. Introduction of Packaging Solution Center & JOINT2
3. R&D Status for Advanced Package

January 2023: Resonac was born

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Showa Denko

Showa Denko Materials
(Former Hitachi Chemical)

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Chemistry for Change

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Corporate introduction - Net Sales

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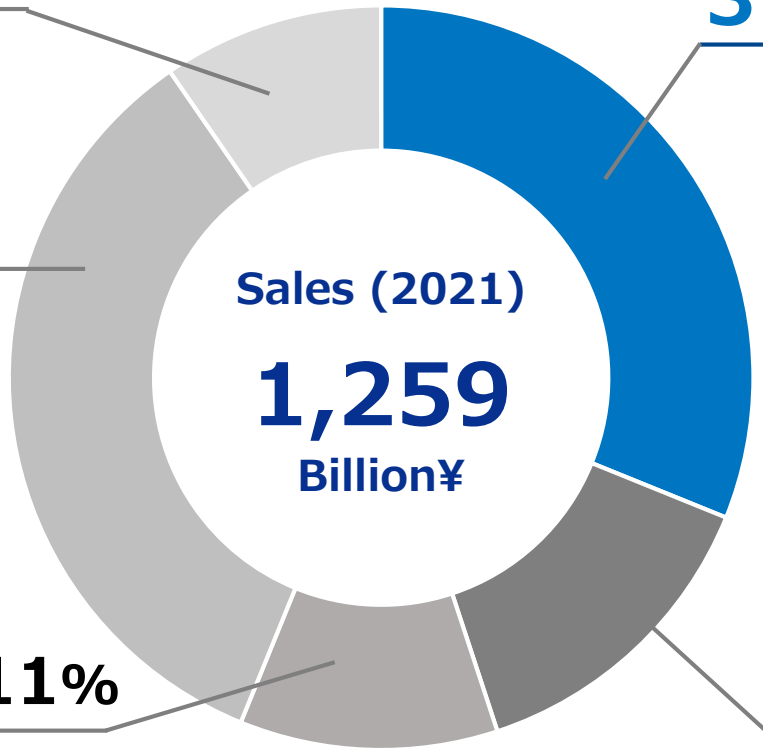
Semi conductor and Electronics materials 31% (392 Billion¥)

1. High purity Gas for semiconductor
2. CMP slurry
3. Epoxy molding compound
4. Die bonding material
5. Cupper clad laminate
6. Photosensibity film
7. Photosensibity solder mask
8. Hard disc
9. SiC epitaxial wafer
10. Composite semiconductor (LED)



Other 10%

Life science products etc.

Chemical 34%

Petroleum chemistry
Chemicals
Graphite electrode

Innovation material 11%

High-functionary chemicals
High-performance resin
Coating material , Ceramics ,
Aluminium functional component

Mobility 14%

Automobile component
Lithium-ion battery material

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Top Company in Semiconductor related Materials

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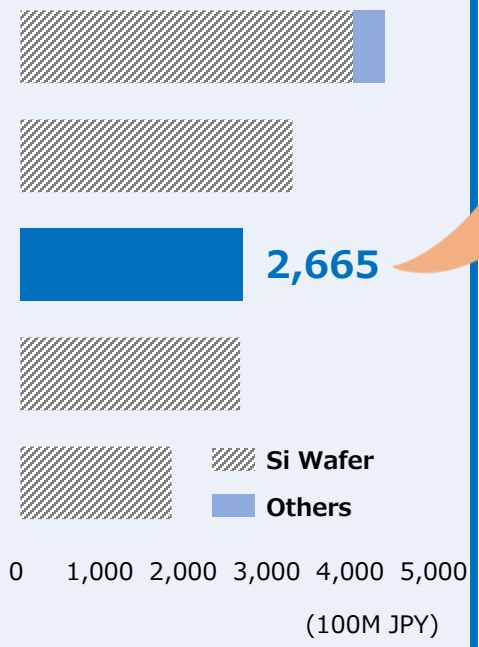
Top Share in Back–End Process

Global Players and Sales in Semiconductor related Materials(2021)

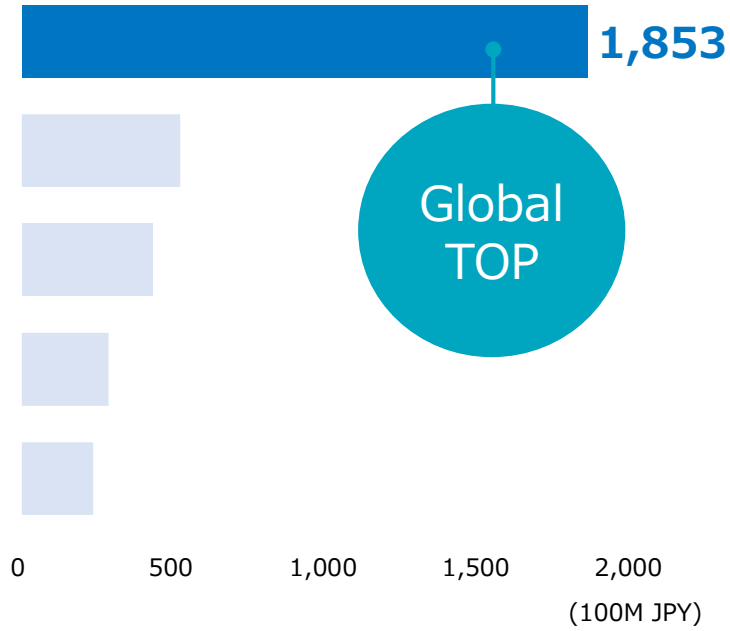
Company	Main Products
A	Si Wafer
B	Si Wafer
RESONAC	High Purity Gases, CMP, Back-End Materials
C	Si Wafer
D	Si Wafer



Source : Showa Denko's original survey

Materials for Back-End Process

Company	Main Products
RESONAC	CCL (No.1) DAF (No.1) DFR (No.1) EMC (No.2)
G	CCL for PKG
K	CCL, EMC, DAF, Photosensitive Materials
L	CCL for PKG
M	CCL for PKG EMC



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Materials Line-Up for Semiconductor PKG

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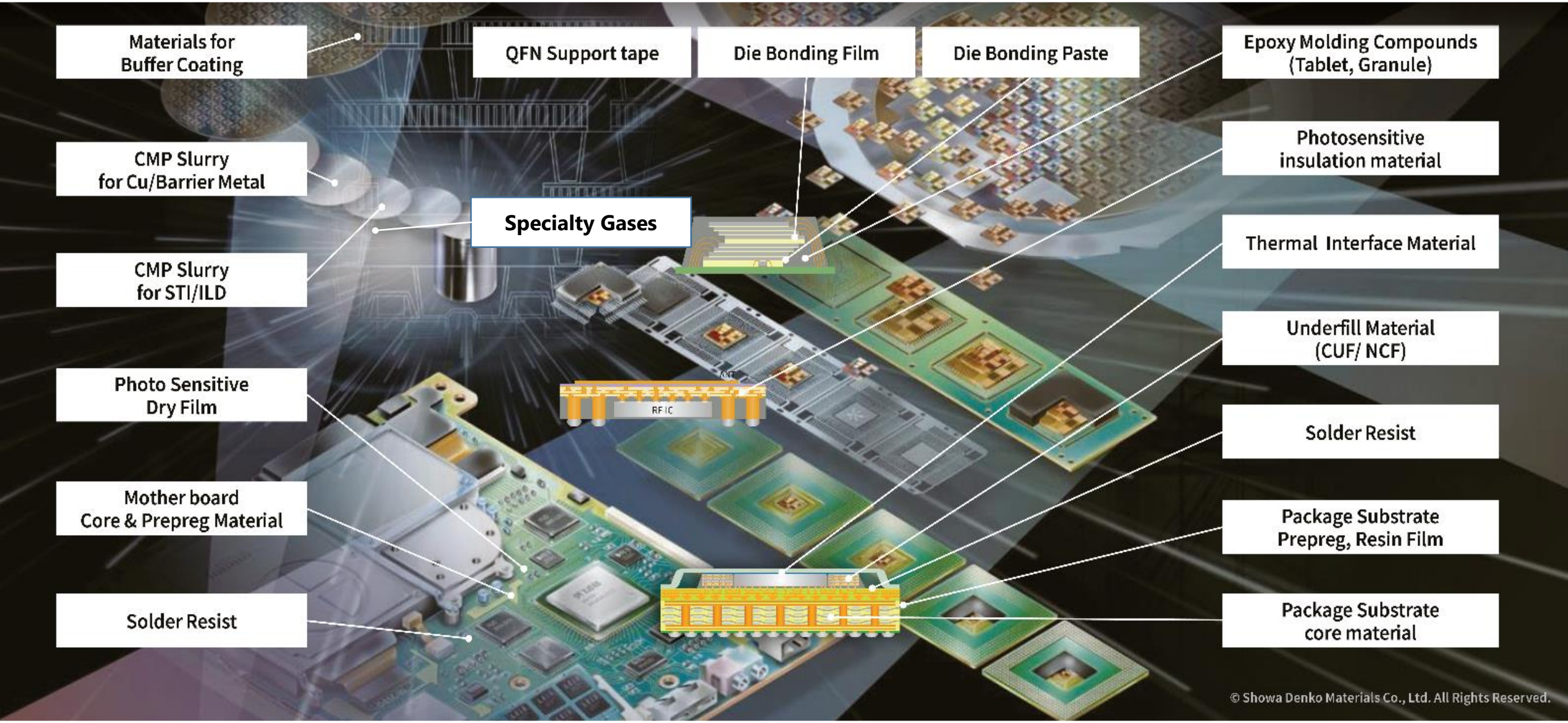

Packaging Solution Center (PSC)

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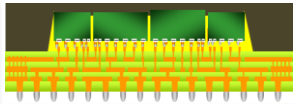
Packaging Solution Center is located on the **3rd and 4th floor in Kawasaki-city, Kanagawa-pref.**

Total floor area: 7,000 m²

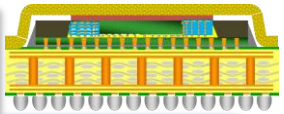
[Strong point of PSC]

- Global top for packaging R&D site
- Long term experience of PKG assembly and reliability evaluation (over 28 years)
- Deep knowledge of assembly evaluation
- Through integrated Assembly Line
- Combination and control of materials

JOINT1 : FO-WLP & PLP



JOINT2 : 2.xD & 3D



[Through collaboration]

- Many experiences and results through Open Innovation
- Many connections among material and equipment suppliers.

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Function & Target of PSC

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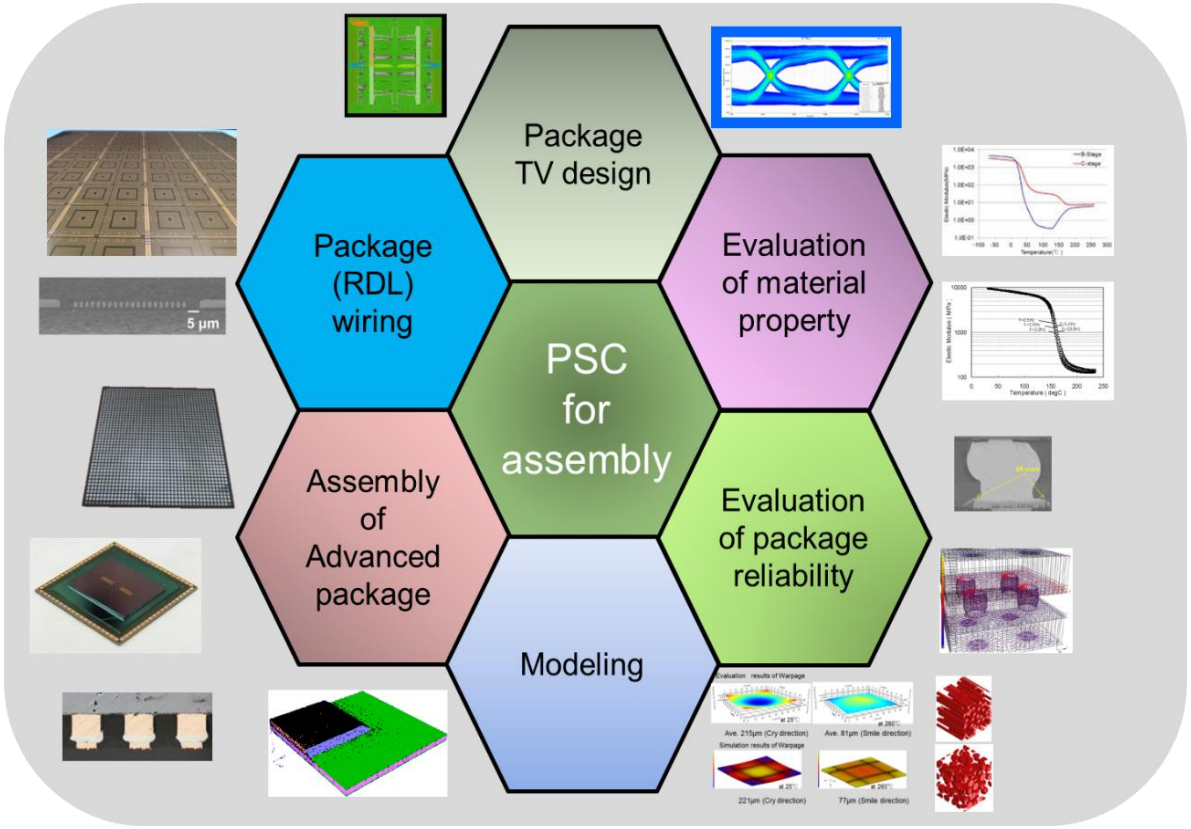
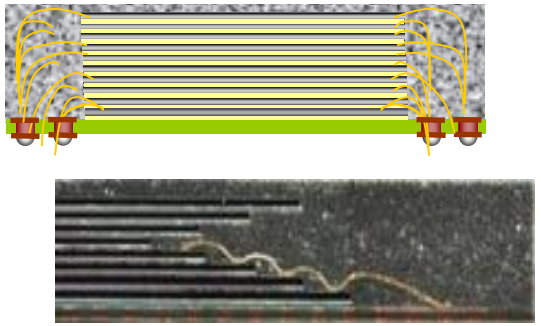
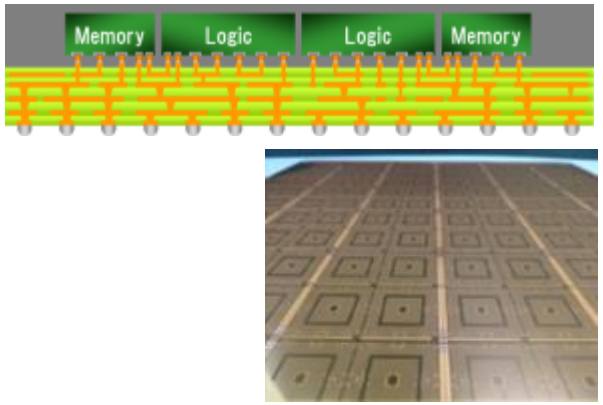


Function of PSC

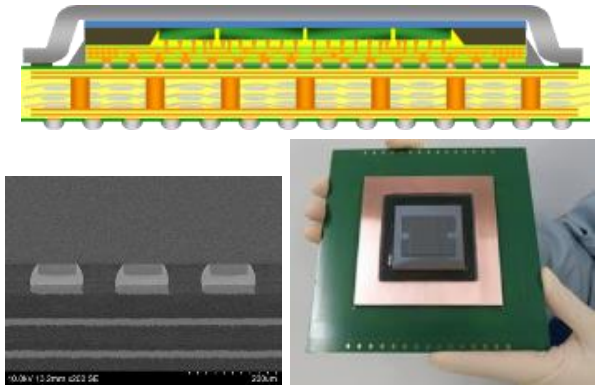
Memory



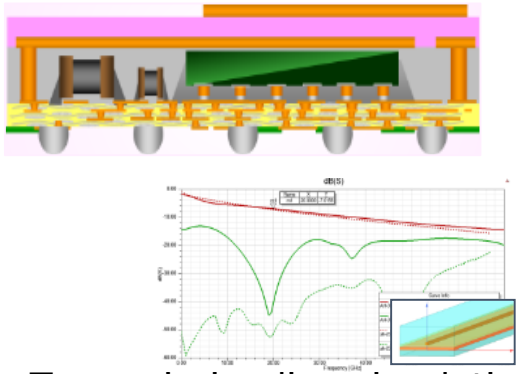
FO-WLP/PLP



2.xD/3D



AiP/ RFFE



Transmission line simulation

Regardless of the collaboration type,
all activities are operated with utilizing PSC' key functions.

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3rd Floor layout

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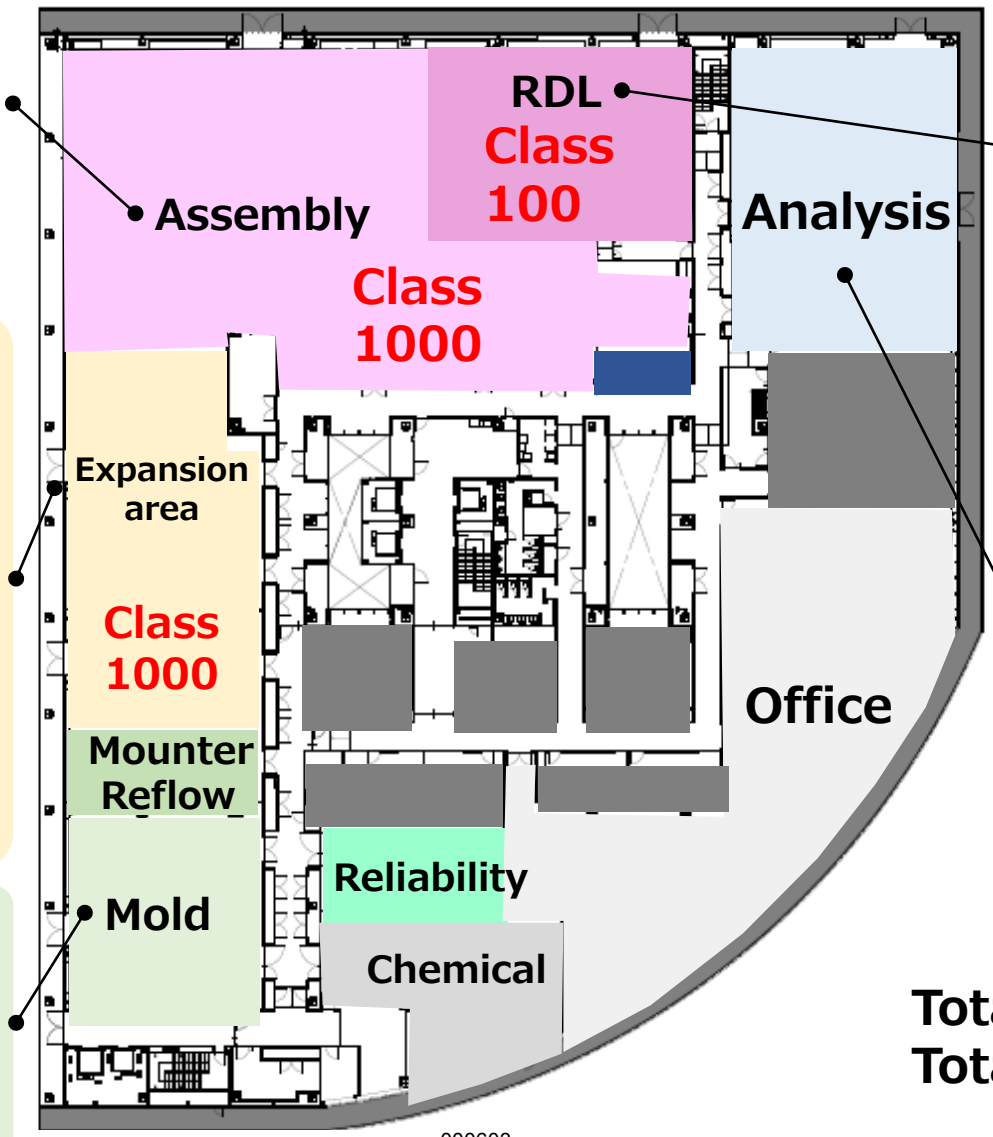
In **Assembly** area
- ✓ Grinder
- ✓ Blade & Laser Dicer
- ✓ CoC, CoW flip chip bonder
- ✓ Laminator
- ✓ Plating

In **expansion** area
- ✓ C2W bonder
- ✓ Plasma asher
- ✓ Large die mounter
- ✓ Panel CMP
- ✓ Temporary bonder & debonder
- ✓ Compression molding
- ✓ C2W bonder
- ✓ Panel Grinder
- ✓ Panel Su/Ag plating

In **Mold** area
- ✓ Transfer
- ✓ Substrate Comp.
- ✓ Wafer Comp.
- ✓ Panel Comp.



In **RDL** area
- ✓ Spin coater
- ✓ Slit coater
- ✓ Vacuum Dryer
- ✓ Stepper
- ✓ Developer
- ✓ Sputter

In **Analysis** area
- ✓ FE-SEM-EDX
- ✓ SAT
- ✓ 3D measurement
- ✓ FIB
- ✓ X-ray CT
- ✓ Shadow moiré
- ✓ Stylus profiler
- ✓ Probe tester
- ✓ Laser decapsulator

Total floor area: 4,200 m²
Total clean room: 1,450 m²

Co-Creative R&D Platform

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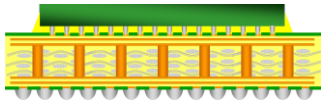
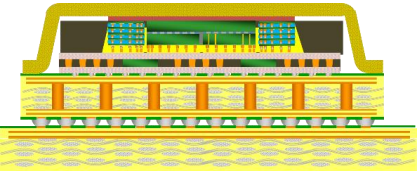
PKG structure	Test Vehicle		
 QFP	Easy	1~2 combined materials	Single R&D Division can cover
 FC-BGA	Challenging	4~5 combined evaluation	**Package Solution Center/PSC** *Combination of Internal Knowledge
 2.xD&3D	Too complicated	More than 10 combination	**JOINT2** *Need knowledge from External Collaborator

New consortium "JOINT2" for

1. **unifying contact** of each equipment & material companies to customer.
2. creating and increasing opportunity of **discussion among equipment & material companies**.
3. building **advanced PKG test vehicle**.

We hope these activities accelerate Customer's R&D and expand our material business.

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Be a leader in semiconductor technology innovation

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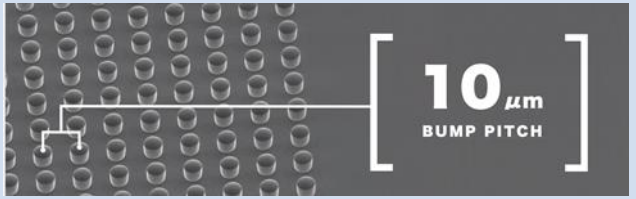
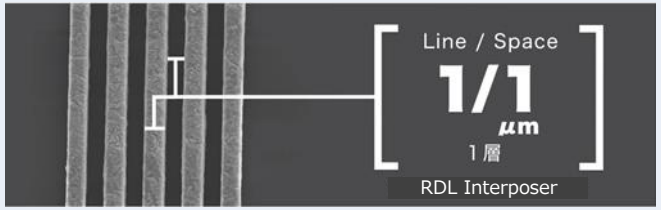
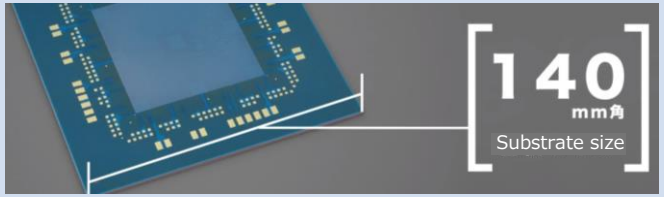
“Open innovation platform” evolve to “Consortiums with multiple company”

JOINT2 ADVANCED PACKAGE EVALUATION PLATFORM

RESONAC, Eat Well, Live Well. Ajinomoto, YAMAHA YAMAHA ROBOTICS HOLDINGS CO., LTD., DNP, UYEMURA, DISCO, JOINT2, tok, SHINKO, EBARA, MMEC, NAMICS, Panasonic CONNECT

Multiple working groups × Mutual utilization of technology and information

Working Group	Program
WG-A	**Fine bump interconnection** 
WG-B	**Fine circuitry interconnection** 
WG-C	**High reliability large package** 

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Back-end Process & "JOINT2" Partner

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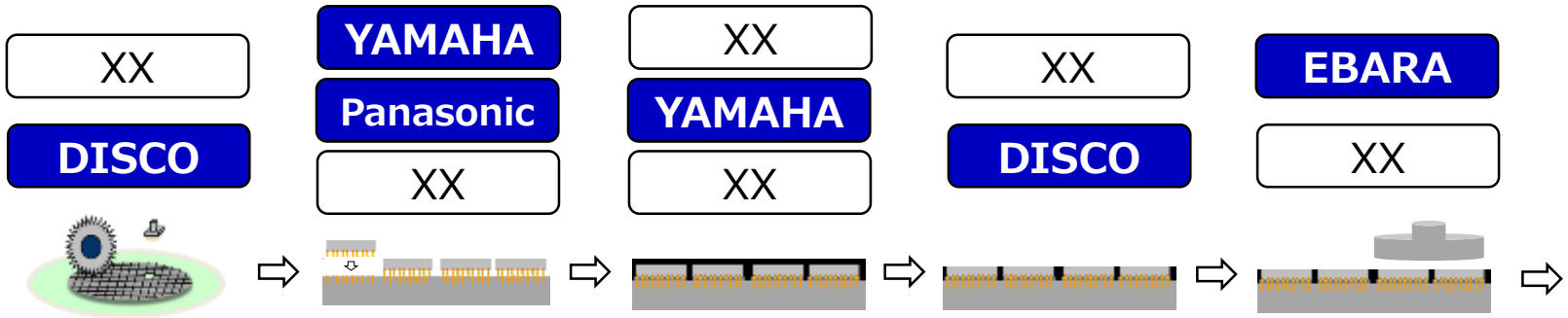
JOINT2 is unparalleled scale consortium with high market share companies for Back-end Process



* Under discussion to join

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Technical roadmap and schedule

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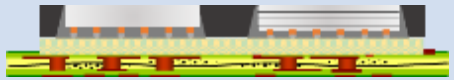
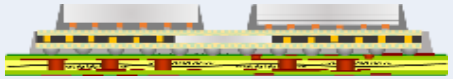
Evaluation item	2021	2022	2023	2024	2025	2026
[WG-A] Fine Bump Interconnect 2.5D  2.1D 	Bump pitch ≦ 20 µm(2.5D), 40 µm(2.1D) Substrate TTV ≦ 10 µm		Bump pitch ≦ 15 µm(2.5D), 30 µm(2.1D) Substrate TTV ≦ 5 µm		Bump pitch ≦ 10 µm(2.5D), 20 µm(2.1D) Substrate TTV ≦ 3 µm	
[WG-B] Fine Circuitry Interconnection  RDL Interposer  Chip Embedded Interposer	L/S ≦ 2/2 µm Single layer Process development	L/S ≦ 2/2 µm Multi layers	L/S ≦ 1.5/1.5 Multi layers Process development L/S ≦ 10/10 µm	L/S ≦ 1.2/1.2 Multi layers	L/S ≦ 1/1 µm Multi layers Process development L/S ≦ 5/5 µm	
[WG-C] High Reliability Large Package 2.xD 	Chip-let size ≧ 20 mm Substrate size ≧ 100 mm	Chip-let size ≧ 35 mm Substrate size ≧ 120 mm		Chip-let size ≧ 50 mm Substrate size ≧ 140 mm		

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Fine Bump Interconnection

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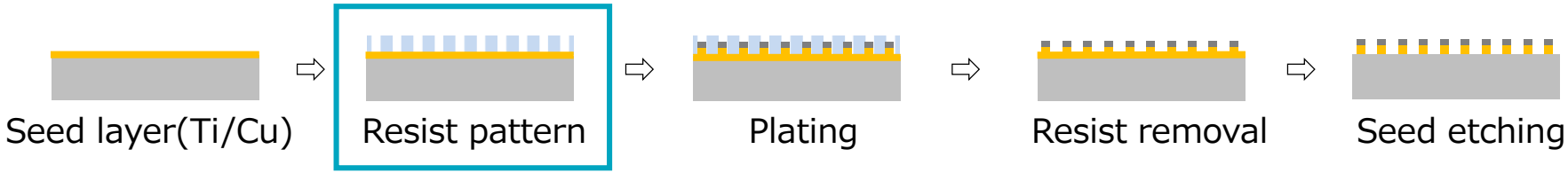
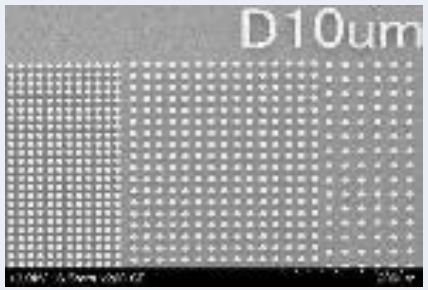
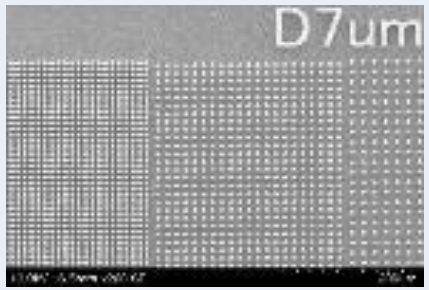
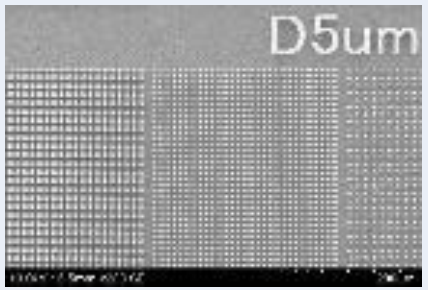


TOK(Resist) **+ Uyemura(Plating)**

Diameter	Φ10 μm (20 μm Pitch)	Φ7 μm (14 μm Pitch)	Φ5 μm (10 μm Pitch)
Resist pattern			
	No residue		
Bump fabrication			
	No missing bump		

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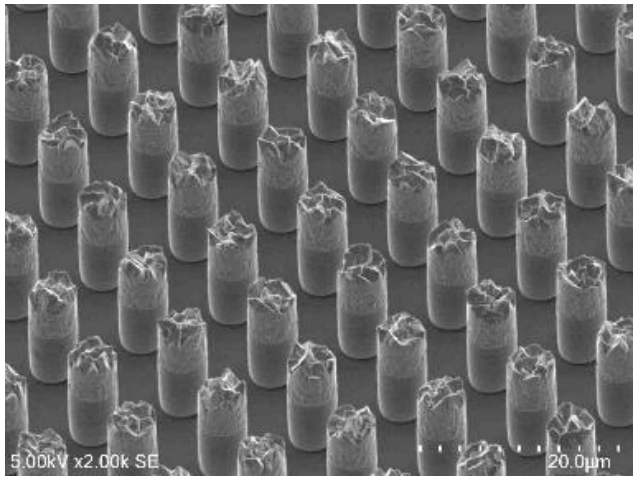
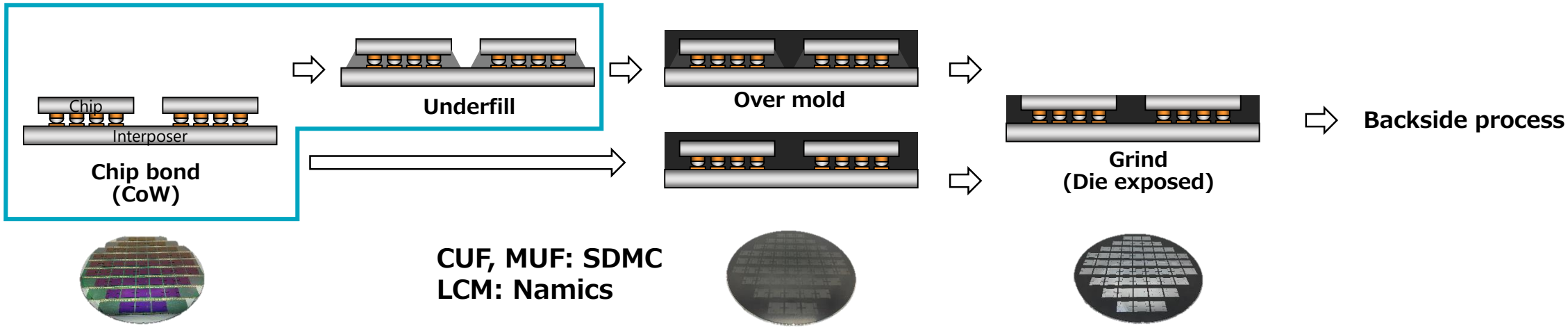
SEM image

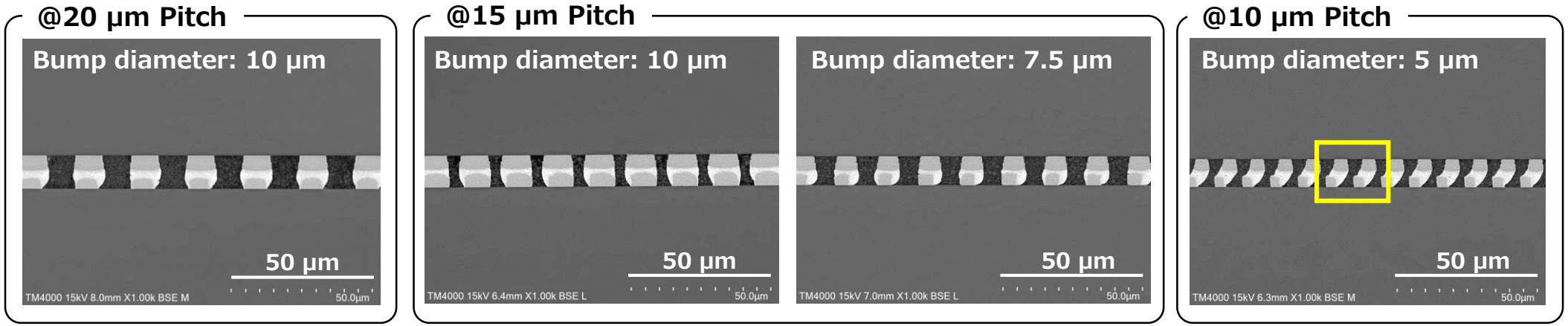


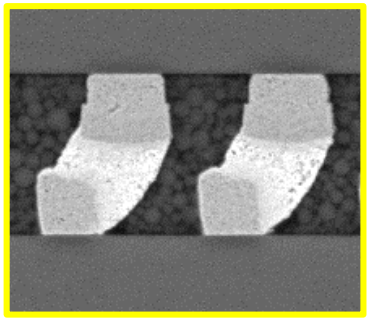
Φ5 μm(10 μm Pitch) bump

Fine Pitch Underfill Technology



● Cross section image after bonding and underfilling





Excellent underfillability in narrow pitch and gap

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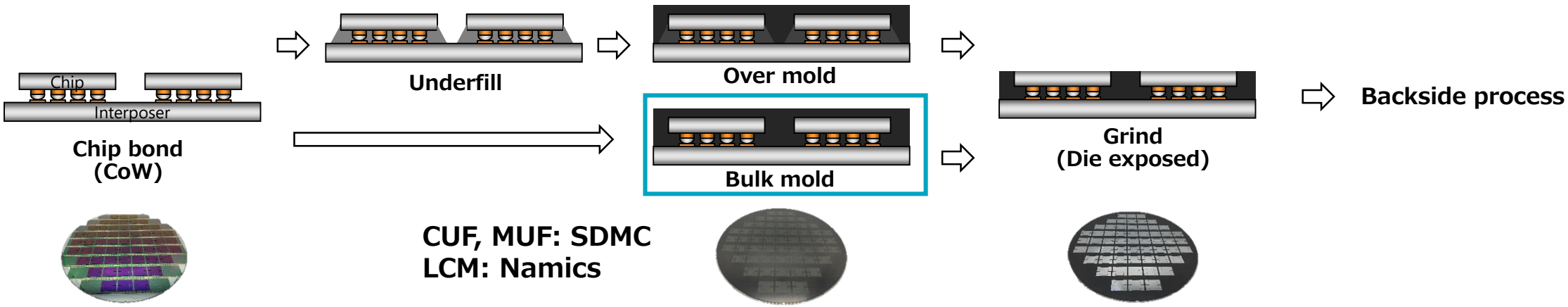
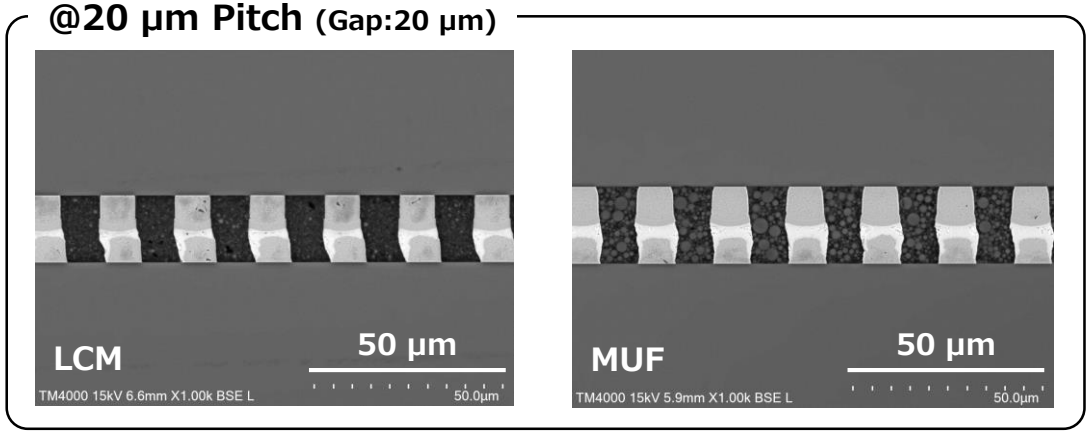
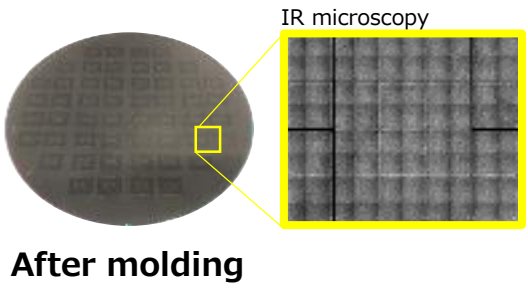
Fine Pitch Underfill Technology

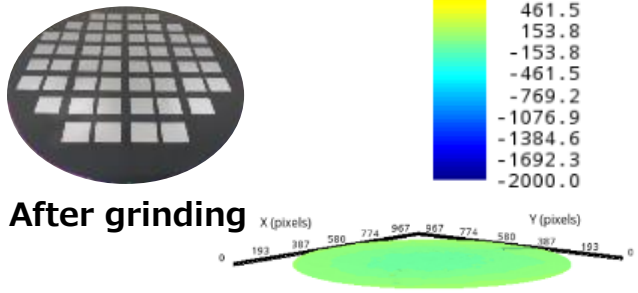


● Cross section image after Compression mold (Bulk molding)





No viod



Low warpage

Achieves narrow gap filling by compression mold

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Flux-less Bonding Technology

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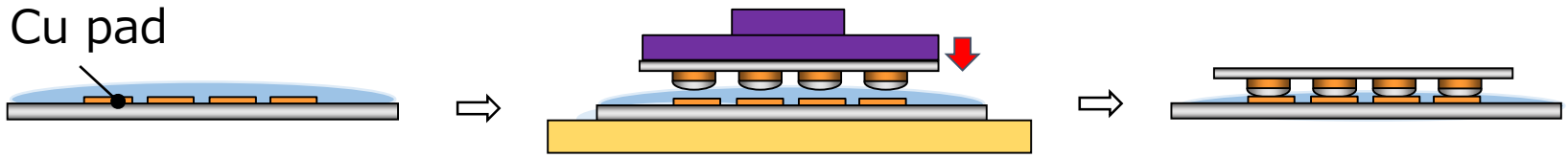
Current

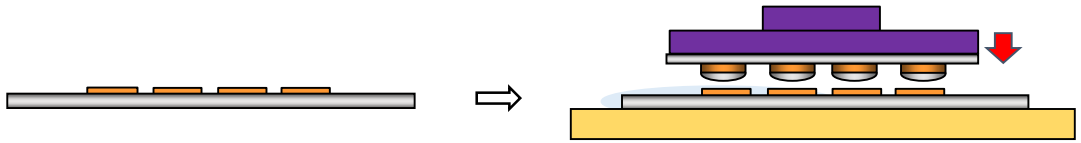
Flux coating → Bonding → Flux cleaning



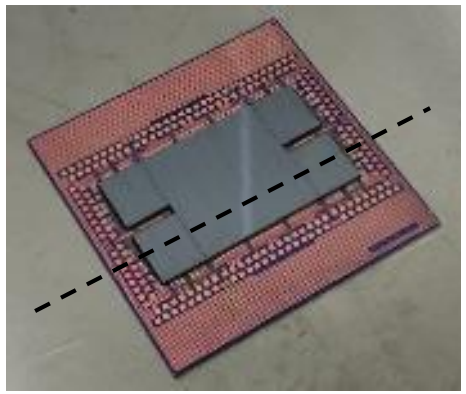
Challenge
1. Flux residue
2. Low productivity

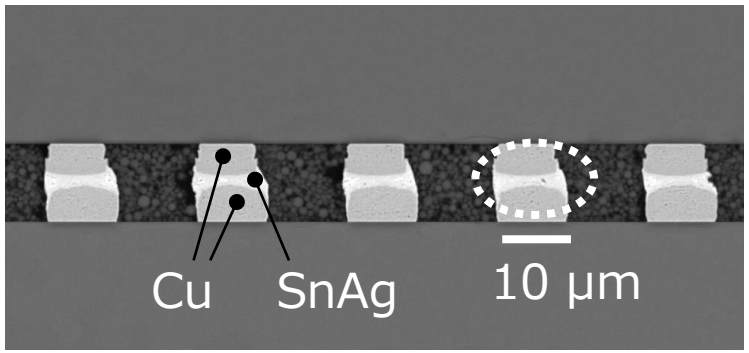
Proposal

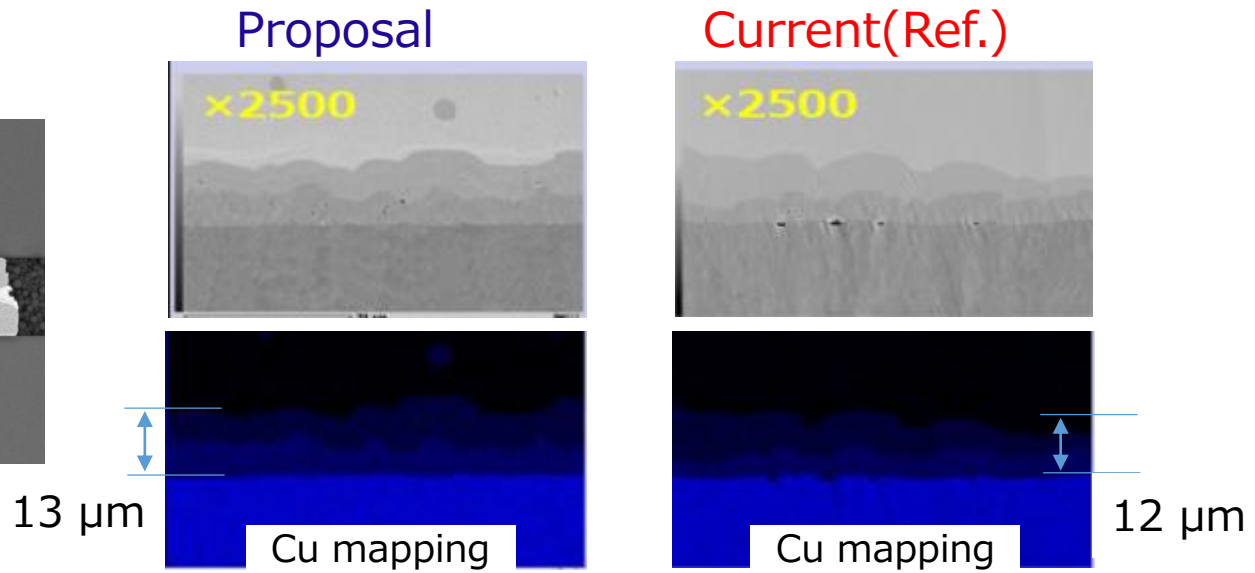
Cu surface activator → Bonding



Advantage
1. No residue
2. Process shortening







IMC diffusion comparison

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RDL Interposer by Semi-Additive Process

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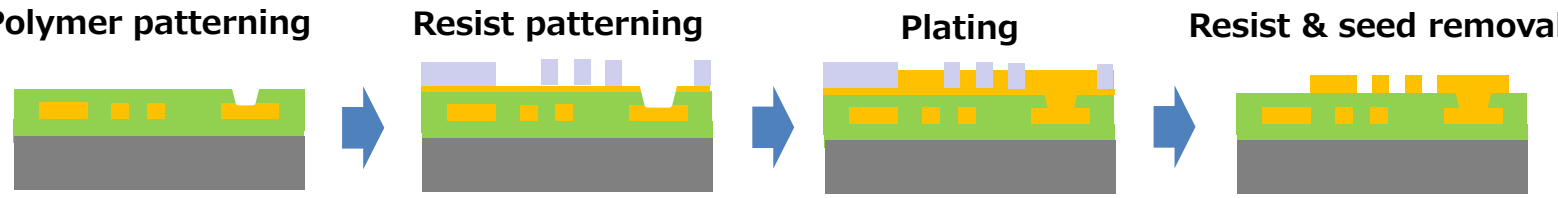
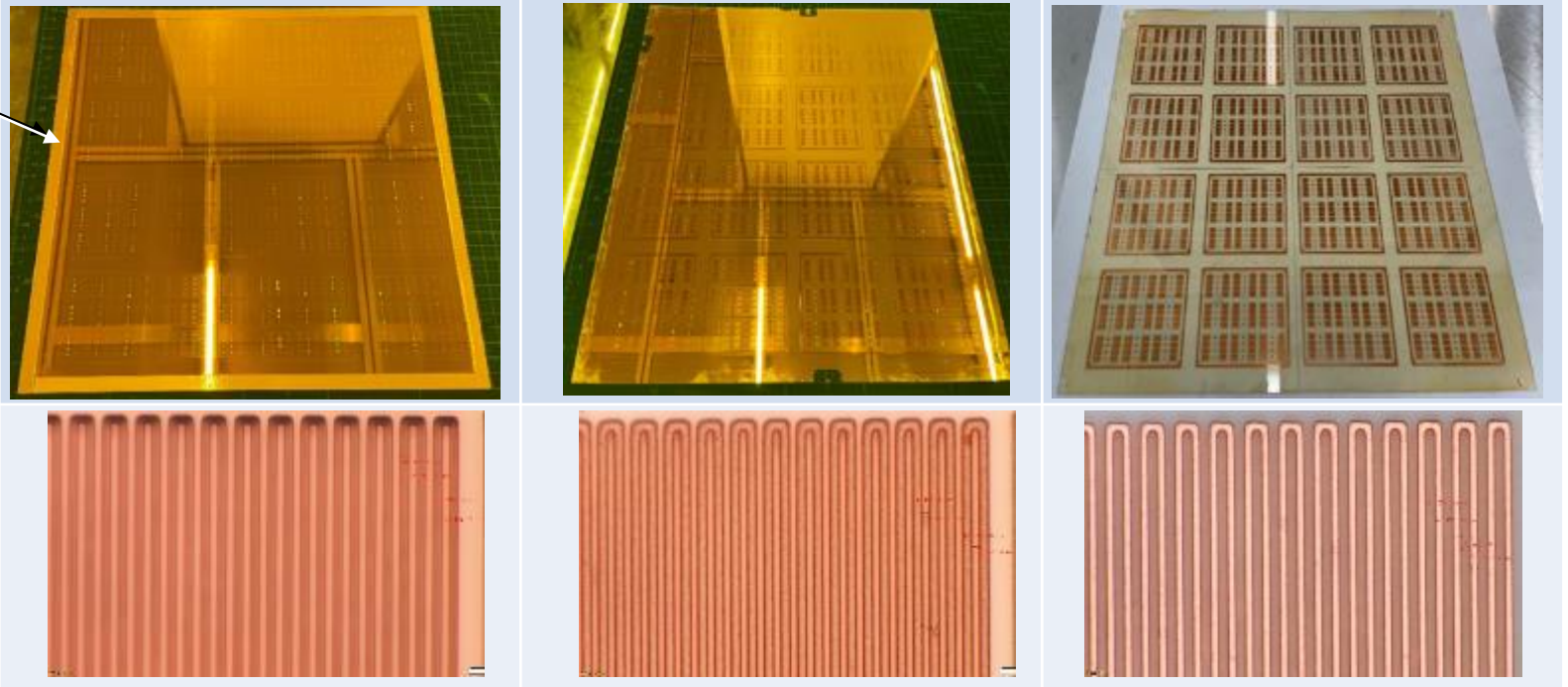
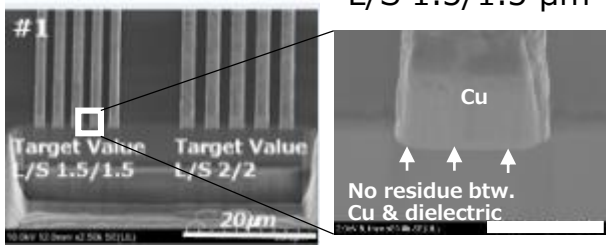
Semi-additive plating



Resist patterning	Cu Plating	Resist & seed removal

Glass Panel





Panel size: 320x320 mm

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RDL Interposer by Semi-Additive Process

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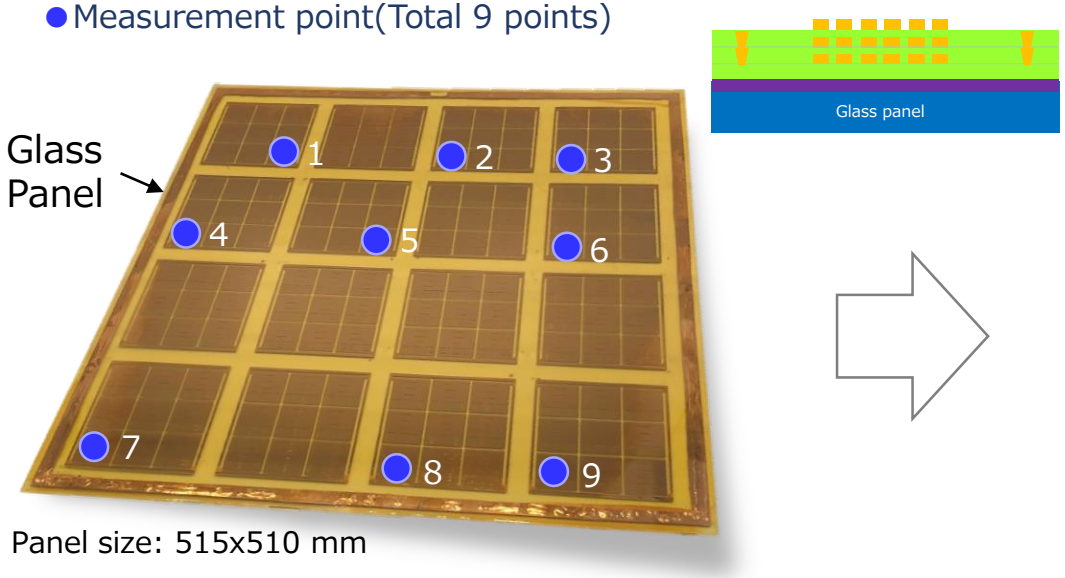
● Fabrication results of three layers of Cu wirings by SAP

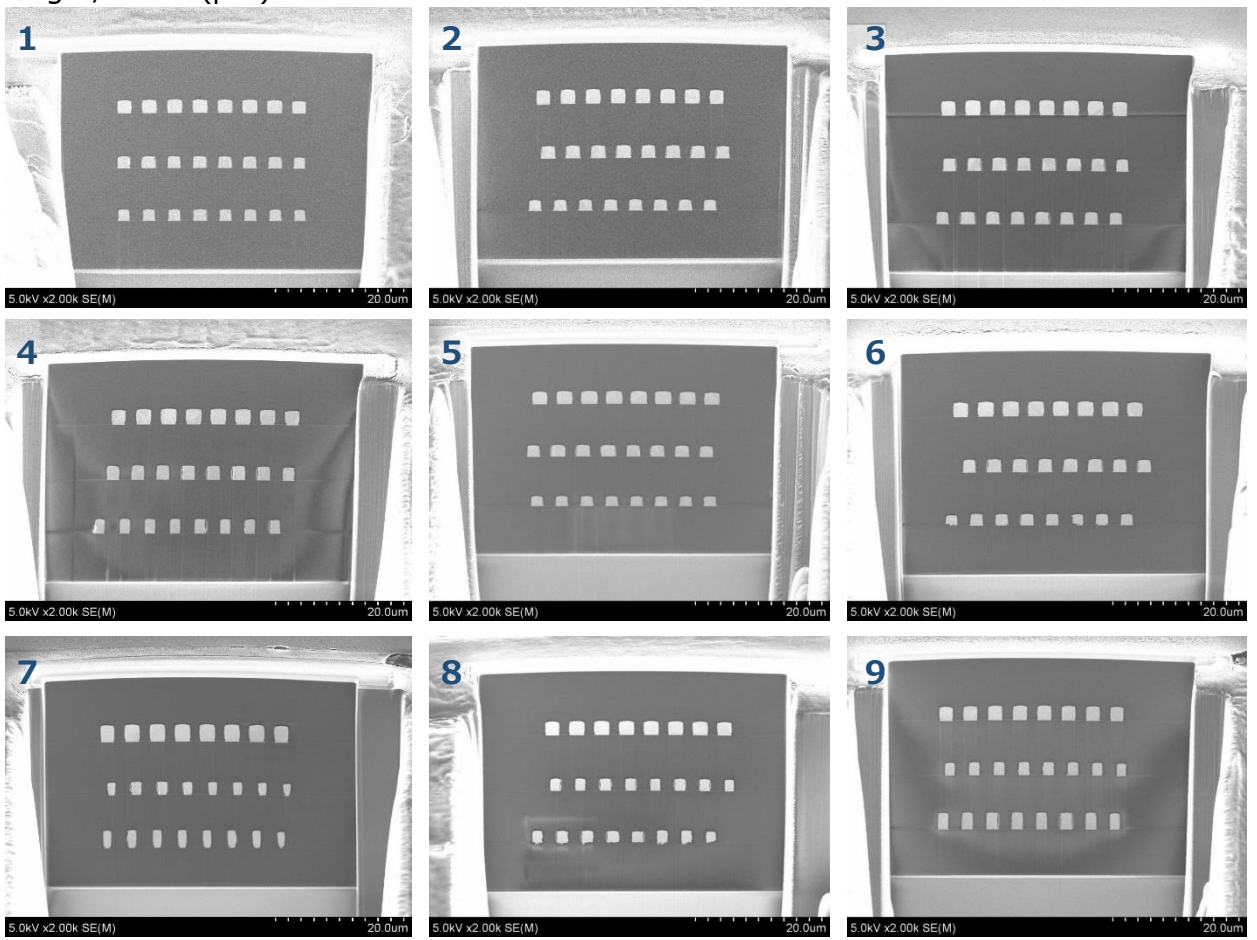
■ In-plane observation results

● Measurement point(Total 9 points)



Panel size: 515x510 mm

Height/Width (μm)



L/S 2.0/2.0 μm

Processing and imaging conditions

FIB : NB5000(Hitachi High-Tech Co.)
Accelerating voltage 40 kV
FE-SEM : S-4800(Hitachi High-Tech Co.)
Accelerating voltage 5 kV

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Fine Lateral Interconnection
Chip Bridge Interposer

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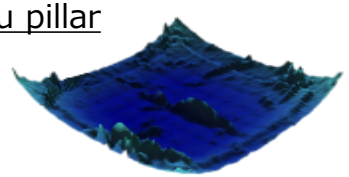
Size: 320x320 mm

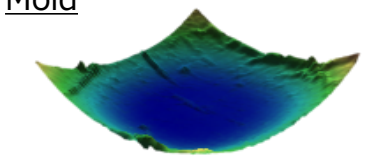
● Panel Warpage

Cu pillar



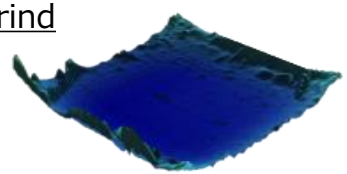
850 μm

Mold



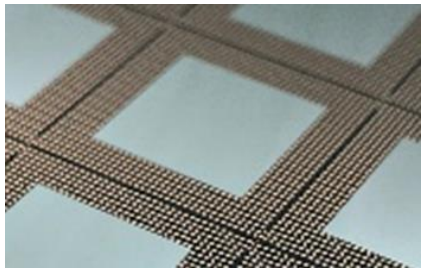
2200 μm

Grind

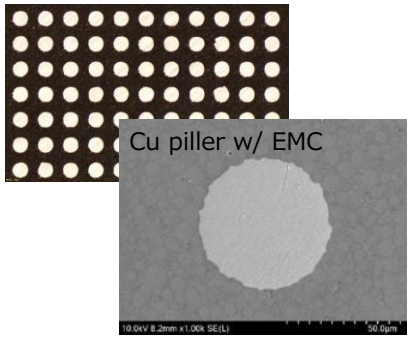


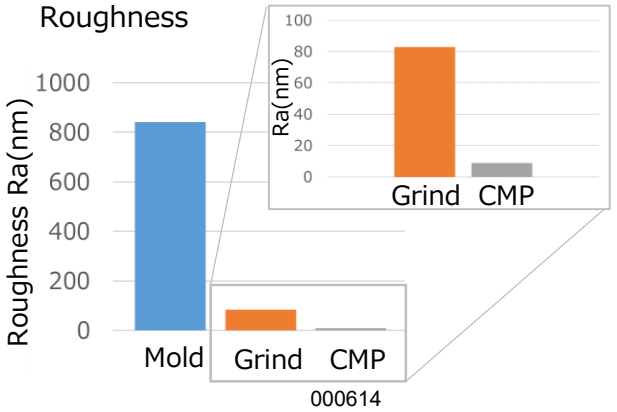
700 μm

● Planarization (CMP)



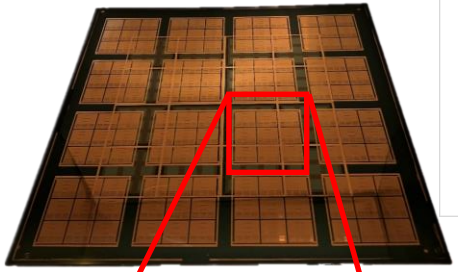
Overview after CMP

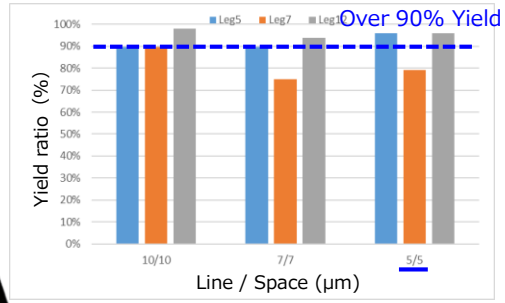


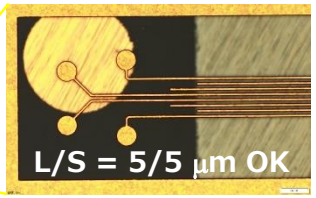


● RDL

Appearance after SAP



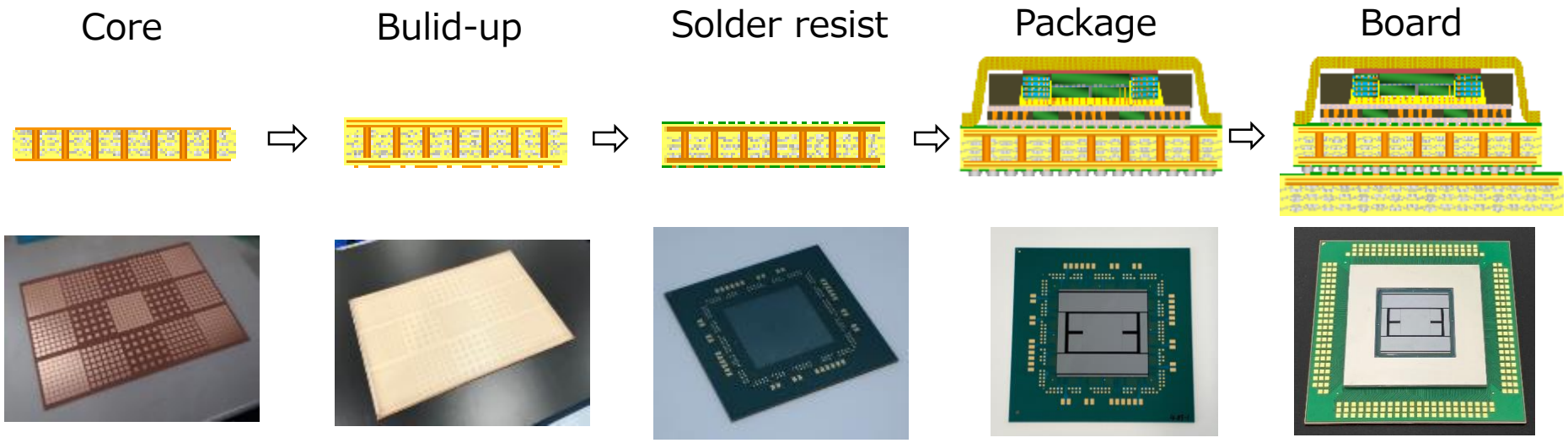




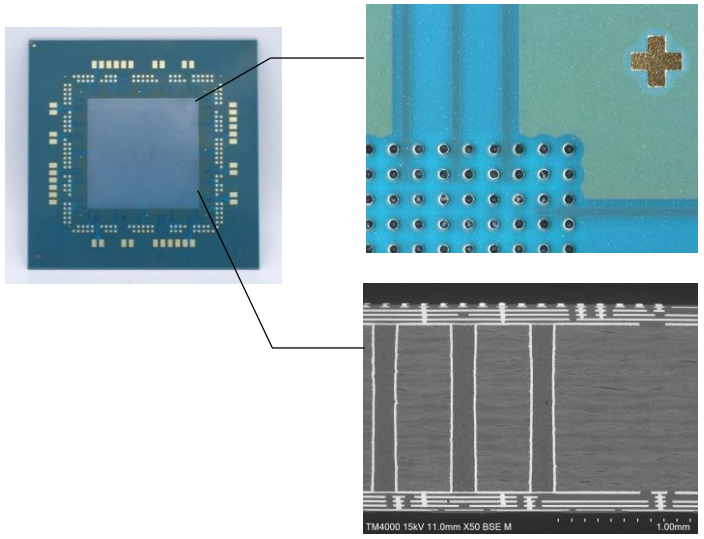
High Reliability Large Package
Package Substrate Fabrication

RESONAC

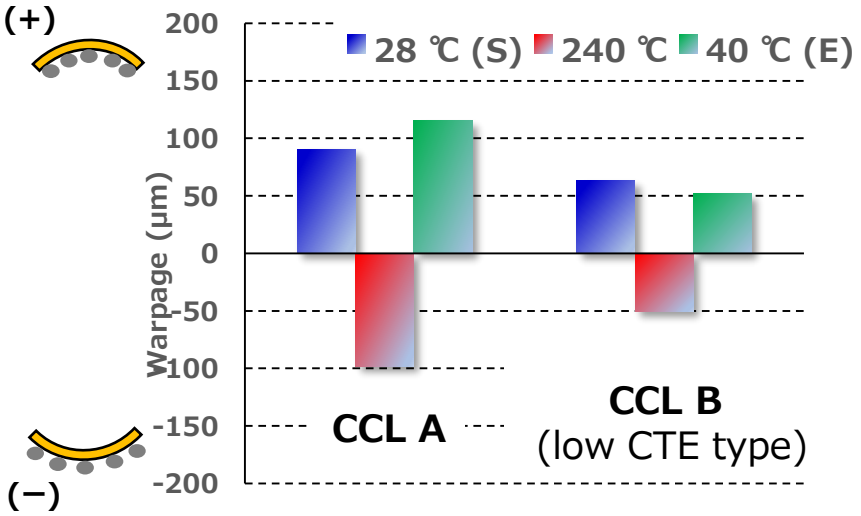
Fabrication Process



Completed 100x100 mm substrate fabrication



Substrate Structure		Target Specification
Layer		4-2-4
Core	Thickness	1.3 mm
	Cu foil thickness	12 μm
BU	Thickness on copper	15 μm
Cu thickness		15 μm
SR	Thickness on copper	18 μm
	SR opening	SMD



- **Large substrates could be fabricated according to specifications.**
- **Warpage was suppressed by using low CTE CCL.**

Interposer / Substrate Mounting

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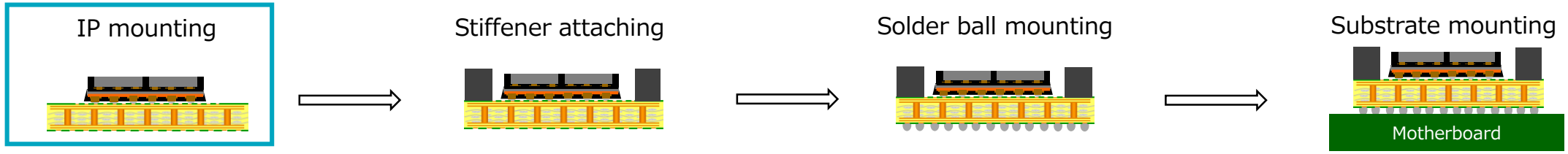
●Mounting process（Interposer, Substrate）

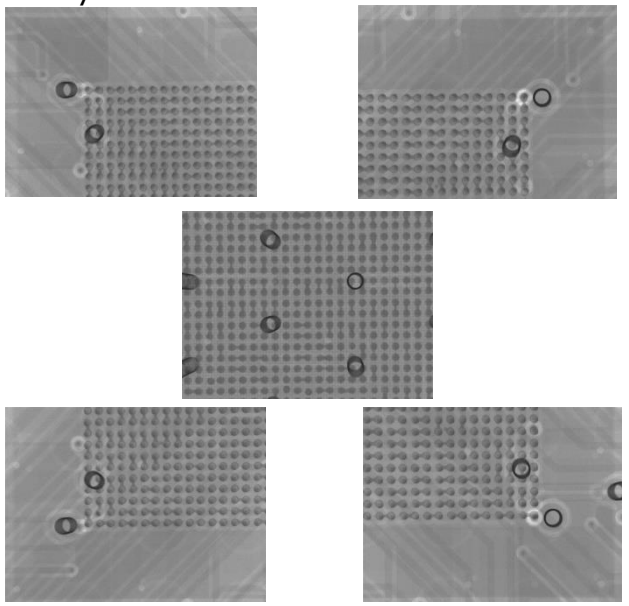


IP mounting

IP mounting（mounter）

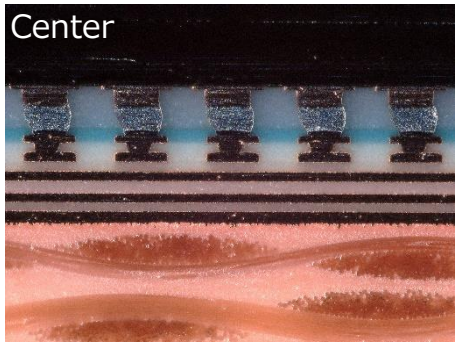
Solder joint（reflow）

X-ray

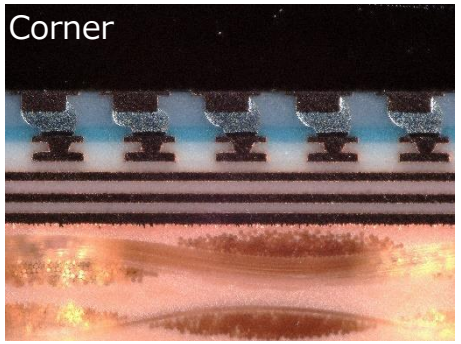


Cross section

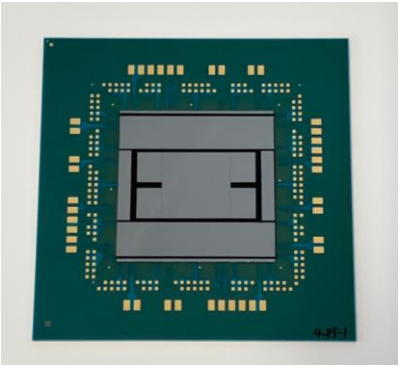
Center



Corner



Overview after IP mounting



Solder joints were formed with good alignment.

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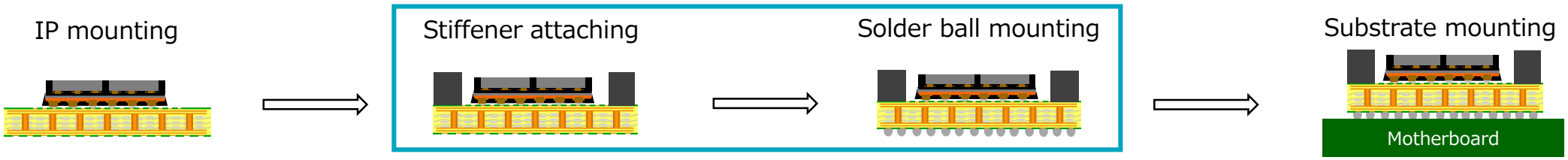
Interposer / Substrate Mounting

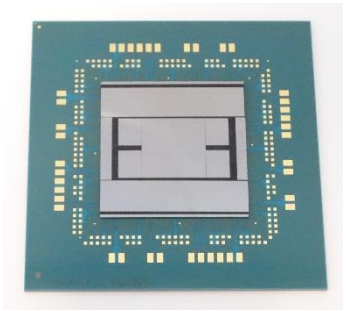
RESONAC

●Mounting process（Interposer, Substrate）

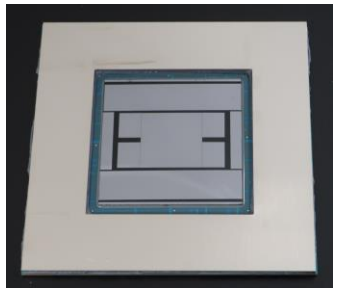


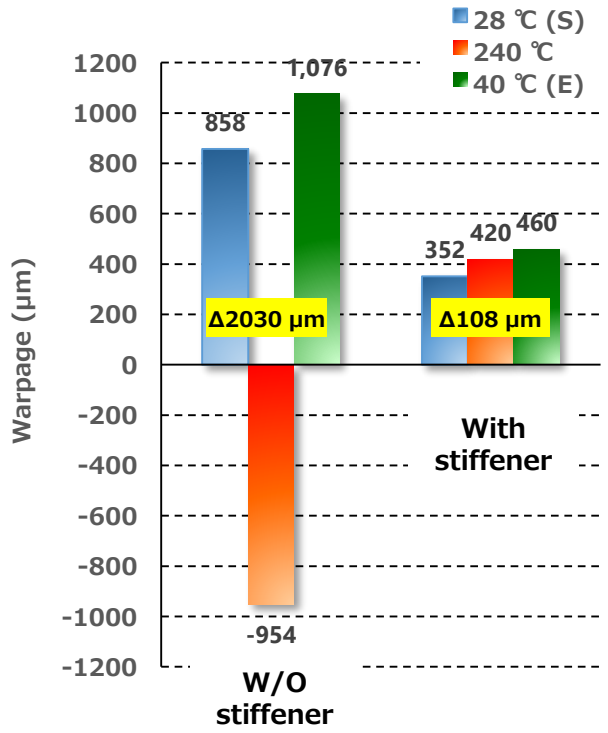
Stiffener attaching

W/O stiffener



With stiffener





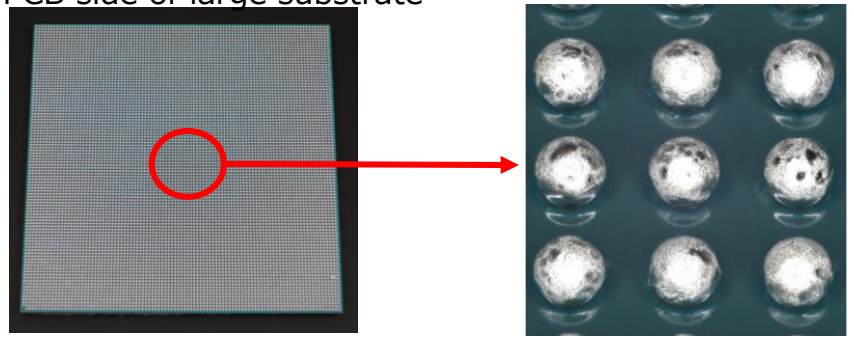
Warpage was improved by Stiffener.

000617

Solder ball mounting

Item		Target Specification
Ball pitch		1 mm
Ball size		Φ600 μm
Pad size		Φ600 μm
SR	Structure	SMD
	SRO	Φ500 μm

PCB side of large substrate

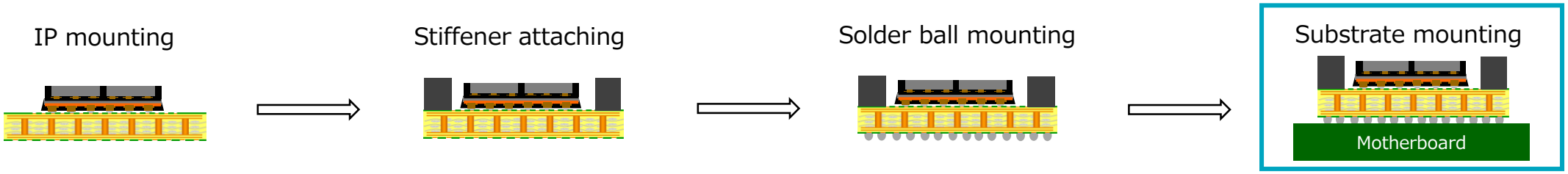


Solder ball height: 478 μm (Avg.)

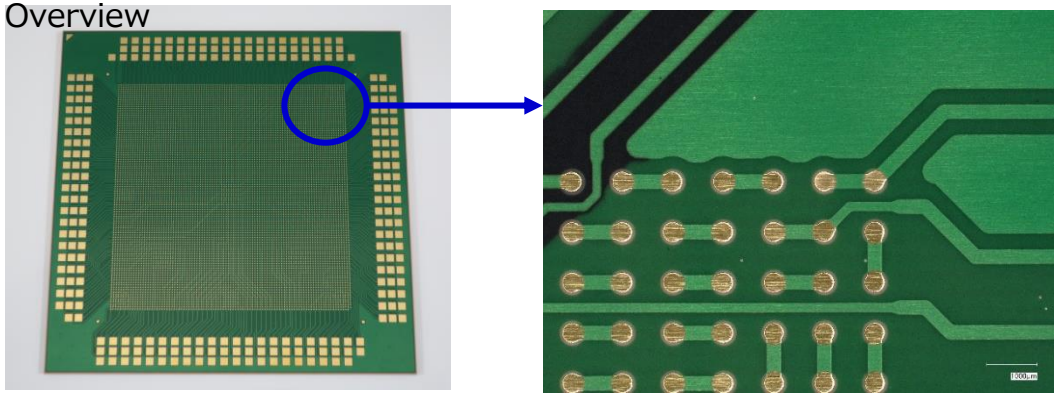
Interposer / Substrate Mounting

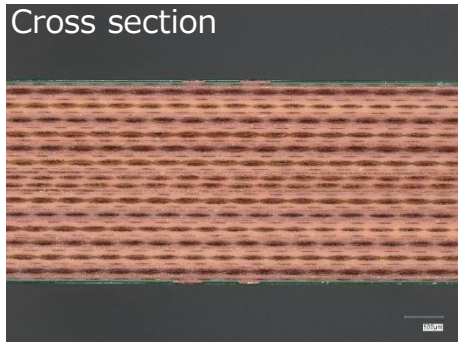
RESONAC

●Mounting process（Interposer, Substrate）



Mother board (PCB)





Item		Target Specification
Layer		28 (Simple structure)
Size		150x150 mm
Thickness		2.8 mm
Pad	Pitch	1 mm
	Size	Φ400 μm
	SRO	Φ500 μm

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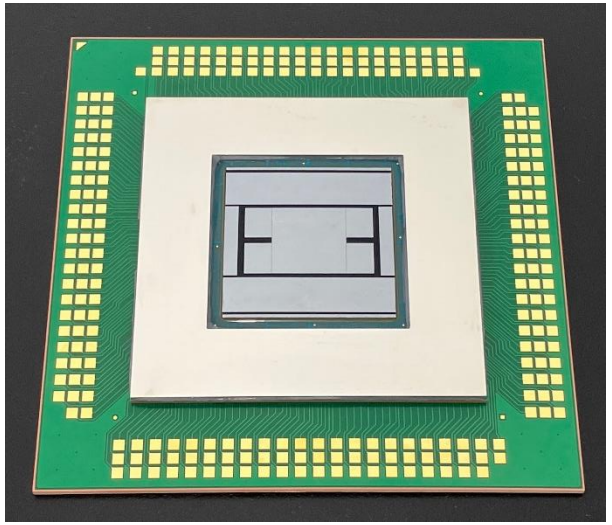
Reliability sample



Completed the reliability sample after mounting the 2.5D package substrate on the PCB.

Packaging Solution Center in U.S.(Draft)

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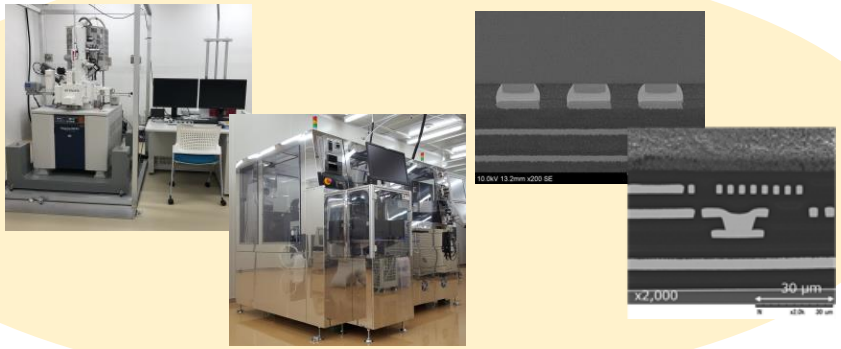
Packaging Solution Center in Silicon Valley

- ✓ Assembly technology: Dicer, Bonder, Cleaner, Dispenser, Plating, Molding, Reflow, etc.
- ✓ RDL technology: Coater, Laminator, Exposure, Developer, Oven, Sputtering, Plating, CMP, etc.
- ✓ Reliability & Failure analysis technology: SEM, AFM, Reflow, TC chamber, B-HAST chamber

YOU

Material supplier



Equipment supplier

Substrate supplier

Partner Contribution Scheme

- ✓ Provide your State-of-the-art equipment and materials to realize customer's POC
- ✓ Cover our operating costs together with us
- ✓ Send your engineers to R&D site to cooperate with us
- ✓ Regular Projects to propose to both customers
- ✓ Some equipment and technology are open to use for your own project

If you are interested to join in this Ecosystem, please don't hesitate to contact us!

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「JOINT2 is being implemented under the "Research and Development Project for Strengthening Post 5G Information Communication System Infrastructure" (JPNP20017), a subsidized project of the New Energy and Industrial Technology Development Organization (NEDO), a national research and development agency.」

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Note

Performance forecast and other statements pertaining to the future as contained in this presentation are based on the information available as of today and assumptions as of today regarding risk factors that could affect our future performance. Actual results may differ materially from the forecast due to a variety of risk factors, including, but not limited to, the influence of the coronavirus disease 2019 (COVID-19) on the world economy, the economic conditions, costs of naphtha and other raw materials, demand for our products such as graphite electrodes and other commodities, market conditions, and foreign exchange rates. We undertake no obligation to update the forward-looking statements unless required by law.

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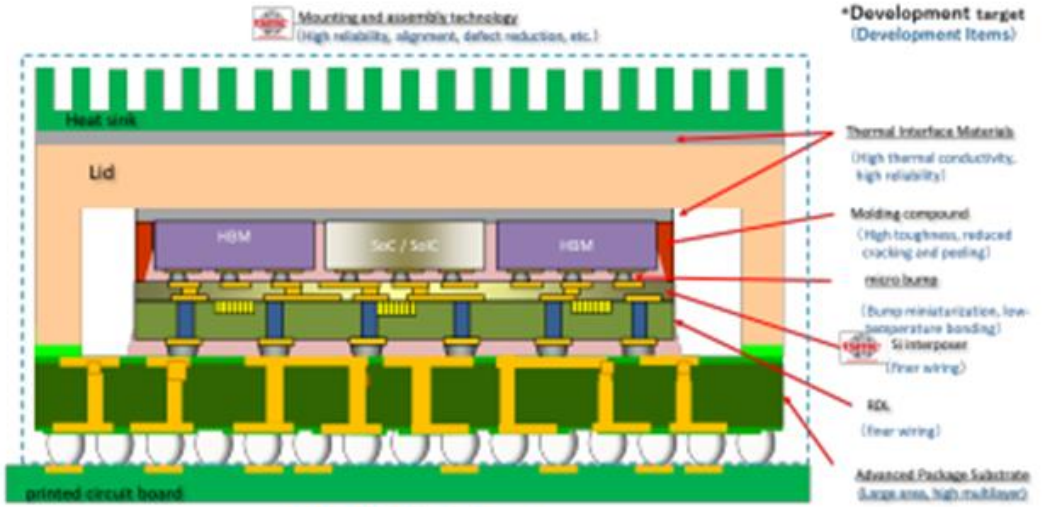
Japanese government semiconductor strategy by METI(Ministry of Economy, Trade and Industry)

【参考】先端半導体製造（後工程）プロセス技術の開発 採択テーマ概要（1）

- 高性能コンピューティング、広帯域5Gネットワークスイッチング、自律走行の人工知能や統合センシング・診断等を実現するためには、半導体デバイスのさらなる集積化・高性能化を可能とする3Dパッケージ技術（ロジック、メモリー、周辺デバイスを1つのパッケージに高密度に実装する技術）の開発が不可欠。
- このため、本事業では、基板上実装技術（on-substrate technologies）を中心として、新しい加工材料、基板材料、接合プロセス、新規の接合・計測機器技術等を含む3Dパッケージング技術について開発し、 TSMCジャパン３DIC研究開発センターが産総研のクリーンルームに構築するプロセスラインでの評価・検証を通じて、信頼性の高い組立技術として統合する。
- また、 本センターは、日本の材料・装置メーカー及び研究機関・大学（下記）とのパートナーシップに強力に取り組む。最先端の技術ポジションを獲得すべく、拡張性があり、製造可能で費用効果の高いソリューションの開発を行う。

パイロットラインを構築する産総研クリーンルーム（つくば市）



3DIC構造イメージ

実施者：ＴＳＭＣジャパン３ＤＩＣ研究開発センター株式会社

<パートナー企業・機関（50音順）>※下記に限定するものではない

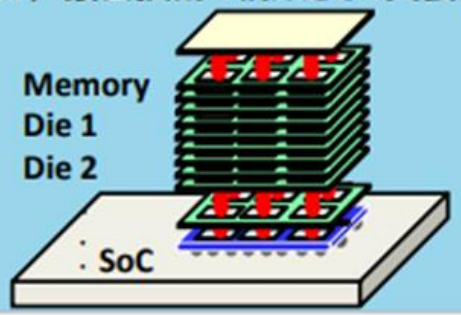
【材料メーカー】旭化成、イビデン、JSR、昭和電工マテリアルズ、信越化学工業、新光電気工業、住友化学、積水化学工業、東京応化工業、長瀬産業、日東電工、日本電気硝子、富士フィルム、三井化学、**【装置メーカー】**キーエンス、芝浦メカトロニクス、島津製作所、昭和電工、ディスコ、東レエンジニアリング、日東電工、日立ハイテク、**【大学・研究機関】**産業技術総合研究所、先端システム技術研究組合（RaaS）、東京大学

quote: 20210531002-2.pdf (meti.go.jp)

【参考】先端半導体製造（後工程）プロセス技術の開発 採択テーマ概要（2）～（5）

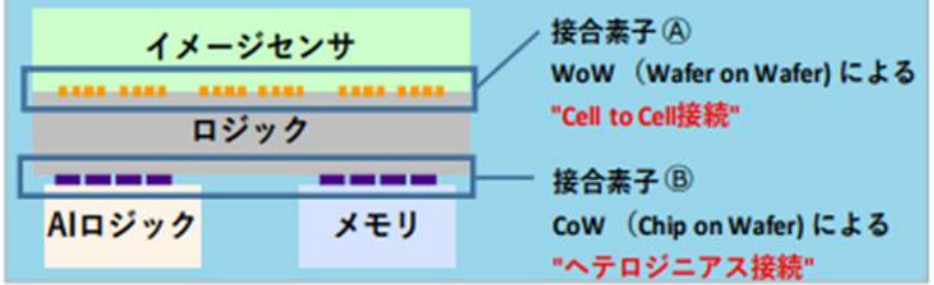
(2) 実施者：先端システム技術研究組合（RaaS）※1

- 事業テーマ：ダイレクト接合３D積層技術開発（WoWおよびCoW向け装置･プロセス開発）
- 概要：Cu-Cu の低温ハイブリッド接合による WoW（Wafer on Wafer）接合技術及び CoW（Chip on Wafer）接合技術の構築とその実装化に取り組む。



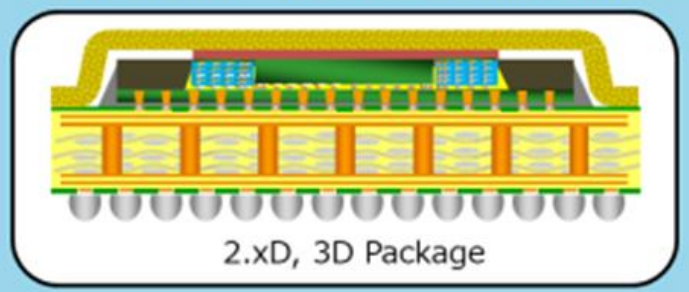
(3) 実施者：ソニーセミコンダクタソリューションズ株式会社

- 事業テーマ：ポスト５ Ｇエッジコンピューティング向け半導体の３D積層要素技術研究開発
- 概要：積層モジュールの基本特性および信頼性取得が可能となるピッチサイズ目標を年度ごとに設定し、ロバストな半導体製造プロセスの要素技術を確立する。



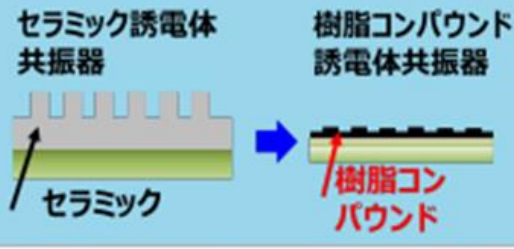
(4) 実施者：昭和電工マテリアルズ株式会社※2

- 事業テーマ：最先端パッケージ評価プラットフォーム創成
- 概要：基板、装置、材料メーカーによるコンソーシアムを創成、評価プラットフォームを設置し次世代半導体パッケージの評価技術、基板、装置及び材料を開発する。



(5) 実施者：住友ベークライト株式会社

- 事業テーマ：次世代情報通信向け先端パッケージの材料開発
- 概要：３次元実装密度向上において重要となる、Wafer Level PKG向け封止材、アンテナ向け封止材、再配線用感光材のファインピッチ対応技術を開発する。

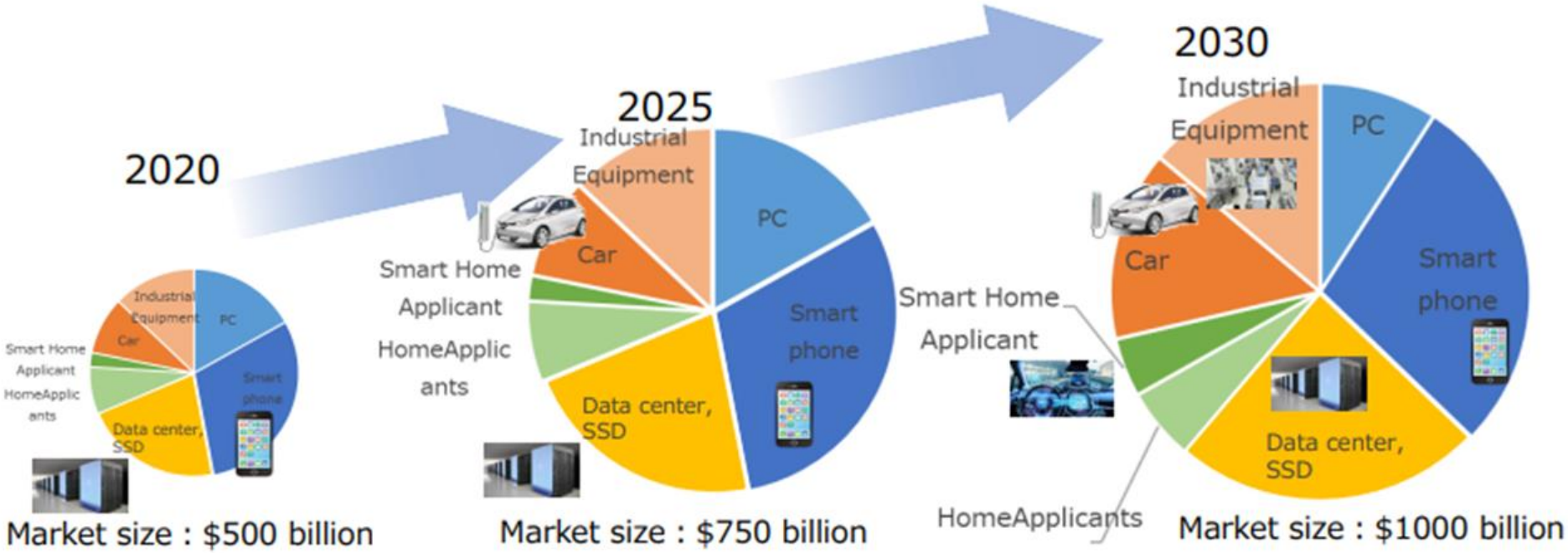


※1 （共同実施先、組合員企業等）国立研究開発法人産業技術総合研究所、SCREENホールディングス、ダイキン工業、富士フイルム、パナソニックスマートファクトリソリューションズ、東京大学
※2 （共同実施先、協力企業等）味の素ファインテクノ、上村工業、荏原製作所、新川、新光電気工業、大日本印刷、ディスコ、東京応化工業、TOWA、ナミックス、パナソニックスマートファクトリーソリューションズ、ヤマハロボティクスホールディングス

quote: 20210531002-2.pdf (meti.go.jp)

Basic Semiconductor Revitalization Strategy in Japan

Step 1 : Enhancement of Basic Production Capacity for IoT



Step 2 : Realization of Next Generation Semiconductor Technology through JP-US Collaboration

Step 3 : RD For Future technology

Photonics-Electronics Convergence, Quantum Computing through Global Collaboration

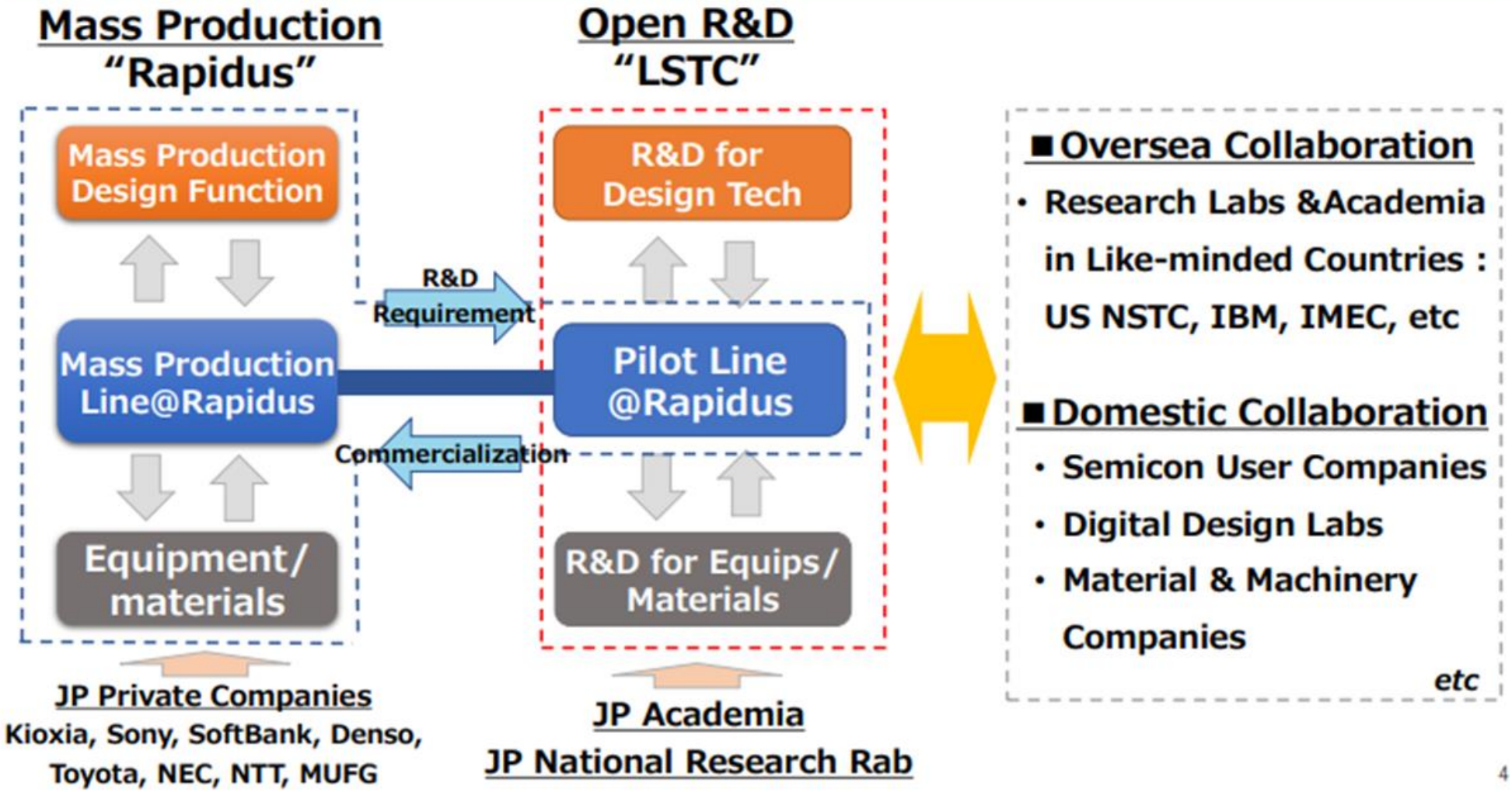
(Reference) : prepared by METI, based on data from OMDIA

quote: 1111_001a.pdf (meti.go.jp)

Project Framework for Next Generation Beyond 2nm Project (B2P)

<METI announcement on 11th Nov.>: Establishment of Two Entities for B2P

1. "LSTC": Open Collaborative R&D Platform (Public Entity) ※Leading-Edge Technology Center
2. "Rapidus": Mass Production Entity (Inc.)



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quote: 1111_001a.pdf (meti.go.jp)