Advanced Packaging Materials and Open Innovation at Resonac

Hidenori Abe
Senior Director, Electronics Business Headquarters
Resonac Corporation
March 15, 2023
1. Corporate Introduction

2. Introduction of Packaging Solution Center & JOINT2

3. R&D Status for Advanced Package
January 2023: Resonac was born

Showa Denko

Showa Denko Materials (Former Hitachi Chemical)

Chemistry for Change
Corporate introduction - Net Sales

Semi conductor and Electronics materials

- 31% (392 Billion ¥)
- High purity Gas for semiconductor
- CMP slurry
- Epoxy molding compound
- Die bonding material
- Cupper clad laminate
- Photosensibity film
- Photosensibity solder mask
- Hard disc
- SiC epitaxial wafer
- Composite semiconductor (LED)

Other 10%
- Life science products etc.

Chemical 34%
- Petroleum chemistry
- Chemicals
- Graphite electrode

Innovation material 11%
- High-functionary chemicals
- High-performance resin
- Coating material, Ceramics, Aluminium functional component

Mobility 14%
- Automobile component
- Lithium-ion battery material

Sales (2021) 1,259 Billion ¥
Global Players and Sales in Semiconductor related Materials (2021)

<table>
<thead>
<tr>
<th>Company</th>
<th>Main Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Si Wafer</td>
</tr>
<tr>
<td>B</td>
<td>Si Wafer</td>
</tr>
<tr>
<td>C</td>
<td>Si Wafer, High Purity Gases, CMP, Back-End Materials</td>
</tr>
<tr>
<td>D</td>
<td>Si Wafer</td>
</tr>
</tbody>
</table>

Source: Showa Denko’s original survey

Materials for Back-End Process

<table>
<thead>
<tr>
<th>Company</th>
<th>Main Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>CCL (No.1)</td>
</tr>
<tr>
<td>K</td>
<td>CCL, EMC, DAF, Photosensitive Materials</td>
</tr>
<tr>
<td>L</td>
<td>CCL for PKG</td>
</tr>
<tr>
<td>M</td>
<td>CCL for PKG EMC</td>
</tr>
</tbody>
</table>

Top Share in Back-End Process

- **RESONAC**
  - CCL (No.1)
  - DAF (No.1)
  - DFR (No.1)
  - EMC (No.2)

- **Global TOP**
  - Si Wafer: 2,665
  - Si Wafer (100M JPY)

000599
Materials Line-Up for Semiconductor PKG

- Materials for Buffer Coating
- CMP Slurry for Cu/Barrier Metal
- CMP Slurry for STI/ILD
- Photo Sensitive Dry Film
- Mother board Core & Prepreg Material
- Solder Resist
- QFN Support tape
- Die Bonding Film
- Die Bonding Paste
- Epoxy Molding Compounds (Tablet, Granule)
- Photosensitive insulation material
- Thermal Interface Material
- Underfill Material (CUF/ NCF)
- Solder Resist
- Package Substrate Prepreg, Resin Film
- Package Substrate core material
Packaging Solution Center (PSC)

Packaging Solution Center is located on the 3rd and 4th floor in Kawasaki-city, Kanagawa-pref.
Total floor area: 7,000 m²

[ Strong point of PSC ]
- Global top for packaging R&D site
- Long term experience of PKG assembly and reliability evaluation (over 28 years)
- Deep knowledge of assembly evaluation
- Through integrated Assembly Line
- Combination and control of materials

[ Through collaboration ]
- Many experiences and results through Open Innovation
- Many connections among material and equipment suppliers.

JOINT1: FO-WLP & PLP
JOINT2: 2.xD & 3D

IMAPS 19th Conference on DEVICE PACKAGING | March 13-16, 2023 | Fountain Hills, AZ USA
Function & Target of PSC

Regardless of the collaboration type, all activities are operated with utilizing PSC’ key functions.
3rd Floor layout

In Assembly area
- Grinder
- Blade & Laser Dicer
- CoC, CoW flip chip bonder
- Laminator
- Plating

In expansion area
- C2W bonder
- Plasma ashcer
- Large die mounter
- Panel CMP
- Temporary bonder & debonder
- Compression molding
- C2W bonder
- Panel Grinder
- Panel Su/Ag plating

In Mold area
- Transfer
- Substrate Comp.
- Wafer Comp.
- Panel Comp.

In RDL area
- Spin coater
- Slit coater
- Vacuum Dryer
- Stepper
- Developer
- Sputter

In Analysis area
- FE-SEM-EDX
- SAT
- 3D measurement
- FIB
- X-ray CT
- Shadow moiré
- Stylus profiler
- Probe tester
- Laser decapsulator

Total floor area: 4,200 m²
Total clean room: 1,450 m²
New consortium “JOINT2” for

1. unifying contact of each equipment & material companies to customer.
2. creating and increasing opportunity of discussion among equipment & material companies.
3. building advanced PKG test vehicle.

We hope these activities accelerate Customer’s R&D and expand our material business.
“Open innovation platform” evolve to “Consortiums with multiple company”

Multiple working groups × Mutual utilization of technology and information

<table>
<thead>
<tr>
<th>Working Group</th>
<th>Program</th>
</tr>
</thead>
<tbody>
<tr>
<td>WG-A</td>
<td>Fine bump interconnection</td>
</tr>
<tr>
<td></td>
<td>![Fine bump interconnection image]</td>
</tr>
<tr>
<td>WG-B</td>
<td>Fine circuitry interconnection</td>
</tr>
<tr>
<td></td>
<td>![Fine circuitry interconnection image]</td>
</tr>
<tr>
<td>WG-C</td>
<td>High reliability large package</td>
</tr>
<tr>
<td></td>
<td>![High reliability large package image]</td>
</tr>
</tbody>
</table>
JOINT2 is unparalleled scale consortium with high market share companies for Back-end Process.

**Equipment**
- DISCO
- YAMAHA
- Panasonic
- XX
- EBARA

**Back-end Process**

**Material**
- Namics
- Resonac
- XX
- Resonac

**Substrate Process**
- Resonac
- Ajinomoto
- Resonac

**Material**
- Resonac
- XX

**JOINT2 partner**

* Under discussion to join
### Technical roadmap and schedule

<table>
<thead>
<tr>
<th>Evaluation item</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
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<tbody>
<tr>
<td><strong>[WG-A] Fine Bump Interconnect</strong></td>
<td></td>
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<tr>
<td>2.5D</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
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<tr>
<td>2.1D</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
<td><img src="image9.png" alt="Image" /></td>
<td><img src="image10.png" alt="Image" /></td>
<td><img src="image11.png" alt="Image" /></td>
<td><img src="image12.png" alt="Image" /></td>
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<tr>
<td>Bump pitch ≤ 20 μm (2.5D), 40 μm (2.1D)</td>
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<tr>
<td>Substrate TTV ≤ 10 μm</td>
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<tr>
<td>Bump pitch ≤ 15 μm (2.5D), 30 μm (2.1D)</td>
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<tr>
<td>Substrate TTV ≤ 5 μm</td>
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<tr>
<td>Bump pitch ≤ 10 μm (2.5D), 20 μm (2.1D)</td>
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<tr>
<td>Substrate TTV ≤ 3 μm</td>
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<tr>
<td><strong>[WG-B] Fine Circuitry Interconnection</strong></td>
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<tr>
<td>RDL Interposer</td>
<td><img src="image13.png" alt="Image" /></td>
<td><img src="image14.png" alt="Image" /></td>
<td><img src="image15.png" alt="Image" /></td>
<td><img src="image16.png" alt="Image" /></td>
<td><img src="image17.png" alt="Image" /></td>
<td><img src="image18.png" alt="Image" /></td>
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<tr>
<td>Chip Embedded Interposer</td>
<td><img src="image19.png" alt="Image" /></td>
<td><img src="image20.png" alt="Image" /></td>
<td><img src="image21.png" alt="Image" /></td>
<td><img src="image22.png" alt="Image" /></td>
<td><img src="image23.png" alt="Image" /></td>
<td><img src="image24.png" alt="Image" /></td>
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<td>L/S ≤ 2/2 μm</td>
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<td>Single layer</td>
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<tr>
<td>Multi layers</td>
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<tr>
<td>L/S ≤ 1.5/1.5 Multi layers</td>
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<tr>
<td>L/S ≤ 1.2/1.2 Multi layers</td>
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<tr>
<td>L/S ≤ 1/1 μm Multi layers</td>
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<tr>
<td>Process development</td>
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<td>Process development</td>
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<tr>
<td>Chip-let size ≥ 20 mm</td>
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<tr>
<td>Substrate size ≥ 100 mm</td>
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<tr>
<td>Chip-let size ≥ 35 mm</td>
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<tr>
<td>Substrate size ≥ 120 mm</td>
<td></td>
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<tr>
<td>Chip-let size ≥ 50 mm</td>
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<tr>
<td>Substrate size ≥ 140 mm</td>
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</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Diameter</th>
<th>Φ10 μm (20 μm Pitch)</th>
<th>Φ7 μm (14 μm Pitch)</th>
<th>Φ5 μm (10 μm Pitch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist pattern</td>
<td><img src="D10um.png" alt="D10um" /></td>
<td><img src="D7um.png" alt="D7um" /></td>
<td><img src="D5um.png" alt="D5um" /></td>
</tr>
</tbody>
</table>

**SEM image**

Φ5 μm (10 μm Pitch) bump

**No residue**

**No missing bump**
Fine Vertical Interconnection
Fine Pitch Underfill Technology

- Chip bond (CoW)
- Interposer
- Underfill
- Over mold
- Grind (Die exposed)
- Backside process

CUF, MUF: SDMC
LCM: Namics

● Cross section image after bonding and underfilling

@20 μm Pitch
Bump diameter: 10 μm
50 μm
50 μm

@15 μm Pitch
Bump diameter: 10 μm
50 μm
50 μm

Bump diameter: 7.5 μm
50 μm
50 μm

@10 μm Pitch
Bump diameter: 5 μm
50 μm
50 μm

Excellent underfillability in narrow pitch and gap
Fine Vertical Interconnection
Fine Pitch Underfill Technology

- Chip bond (CoW)
- Underfill
- Over mold
- Bulk mold
- Grind (Die exposed)
- Backside process

CUF, MUF: SDMC
LCM: Namics

- Cross section image after Compression mold (Bulk molding)

@20 μm Pitch (Gap: 20 μm)

LCM 50 μm
MUF 50 μm

- IR microscopy
- After molding
- After grinding

No void
Low warpage

Achieves narrow gap filling by compression mold
Current Flux coating

Cu pad

Bonding

Flux cleaning

Challenge
1. Flux residue
2. Low productivity

Proposal

Cu surface activator

Bonding

Advantage
1. No residue
2. Process shortening

Proposal

Current (Ref.)

Cu mapping

Flux-less Bonding Technology

Fine Vertical Interconnection

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Fine Lateral Interconnection
RDL Interposer by Semi-Additive Process

Semi-additive plating

Polymer patterning → Resist patterning → Plating → Resist & seed removal

Resist patterning
Cu Plating
Resist & seed removal

Glass Panel

Panel size: 320x320 mm

L/S 1.5/1.5 μm

No residue btw. Cu & dielectric
Fabrication results of three layers of Cu wirings by SAP

In-plane observation results

Measurement point (Total 9 points)

Processing and imaging conditions

FIB : NB5000 (Hitachi High-Tech Co.)
Accelerating voltage 40 kV

FE-SEM : S-4800 (Hitachi High-Tech Co.)
Accelerating voltage 5 kV
Size: 320x320 mm

- Cu pillar/Chip mount
- Mold (175 μm)
- Grind (175→150 μm)
- CMP
- RDL (SAP wirings)

● Panel Warpage
  - Cu pillar
    - 850 μm
  - Mold
    - 2200 μm
  - Grind
    - 700 μm

● Planarization (CMP)

- Overview after CMP
- Roughness
  - Mold
  - Grind
  - CMP
  - Roughness Ra(nm)

- Appearance after SAP
  - L/S = 5/5 μm OK
  - Over 90% Yield

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High Reliability Large Package
Package Substrate Fabrication

Fabrication Process

Completed 100x100 mm substrate fabrication

<table>
<thead>
<tr>
<th>Substrate Structure</th>
<th>Target Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer</td>
<td>4-2-4</td>
</tr>
<tr>
<td>Core</td>
<td>Thickness 1.3 mm</td>
</tr>
<tr>
<td></td>
<td>Cu foil thickness 12 µm</td>
</tr>
<tr>
<td>BU</td>
<td>Thickness on copper 15 µm</td>
</tr>
<tr>
<td>Cu thickness</td>
<td>15 µm</td>
</tr>
<tr>
<td>SR</td>
<td>Thickness on copper 18 µm</td>
</tr>
<tr>
<td></td>
<td>SR opening SMD</td>
</tr>
</tbody>
</table>

- Large substrates could be fabricated according to specifications.
- Warpage was suppressed by using low CTE CCL.

Warpage graph showing:
- CCL A (low CTE type)
- CCL B

Temperatures:
- 28 °C (S)
- 240 °C
- 40 °C (E)
Mounting process (Interposer, Substrate)

- IP mounting
- Stiffener attaching
- Solder ball mounting
- Substrate mounting

Solder joints were formed with good alignment.
Mounting process (Interposer, Substrate)

- **IP mounting**
- **Stiffener attaching**
- **Solder ball mounting**
- **Substrate mounting**

**Stiffener attaching**
- **W/O stiffener**
- **With stiffener**

**Solder ball mounting**

<table>
<thead>
<tr>
<th>Item</th>
<th>Target Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ball pitch</td>
<td>1 mm</td>
</tr>
<tr>
<td>Ball size</td>
<td>Φ600 μm</td>
</tr>
<tr>
<td>Pad size</td>
<td>Φ600 μm</td>
</tr>
<tr>
<td>SR Structure</td>
<td>SMD</td>
</tr>
</tbody>
</table>

Solder ball height: 478 μm (Avg.)

Warpage was improved by Stiffener.
Mounting process (Interposer, Substrate)

IP mounting → Stiffener attaching → Solder ball mounting → Substrate mounting

Mother board (PCB)

Overview

Cross section

Item  | Target Specification
---   | -------------------
Layer | 28 (Simple structure)
Size  | 150x150 mm
Thickness | 2.8 mm
Pad Pitch | 1 mm
Size | ø400 μm
SRO | ø500 μm

Reliability sample

Completed the reliability sample after mounting the 2.5D package substrate on the PCB.
Packaging Solution Center in U.S. (Draft)

Packaging Solution Center in Silicon Valley
✓ Assembly technology: Dicer, Bonder, Cleaner, Dispenser, Plating, Molding, Reflow, etc.
✓ RDL technology: Coater, Laminator, Exposure, Developer, Oven, Sputtering, Plating, CMP, etc.
✓ Reliability & Failure analysis technology: SEM, AFM, Reflow, TC chamber, B-HAST chamber

Material supplier
Equipment supplier
Substrate supplier

YOU

Partner Contribution Scheme
✓ Provide your State-of-the-art equipment and materials to realize customer’s POC
✓ Cover our operating costs together with us
✓ Send your engineers to R&D site to cooperate with us
✓ Regular Projects to propose to both customers
✓ Some equipment and technology are open to use for your own project

If you are interested to join in this Ecosystem, please don't hesitate to contact us!
「JOINT2 is being implemented under the "Research and Development Project for Strengthening Post 5G Information Communication System Infrastructure" (JPNP20017), a subsidized project of the New Energy and Industrial Technology Development Organization (NEDO), a national research and development agency.」
Note

Performance forecast and other statements pertaining to the future as contained in this presentation are based on the information available as of today and assumptions as of today regarding risk factors that could affect our future performance. Actual results may differ materially from the forecast due to a variety of risk factors, including, but not limited to, the influence of the coronavirus disease 2019 (COVID-19) on the world economy, the economic conditions, costs of naphtha and other raw materials, demand for our products such as graphite electrodes and other commodities, market conditions, and foreign exchange rates. We undertake no obligation to update the forward-looking statements unless required by law.
Japanese government semiconductor strategy by METI(Ministry of Economy, Trade and Industry)
【参考】先端半導体製造（後工程）プロセス技術の開発・採択テーマ概要（1）

- 高性能コンピューティング、広帯域5Gネットワークスイッチング、自律走行の人工知能や統合センシング・診断等を実現するためには、半導体デバイスのさらなる集積化・高性能化を可能とする3Dパッケージ技術（ロジック、メモリー、周辺デバイスを1つのパッケージに高密度に実装する技術）の開発が不可欠。

- このため、本事業では、基板上実装技術（on-substrate technologies）を中心として、新しい加工材料、基板材料、接合プロセス、新規の接合・計測機器技術等をも含む3Dパッケージング技術について開発し、TSMCジャパン3DIC研究開発センターが産総研のクリーンルームに構築するプロセスラインでの評価・検証を通じて、信頼性の高い組立技術として統合する。

- また、本センターは、日本国内の材料・装置メーカー及び研究機関・大学（下記）とのパートナーシップで強力に取り組む。最先端の技術ポジションを獲得すべく、拡張性があり、製造可能で費用効果の高いソリューションの開発を行う。
(2) 実施者：先端システム技術研究組合（RaaS）※1
事業テーマ：ダイレクト接合 3D積層技術開発（WoWおよびCoW向け装置・プロセス開発）
概要：Cu-Cu の低温ハイブリッド接合による WoW（Wafer on Wafer）接合技術及び CoW（Chip on Wafer）接合技術の構築とその実装化に取り組む。

(3) 実施者：ソニーセミコンダクタソリューションス株式会社
事業テーマ：ポスト 5G エッジコンピューティング向け半導体の 3D 積層要素技術研究開発
概要：積層モジュールの基本特性および信頼性取得が可能となるビッチサイズ目標を年度ごとに設定し、ロパストな半導体製造プロセスの要素技術を確立する。

(4) 実施者：昭和電工マテリアルズ株式会社※2
事業テーマ：最先端パッケージ評価プラットフォーム創成
概要：基板、装置、材料メーカーによるコンソーシアムを創成し、評価プラットフォームを設置し次世代半導体パッケージの評価技術、基板、装置及び材料を開発する。

(5) 実施者：住友ペラクラフト株式会社
事業テーマ：次世代情報通信向け先端パッケージの材料開発
概要：3 次元実装密度向上において重要となる、Wafer Level PKG向け封止材、アンテナ向け封止材、再配線用感光材のファインピッチ対応技術を開発する。
Basic Semiconductor Revitalization Strategy in Japan

**Step 1: Enhancement of Basic Production Capacity for IoT**

- **2020**
  - Smart Home Applicant
  - HomeApplicants
  - Data center, SSD
  - Market size: $500 billion

- **2025**
  - PC
  - Smart Home Applicant
  - HomeApplicants
  - Data center, SSD
  - Market size: $750 billion

- **2030**
  - PC
  - Smart phone
  - Data center, SSD
  - Market size: $1000 billion

**Step 2: Realization of Next Generation Semiconductor Technology through JP-US Collaboration**

(Reference): prepared by METI, based on data from OMDIA

**Step 3: RD For Future technology**

Photonics-Electronics Convergence, Quantum Computing through Global Collaboration
Project Framework for Next Generation Beyond 2nm Project (B2P)

<METI announcement on 11th Nov.>: Establishment of Two Entities for B2P
1. “LSTC”: Open Collaborative R&D Platform (Public Entity) ※Leading-Edge Technology Center
2. “Rapidus”: Mass Production Entity (Inc.)

Mass Production “Rapidus”
- Mass Production Design Function
- Mass Production Line @Rapidus
- Equipment/materials

Open R&D “LSTC”
- R&D for Design Tech
- R&D for Equipments/Materials
- Pilot Line @Rapidus
- Commercialization

■ Oversea Collaboration
- Research Labs & Academia in Like-minded Countries: US NSTC, IBM, IMEC, etc

■ Domestic Collaboration
- Semiconductor User Companies
- Digital Design Labs
- Material & Machinery Companies
- etc

JP Private Companies
- Kioxia, Sony, SoftBank, Denso, Toyota, NEC, NTT, MUFG

JP Academia
- JP National Research Lab

quote: 1111_001a.pdf (meti.go.jp)