

IMAPS DPC 2023

Novel IR Laser Debonding for Heterogeneous and 3D Integration

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EV Group | At A Glance

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductor markets

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1200 employees worldwide

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan



EVG®320D2W

D2W Hybrid Bonding



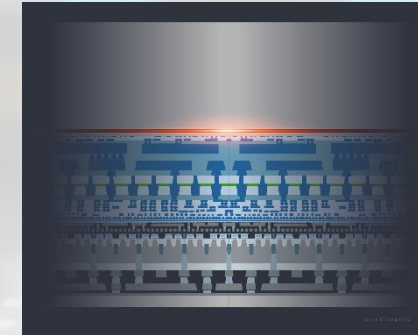
EVG® GEMINI® FB
SmartView® NT3

Hybrid Bonding



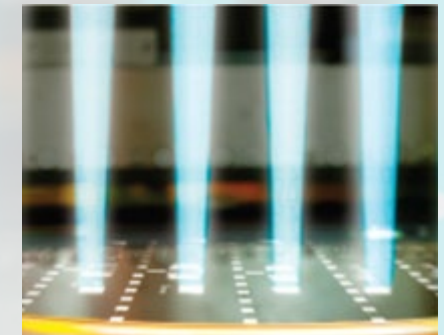
EVG® BONDSscale™

Fusion Bonding



EVG® Nanocleave

IR Laser Release



EVG® Lithoscale
Maskless Exposure Technology

Back-end Lithography

EVG Equipment Solutions | Heterogeneous Integration Portfolio

EVG40NT2

W2W, D2W and D2D
Overlay Metrology for
organic and Inorganic
Dies and wafers



EVG Nanocleave

Selective and full area
IR Laser release through
silicon



EVG GEMINI FB XT

Hybrid Bonding of two FEOL
metallization circuits
<100nm overlay



EVG BONDSCALE

Combination of wafer-to-wafer
bonding and EUV or
Immersion
lithography



EVG320D2W

D2W Fusion and
Hybrid Bonding
using CoD2W
or DPD2W flows



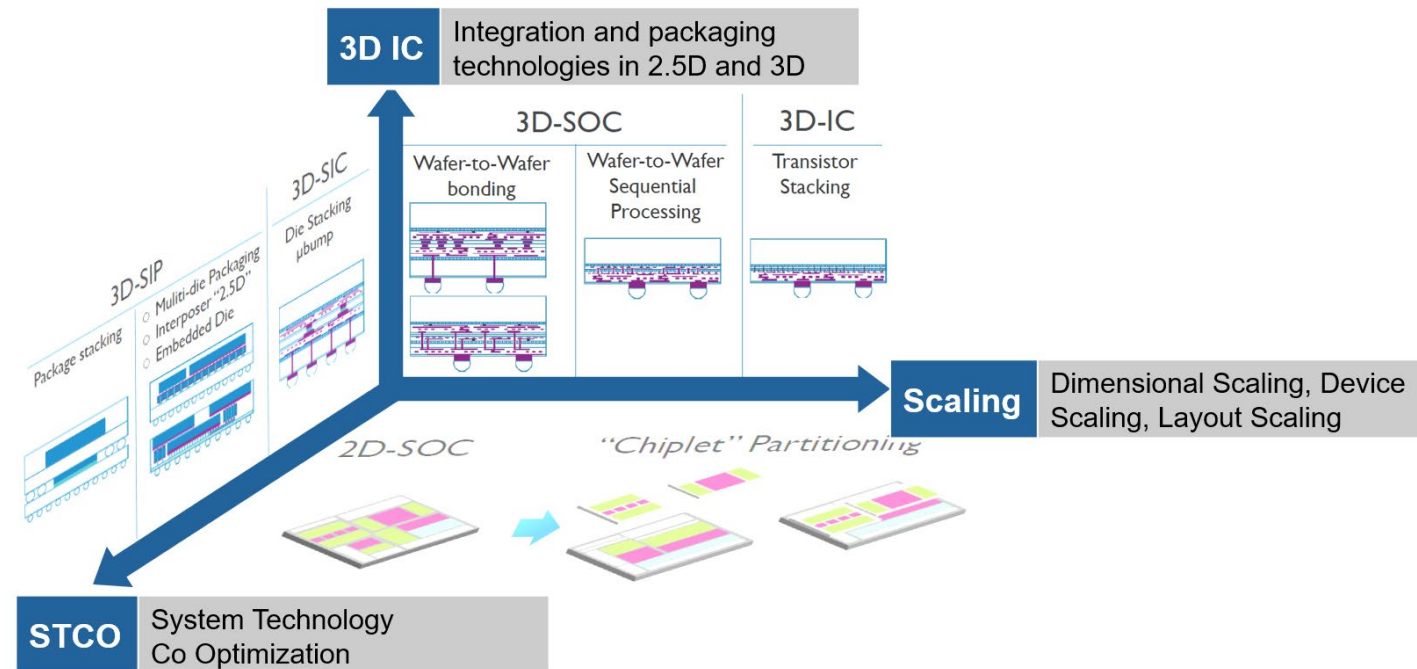
EVG Lithoscale

Fully digital maskless
Lithography for
Adaptive patterning
Rapid prototyping &
fully traceable chiplets

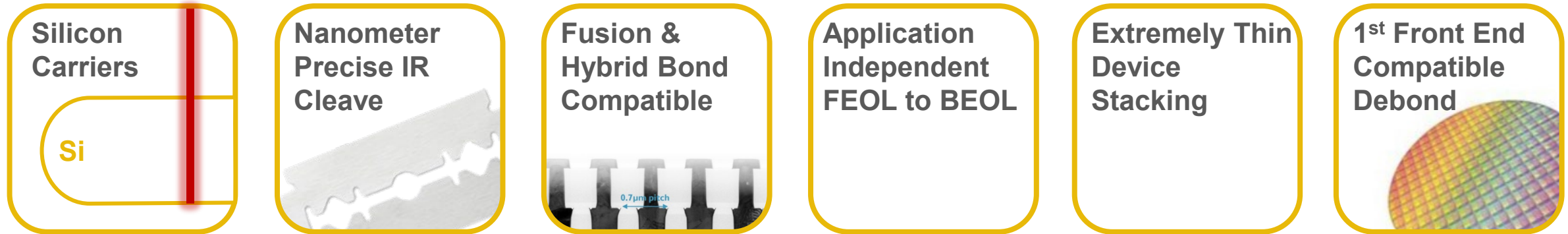


EVG850 TB/DB

Temporary Bonding &
Debonding for next
FoWLP, 2.5D and 3D
processes

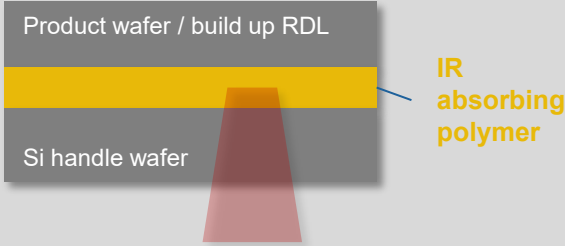
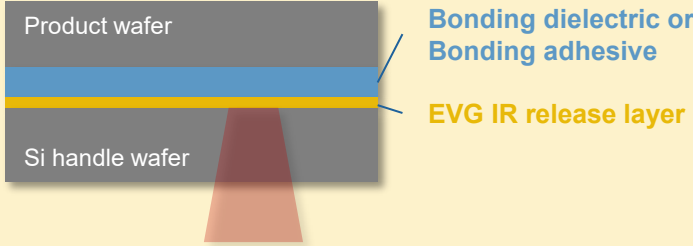
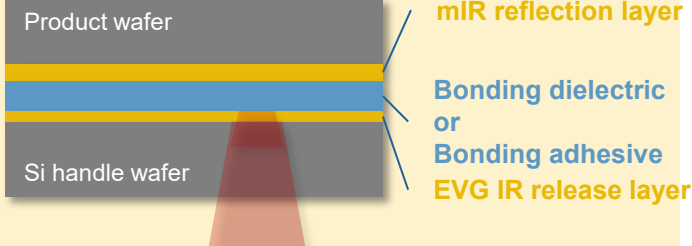


What is NanoCleave?



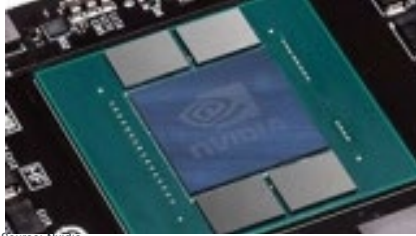
- Novel & universal IR release technology through silicon wafers
- Inorganic IR release layers with nanometer precision separation trigger
- Applicable to all carrier technologies ranging from advanced packaging to 3D integration to future scaling FEOL integration
- Enables die and wafer thicknesses $\ll 10\mu\text{m}$ for improved PPACt
- Process flow qualified with first customers for multiple applications with first orders received

Application and Integration Options

	Previous Option	Nanocleave: Option 1	Nanocleave: Option 2
			
Principle	Volumetric Polymer Absorber	Thin IR release layer	Thin IR release layer with mIR back reflection
Release Mechanism	Volume absorption and decomposition of polymeric matrix using inorganic absorber particles	IR release layer based on metal-inorganic absorbing layers	IR release layer based on metal-inorganic absorbing layers
Bonding Options	Bonding is optional but IR absorber can be used as build up layer as well	Can be combined with various bonding polymer layers (temporary and permanent adhesive layers) or inorganic bonding dielectrics such as SiO2 or SiCN	Extension to Option 1 in order to boost IR absorption changing the absorption properties
Applications	Back end compatible for Fan-out WLP and low cost interposer	3D integration processes for ultra thin die, layer transfer or high density interposers with dual damascene	3D integration processes for ultra thin die, layer transfer or high density interposers with dual damascene

EVG Nanocleave | Applications

→ Memory Stacking



Source: Nvidia

Wafer support during thinning and backside processing before stacking of DRAM or SRAM

- thinner layers ($\ll 40 \mu\text{m}$),
- combination with hybrid bonding

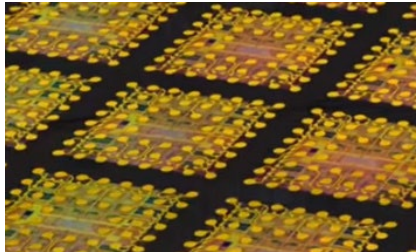
→ Image Sensors



Source: Sony

Film Transfer for next generation image sensors (enhanced spectrum)
Splitting of pixel transistor and photodiode in two layers
Global Shutter implementation

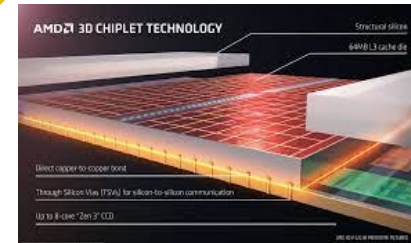
→ FoWLP



Source: Brewer Science

Release for RDL first
Temporary bonding for warpage control for chip first enables thinning and backside processing

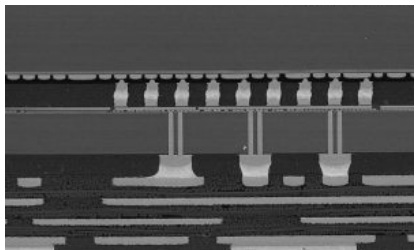
→ D2W Hybrid Bonding



Source: AMD

Advanced carrier technology for Co-D2W, DP-D2W and Reconstructed W2W

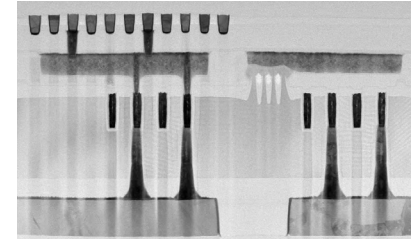
→ Interposer



Source: SystemPlus Consulting

Thinning of interposers, enhanced process temperatures for passive integration and high density RDLs for HPC & AI applications

→ Scaling Booster for thin film transfer



Source: IMEC ITP2022

Ultra thin layer transfer for sequential device flows:

- Silicon thin films for BS-PDN, sequential CFET, hybrid CFET, etc.
- Epitaxial layers such as III/Vs
- 2D Materials such as MX2 or graphene

FoWLP & 2.5D Interposer

Use Case

Industry Challenge

■ 2.5D Interposers

- Integration density in terms of RDL patterning is decreasing to less than 500nm for high performance compute applications
- Integrated passives demand high process temperatures for dielectric deposition and etching ($>300^{\circ}\text{C}$)
- Carrier systems on silicon are restricted to thermoplastic and thermoset materials (thermal limit 270°C)
- Glass carriers and UV laser debonding demand many additional process steps such as backside of bevel deposition to run glass wafers in 300mm lines

■ FoWLP

- Carrier systems based on glass face integration density issues on polymers
- Next generation high performance processes are going to use dual damascene and therefore demand excellent TTV and flatness
- Chucking and thermal conductivity issues for glass

- Applications:
 - 2.5D and 3D thin wafer processes
 - Fan-Out carriers for both chip-first and chip-last process flows

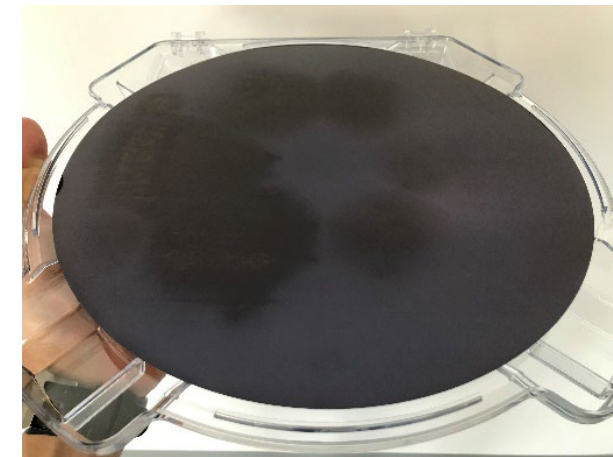
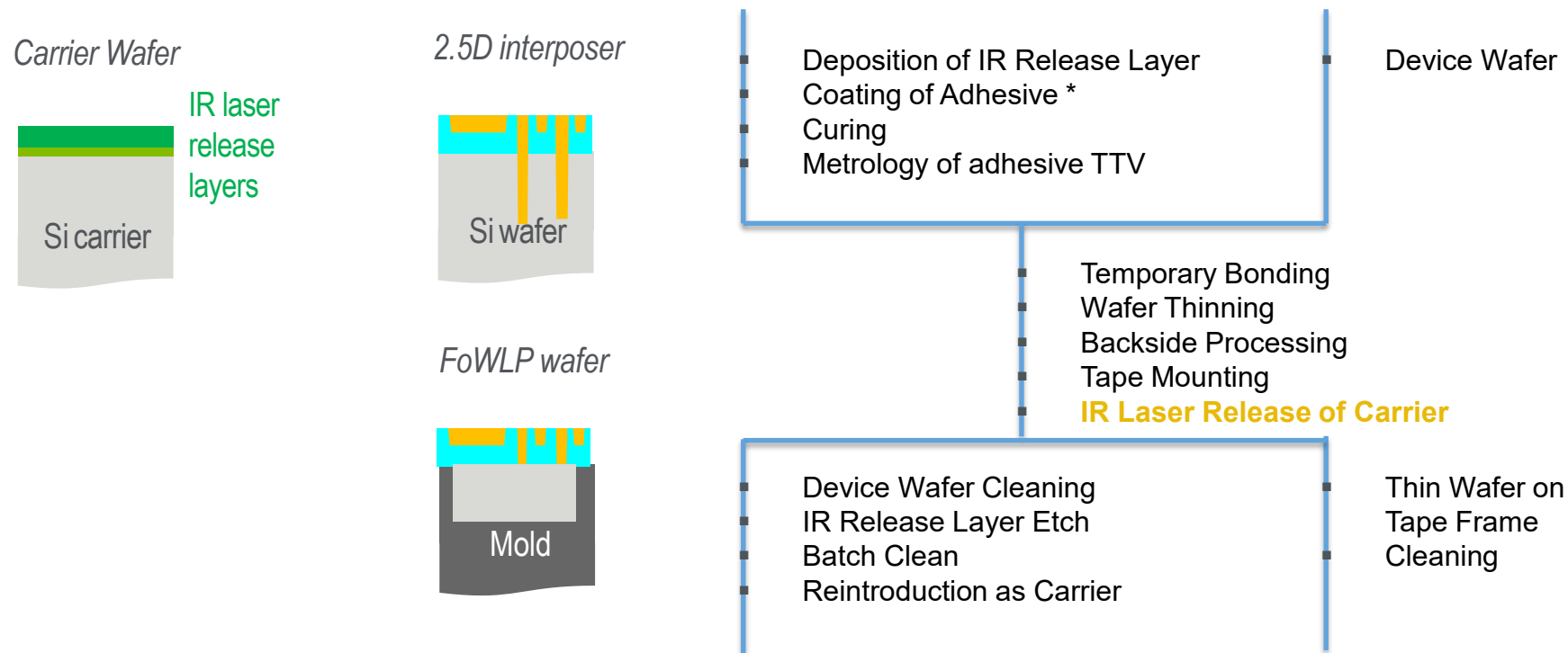


Image of a 300mm FoWLP after IR laser release from a silicon carrier wafer

D2W Hybrid Bonding

Use Case

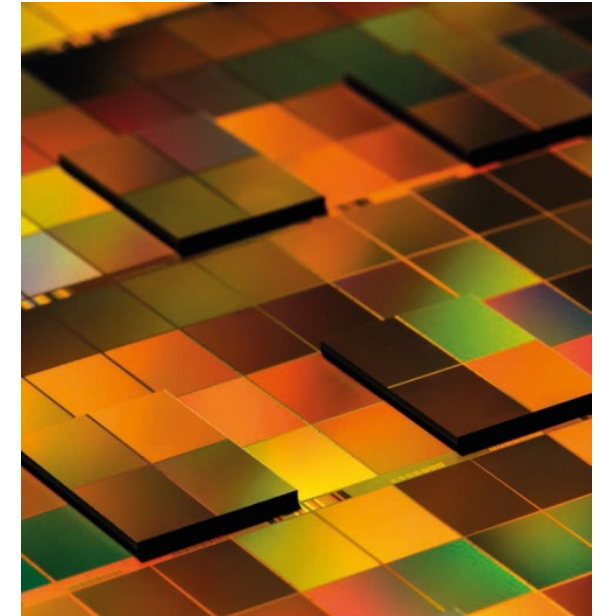
IR Laser Release | **Reconstructed D2W Bonding**

Industry Challenge

- D2W Fusion and Hybrid bonding demands ultra clean die handling and placement (particle control is not solved up to now)
- W2W bonding offers cleanliness and process yield however not known-good-die option
- Ultrathin die stacking with $<40\mu\text{m}$ is not feasible without carrier technology and wafer level thinning

Solution

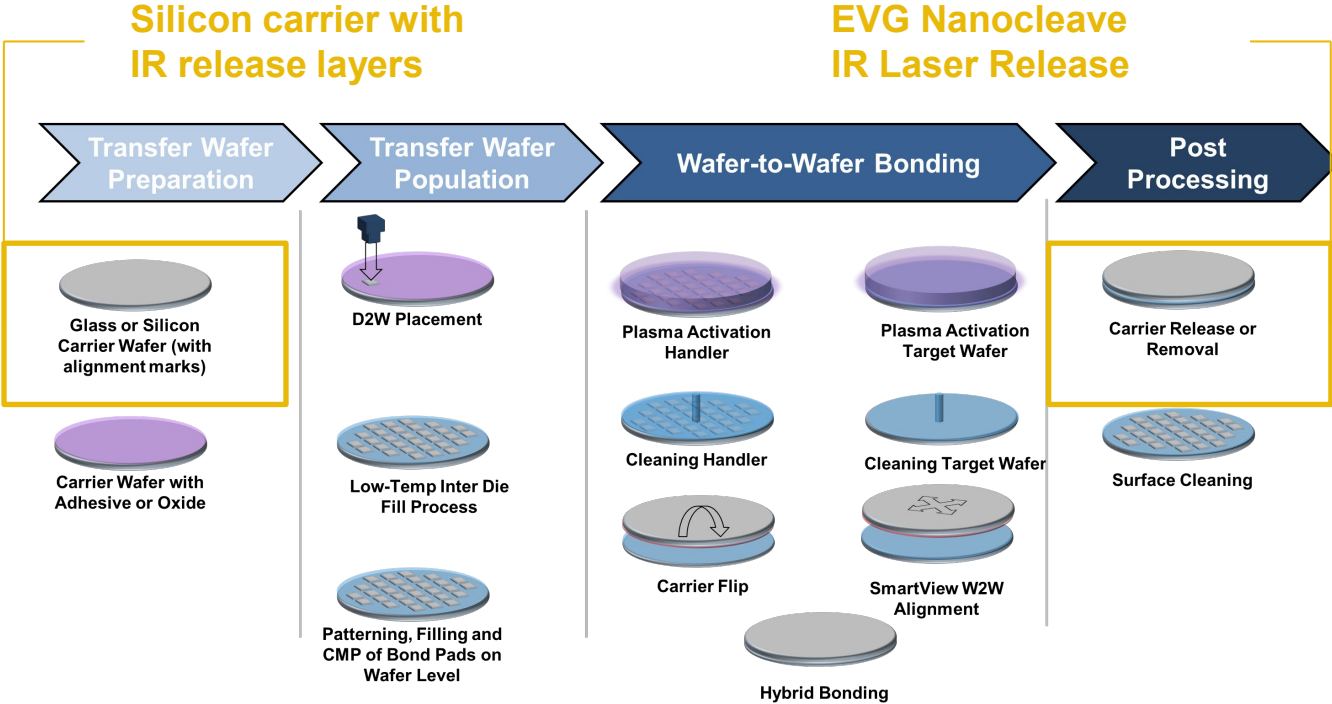
- Reconstructed wafers combine known good die placement, filling with dielectric between dies and subsequent hybrid bond wafer level patterning





IR Laser Release | Reconstructed D2W Bonding

	Reconstituted W2W
Transfer Method	Reconstructed W2W (Anorganic Fill Process)
Pro's	<ul style="list-style-type: none">Proven technologyDie Activation and cleaning equivalent to W2W hybrid bondingOxide managementRework on carrier feasible
Con's	<ul style="list-style-type: none">Error propagation of D2W + W2W alignmentCost of carrier prep, utilization and cleanDie thickness needs to be in narrow range
Maturity	Limited volume production proven for several years





IR Laser Release | Reconstructed W2W Bonding

<div>Flow 1</div> <div>Face up die placement</div>				
Limited to die thickness	Silicon Release Carrier deposition (including plating layers, bonding layers and alignment marks)	Face Up die D2W Bonding	Interlevel dielectric fill and interconnect patterning	Reconstructed W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG Nanocleave)
<div>Flow 2</div> <div>Face down die placement</div>				
Enables down to single digit μm die thickness generating know good wafers for fusion and hybrid bonding	Silicon Release Carrier deposition (including plating layers, bonding layers and alignment marks)	Face Down D2W Bonding	Interlevel dielectric fill, wafer level thinning, and interconnect patterning	Reconstructed W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG Nanocleave)

Hybrid Bonding F2B

Use Case

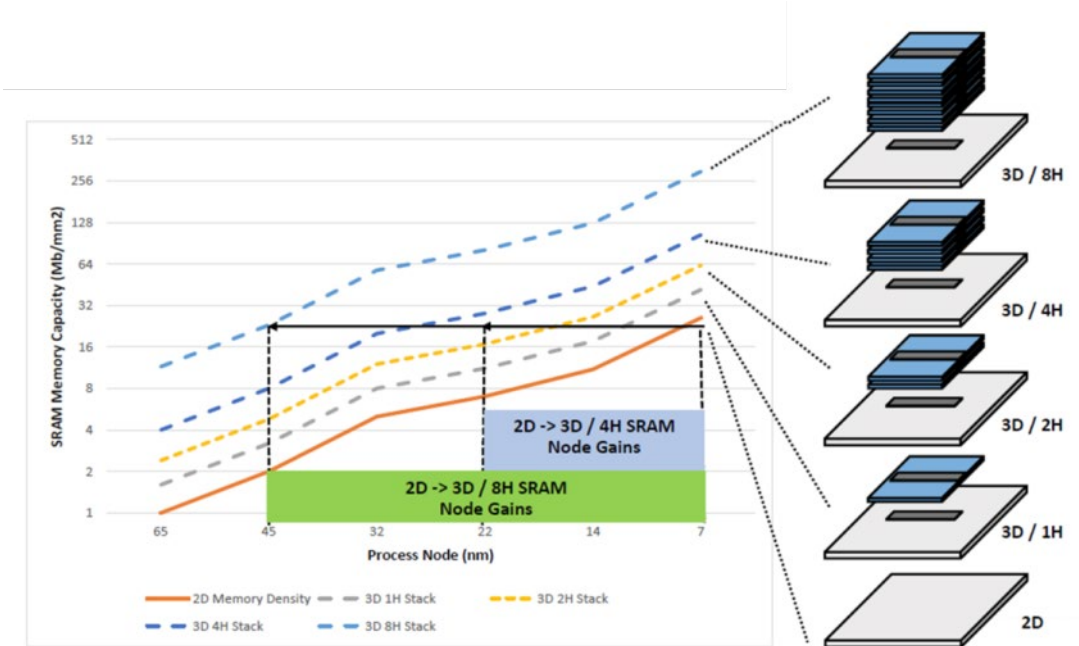
IR Laser Release | Hybrid F2B Bonding

Current Industry Issue

- SRAM Cache integration demands F2B stacking of multiple memory layers (F2F would require redesign of each wafer and hence no option)
- Sequential Wafer stacking in adding thermal process load consecutively as well as inventory of line / product risk increasing

Solution

- Nanocleave enables ultrathin SRAM layers
- Individual layers are prepared on carrier and subsequently bonded & IR released

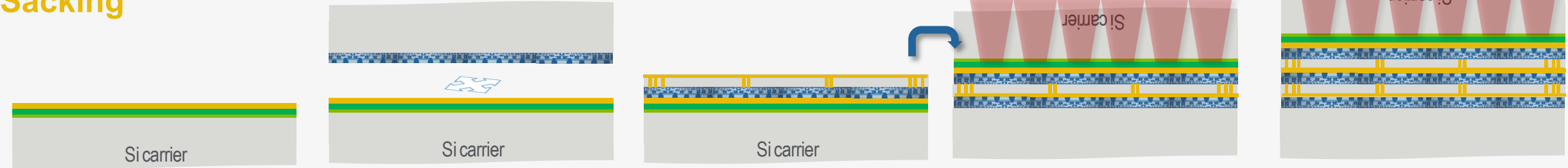


SRAM on Logic



IR Laser Release | F2B Hybrid Bonding

F2B Layer Sacking



Silicon Release Carrier deposition (including plating layers, bonding layers and alignment marks)

Face Down Bonding to IR release carrier wafer

Wafer thinning, TSV etching, hybrid bond pad patterning, CMP

Base + 1 Stacking: W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG Nanocleave)

Base + 2 Stacking: W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG Nanocleave)

Ultra Thin Layer Transfer MX2 or Graphene 2D Material Transfer

Use Case

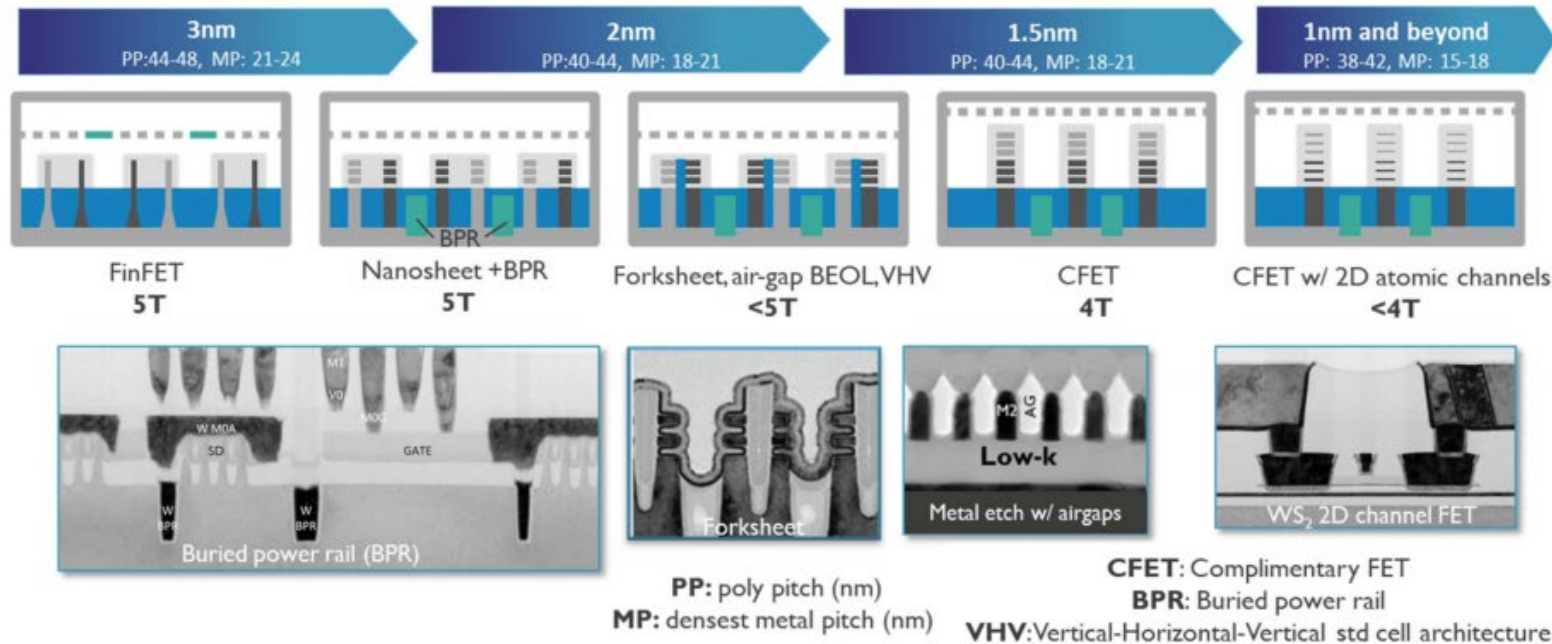
IR Laser Release | Ultra Thin Layer Transfer

Current Industry Issue

- Ultra thin layer transfer can only be enabled using several processes using grinding, polishing and ion etching, being limited by wafer TTV and mainly grinding uniformity
- Implantation and low temperature cleaving is only working on native silicon wafers

Solution

Nanocleave enables novel process flows to support the scaling roadmap

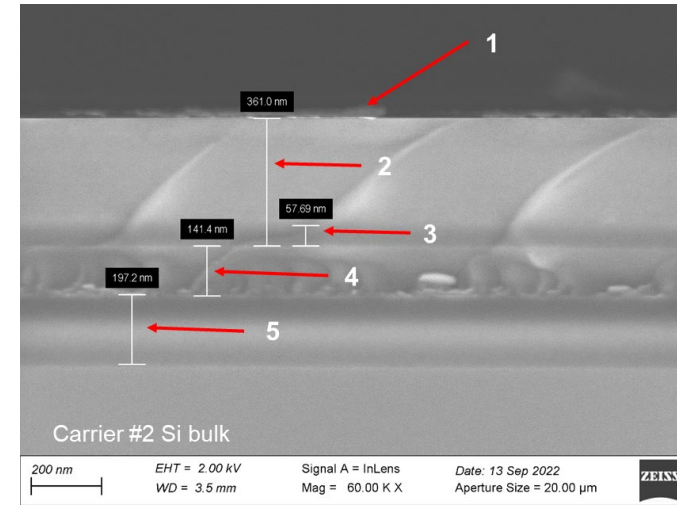
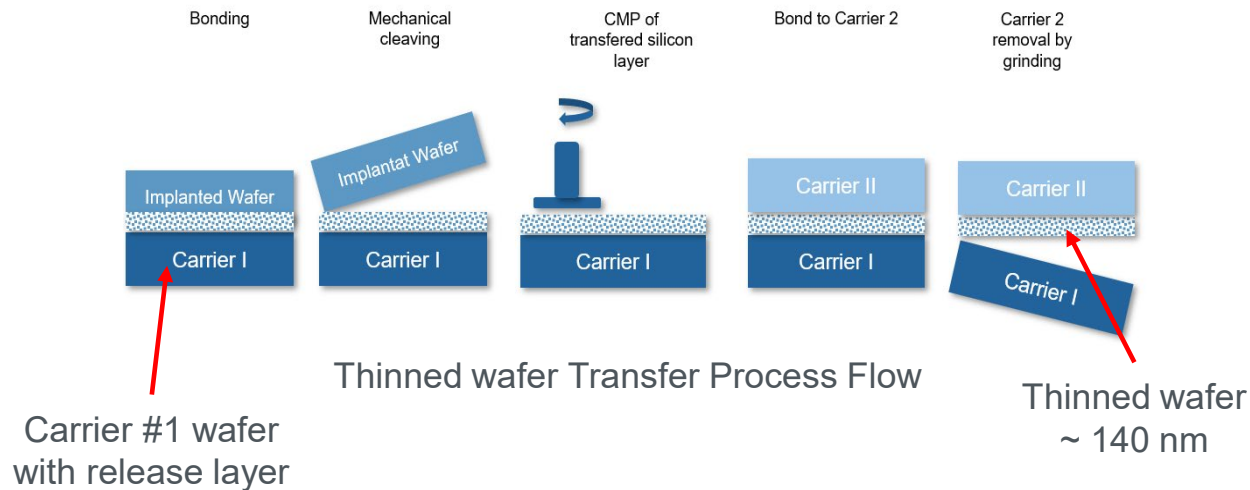


- BSPDN is here to stay
- CFET manufacturing is expected to benefit from wafer bonding
- 2D materials will require thin layer handling (Bond, debond / release, etc.)

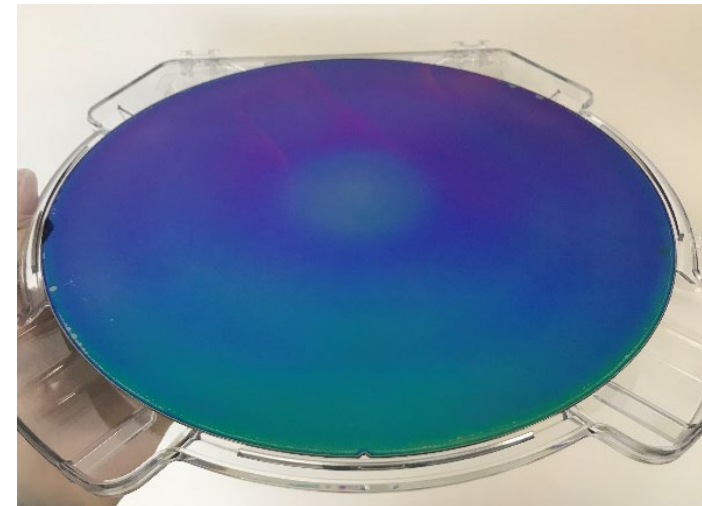
NanoCleave™ | Achievements

Ultra thin wafer transfer

Layer transfer Process Demonstration



Transferred thin wafer, XSEM image



300 mm transferred DB interface wafer

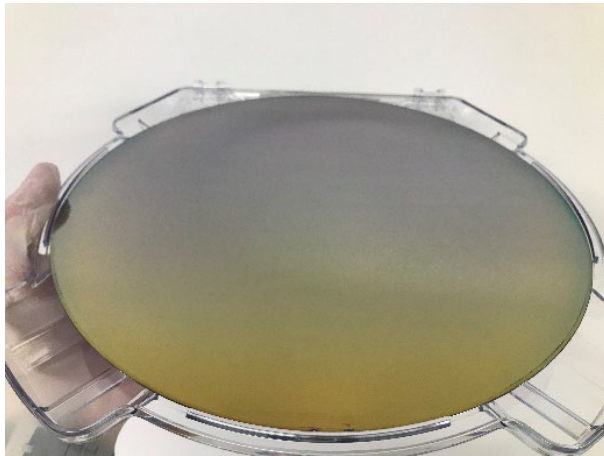
NanoCleave™ | Achievements

Fusion bonded
stacks release

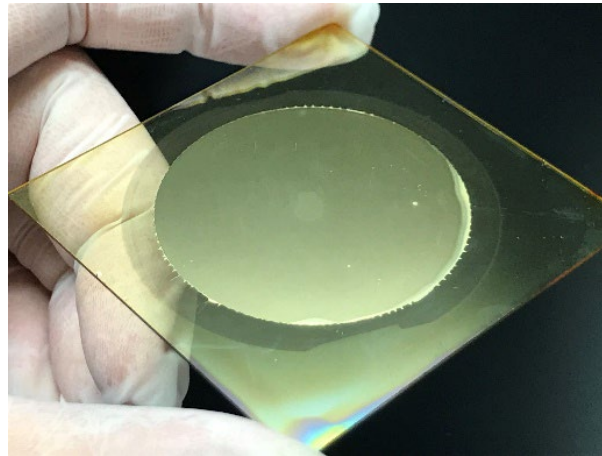
Direct deposited
layer release

Overmold release

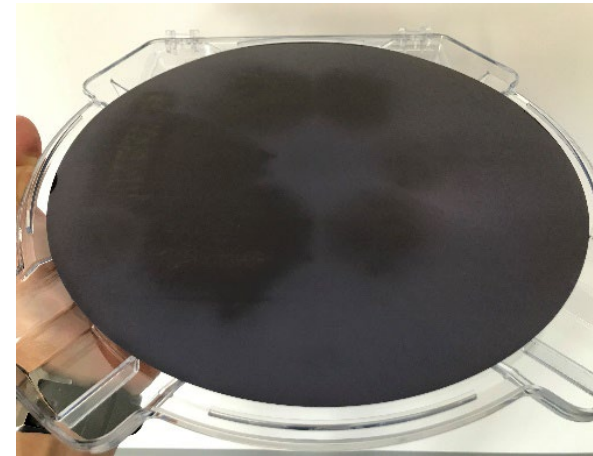
Temporary bond
release



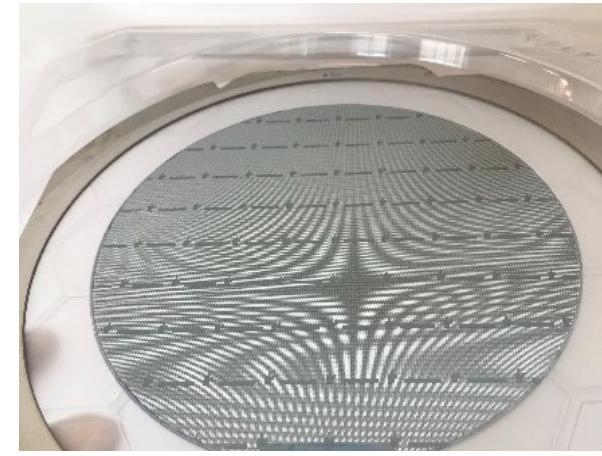
300 mm fusion bonded pattern
device wafers release



Graphene layer transfer from
Sapphire carrier



300 mm reconstituted (FOWLP)
wafer release



200 mm temporary bonded thin
device wafer release

- With NanoCleave carrier wafers, various bond types can be separated.

Summary

W2W Hybrid Bonding

EVG is market leader for W2W hybrid bonding equipment with more than 80% market share over the last 2 years

EVG fusion and hybrid bonding equipment in W2W bonding is standard process in major IDM and Foundries

Sub 100nm W2W overlay accuracy developed and currently moved in high volume production

D2W Hybrid Bonding

Several Process Integration schemes are present in the market today with application specific pros and cons

Enabling wafer based cleaning, activation and processing equipment for D2W hybrid bonding for full process transferability from W2W

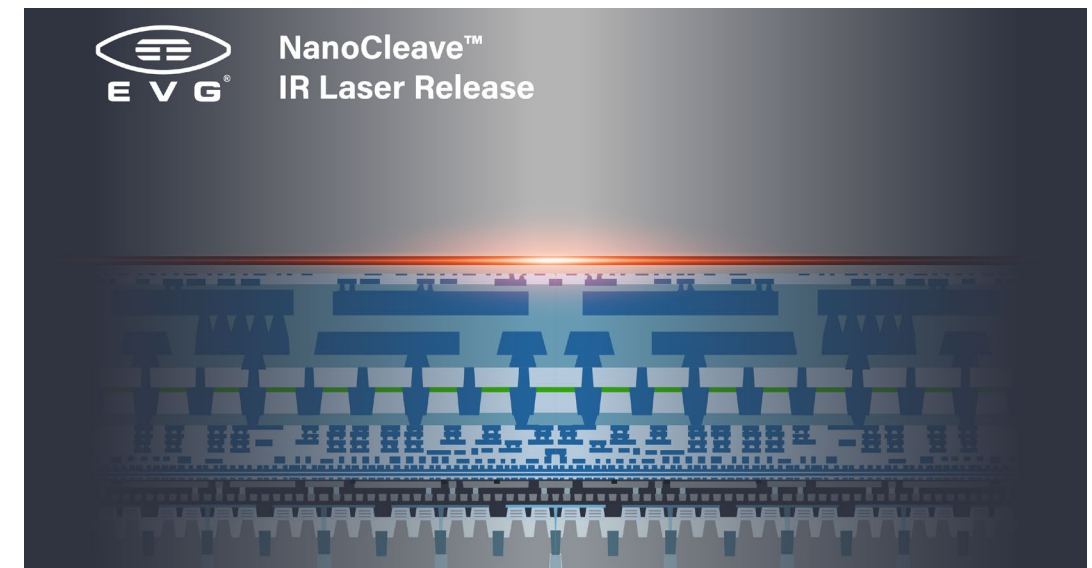
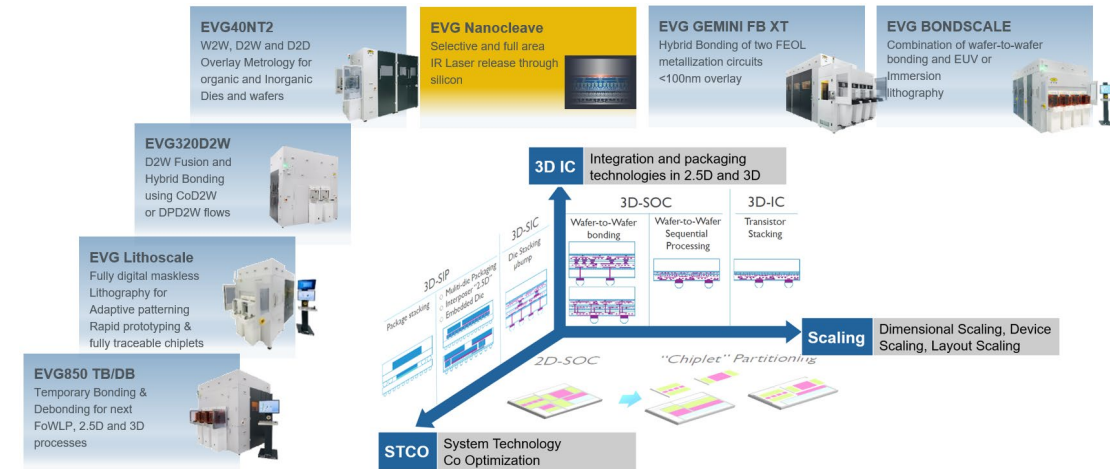
EVG320D2W Fully integrated system solution with standardized process modules

IR Laser Release – EVG Nanocleave

Novel & universal IR release technology through silicon wafers

Precisely controlled cleaving without IR transmission or risk for product

Inorganic IR release layers with nanometer precision separation trigger



Heterogeneous Integration Competence Center | Launch 2020

ST. FLORIAN, Austria, March 2, 2020

“Heterogeneous integration fuels new packaging architectures and demands new manufacturing technologies to support greater system and design flexibility, as well as increased performance and lower system design costs,” stated Markus Wimplinger, corporate technology development & IP director of EV Group.

“EVG’s new HI Competence Center provides an open access innovation incubator for our customers and partners across the microelectronics supply chain to collaborate while pooling our solutions and process technology resources to shorten development cycles and time to market for innovative devices and applications enabled by heterogeneous integration.”

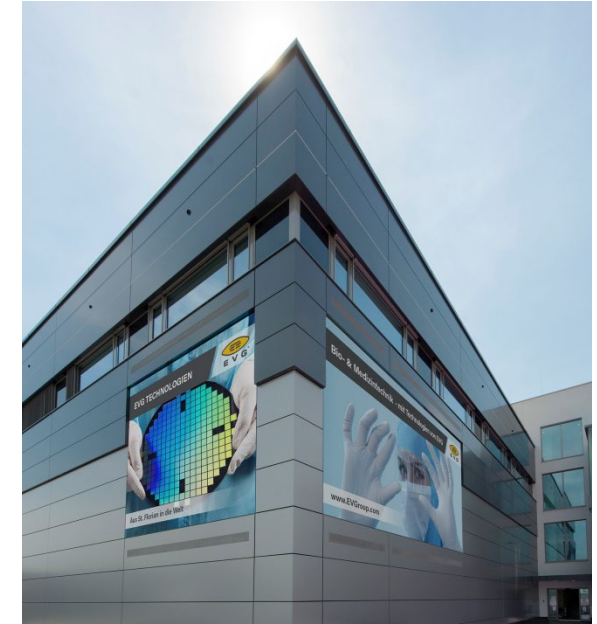
Facility-Infrastructure

IT-Infrastructure

Risk Reduction

Process Development

Process Transfer





NanoCleave™ IR Laser Release

IR laser-initiated release of any ultra-thin film or layer from silicon carriers with nanometer precision

Front-end compatible carrier technology for further integration of fusion and hybrid bonding processes

Revolutionizing 3D and heterogeneous integration as well as material transfer in next-generation scaled transistor designs

Enabling silicon carrier wafers in advanced packaging processes such as FoWLP and 3D SiC