Performance Enablement Through VIPack FOPOP for Mobile and Networking

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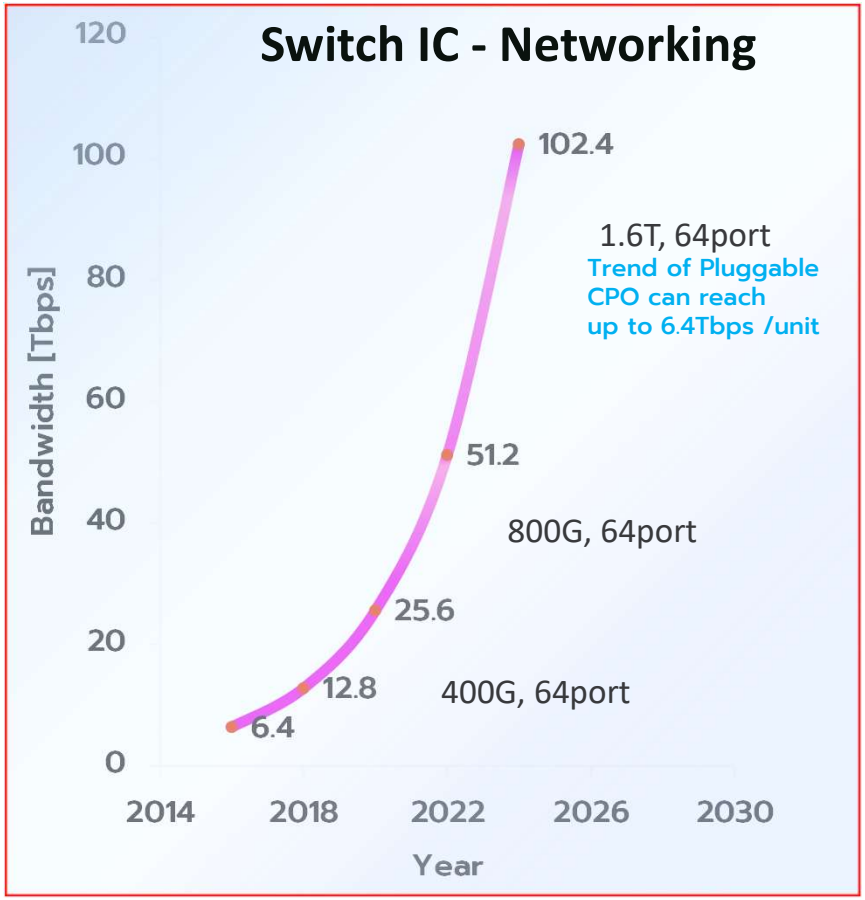
March 2023

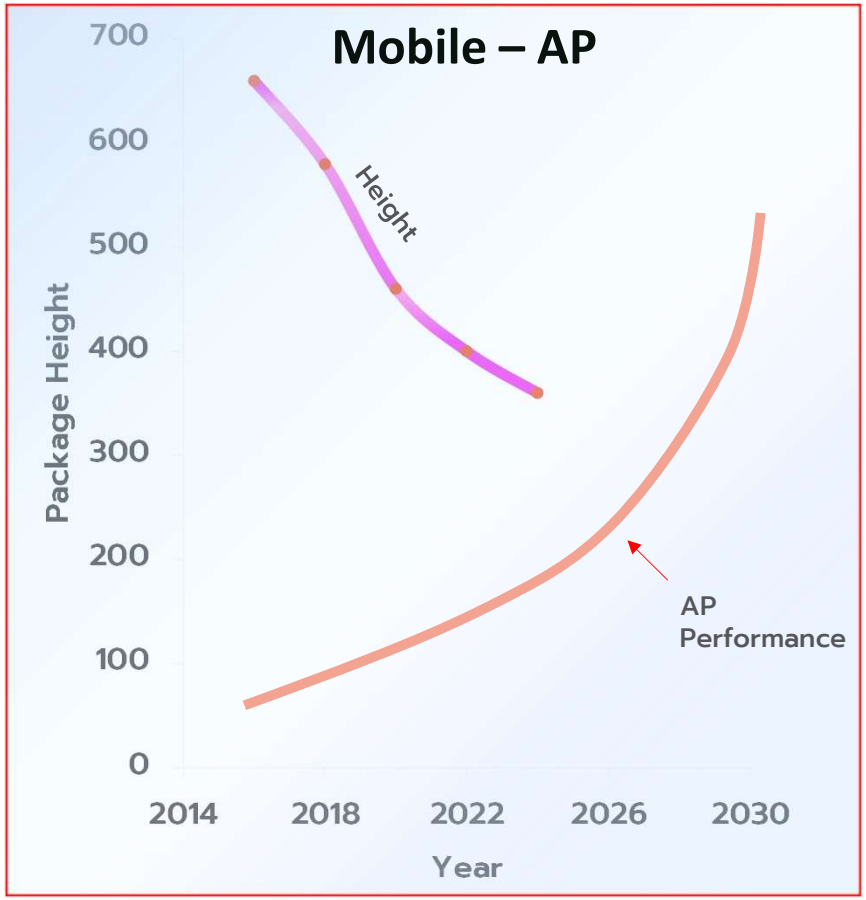
aseglobal.com

Outline:

- Market Drivers
- Mobile & Network Performance Driver and Solutions
- SiPh FOPOP Sub Module & Key Attributes
- Electrical and Thermal Modeling Simulation
- Wafer Level Optical Test
- Conclusion

Market Drivers

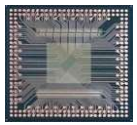
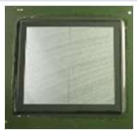


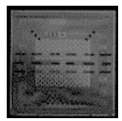
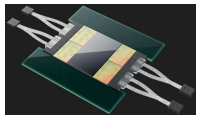


Vertically Integrated Package Platform - VIPack™

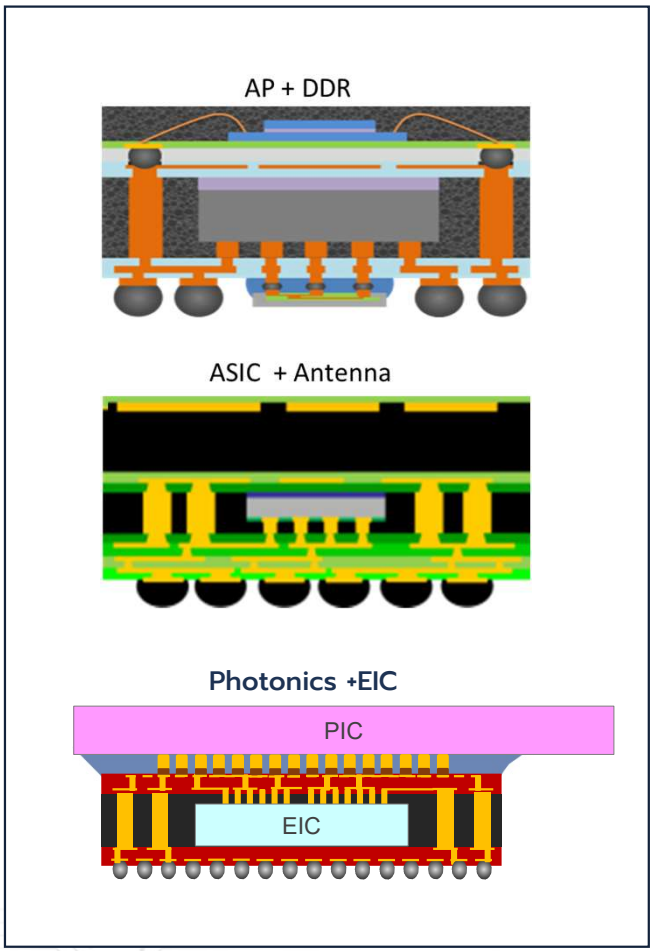
VIPack™

I	II	III	IV	V	VI
FOPoP	FOCoS	FOCoS – Bridge (Embedded)	FOSiP	2.5D/3D IC	Co-Packaged Optics
Integrated Design Ecosystem					

FOPOP Mobile & Networking Performance Enablement



Application:

- *AP + DDR Memory (4G/5G)*
- *ASIC + Antenna (5G)*
- *SiPh + EIC (Networking)*

Development Features:

Mobile:

- *Thinner Form Factor*
  HBPoP ~550um ***FOPoP below 400um***
- *TMV + Double-side RDL Layer*
- *Thin passive IPD integration*
- *Heterogeneous surface grinding*
- *Wafer form memory stacking*
- *Embedded Molding Structure*
- *Lower Impedance/Insertion Losses in RDL vs HBPOP*

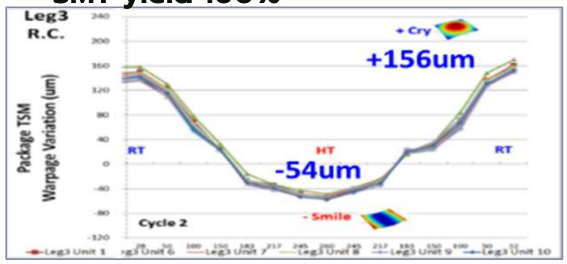
Networking:

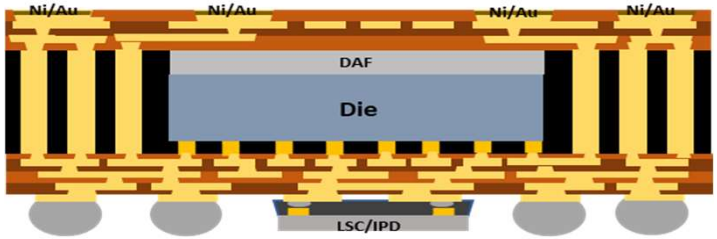
- *Reduced Critical Lengths between PIC/EIC*
- *XY Size Reduction for additional sub-module integration*
- *Advanced Process Technology for Photonic Die Etching & Plating*
- *Bandwidth Density Enablement (Size, Critical Length Reduction)*

Mobile Performance Drivers & Solutions

Mobile Applications Processor – Device Example

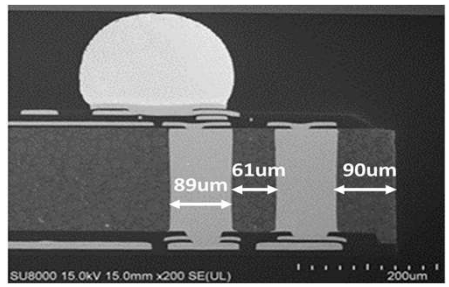
- ✓ PKG warpage H.T 54um (Goal: <80um)
- ✓ SMT yield 100%



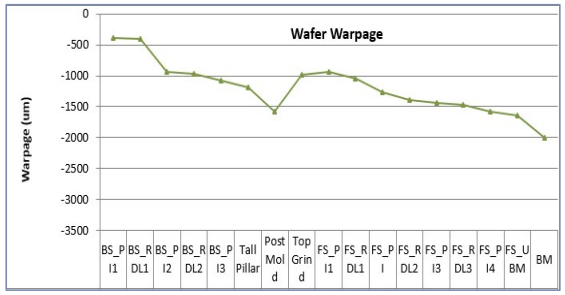


- ✓ PKG THK 389um (w/ ball)
- ✓ Die THK 135um
- ✓ DAF THK 25um
- ✓ Cu stud 20um
- ✓ Cu post pitch 150um
- ✓ Solder ball 135um
- ✓ RDL L/S 5/5um
- ✓ RDL THK 5um
- ✓ PI via 15um
- ✓ PI THK 5um (on RDL)
- ✓ Die to pillar 110um
- ✓ FS & BS-RDL 35/39um

- ✓ 150um pitch Cu pillar w/ 180um THK
- ✓ Tall pillar to PKG edge is 90um (<100um)

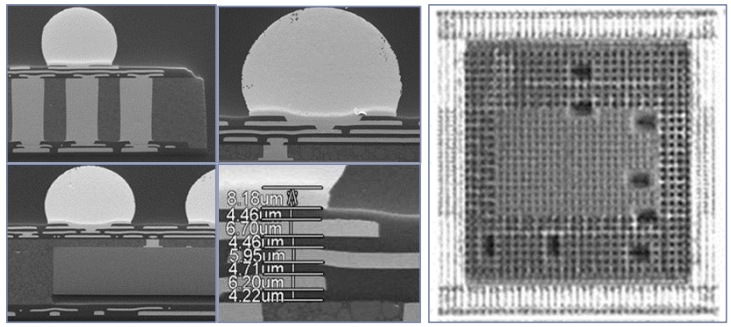


- ✓ PNL warpage 0.5~2.0mm (Goal: <2.5mm)
- ✓ No handling issues

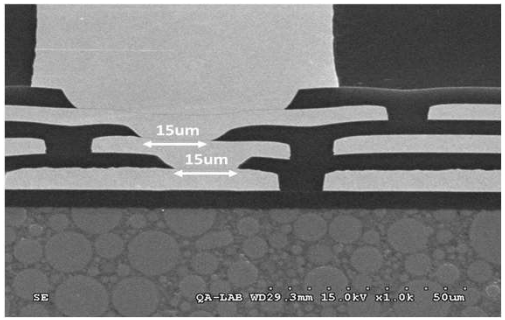


- ✓ No delamination be found

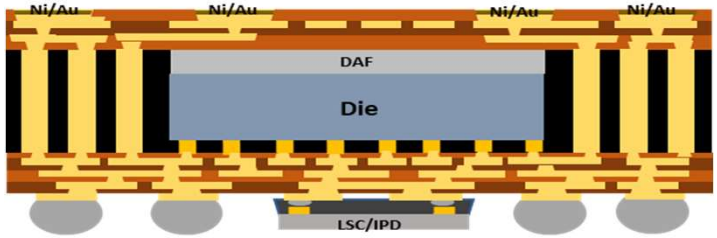
SAT 100% pass



- ✓ PI via 15um
- ✓ RDL flatness on stacked via w/out dimple



Reliability Test Result of FOPoP



☐ L0 CLR / BLR / Drop test passed

CLR

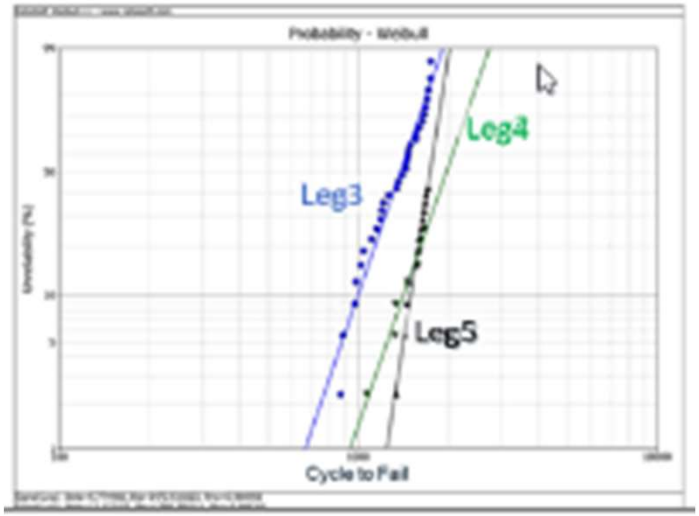
130°C/85%RH CondB—55C-125C

CLR	T0 SAT	MSL1		uHAST192		TCT1000	
		O/S	SAT	O/S	SAT	O/S	SAT
	0F/90	0F/90	0F/90	0F/45	0F/45	0F/45	0F/45

BLR

—40C to 85C

WR Leg #	BS_Cu Ratio RDL1/2	PCB Side	UF	Net	Cycle Count	# of Fails	2-P Weibull Statistics				
							First Fail	5%	50%	63.20%	Beta
3	69.12%/73.5%	A	No	Signal	1774	30F/30	875	880	1382	1473	5.77
4	68.93%/73.3%	A	No	Signal	1774	13F/30	1340	1414	1737	1788	12.63
5	65%/65%	A	No	Signal	1774	8F/30	1068	1248	1970	2100	5.71



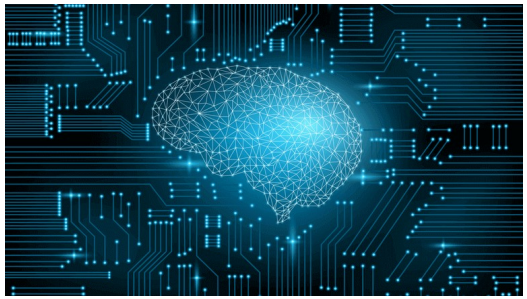
Drop Test

WR Leg #	BS_Cu Ratio RDL1/2	PCB Side	UF	Net	Cycle Count	# of Fails	2-P Weibull Statistics				
							First Fail	5%	50%	63.20%	Beta
3	69.12%/73.5%	A	No	Signal	30	0F/60	-	-	-	-	-
4	68.93%/73.3%	A	No	Signal	30	0F/60	-	-	-	-	-
5	65%/65%	A	No	Signal	30	0F/60	-	-	-	-	-

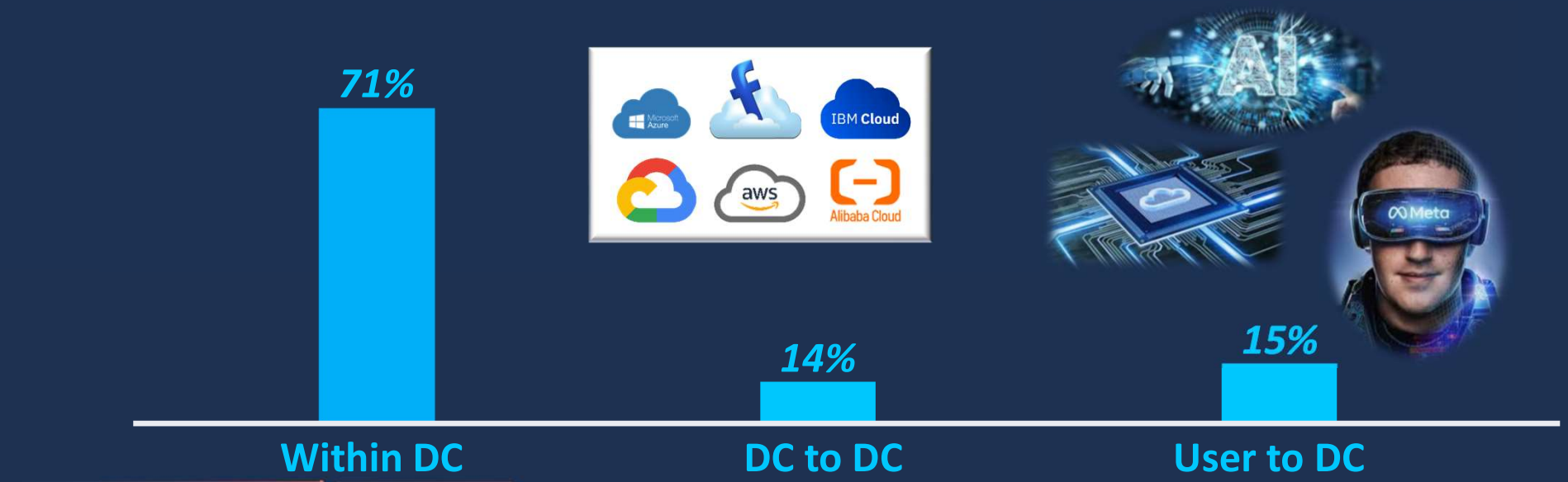
Networking Drivers and Solutions

Emerging Application Markets






Year	Global Internet Traffic
1992	100 GB per day

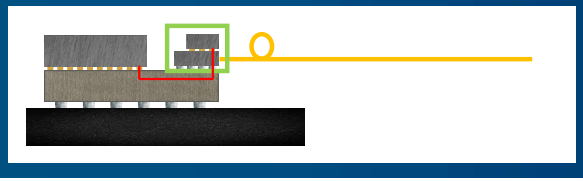


[Ref] Cisco 2020 Whitepaper 2020

Speed Evolution

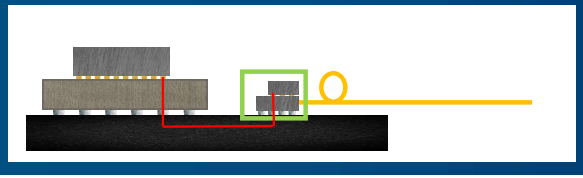
Replace Cu with Optics

Co-packaged Optics



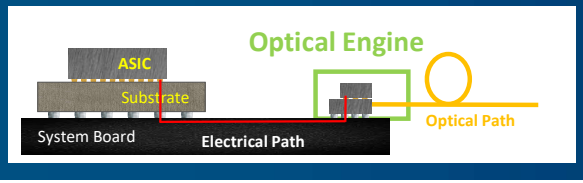
Engine Speed ~6.4Tbps
Energy efficiency <5pJ/bit

On-board Optics



Engine Speed ~ 1.6Tbps
Energy efficiency ~20pJ/bit

Pluggable Optical Transceiver

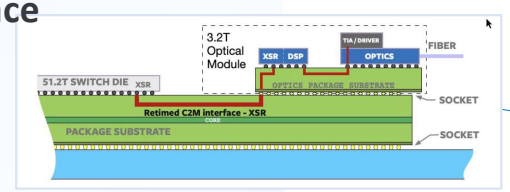


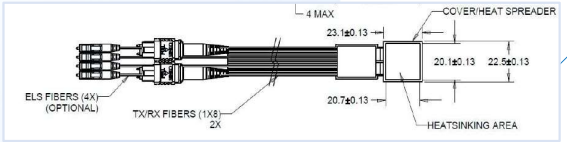
Engine Speed < 400Gbps
Energy efficiency ~25pJ/bit

Background: Co-packaged Optics (CPO)

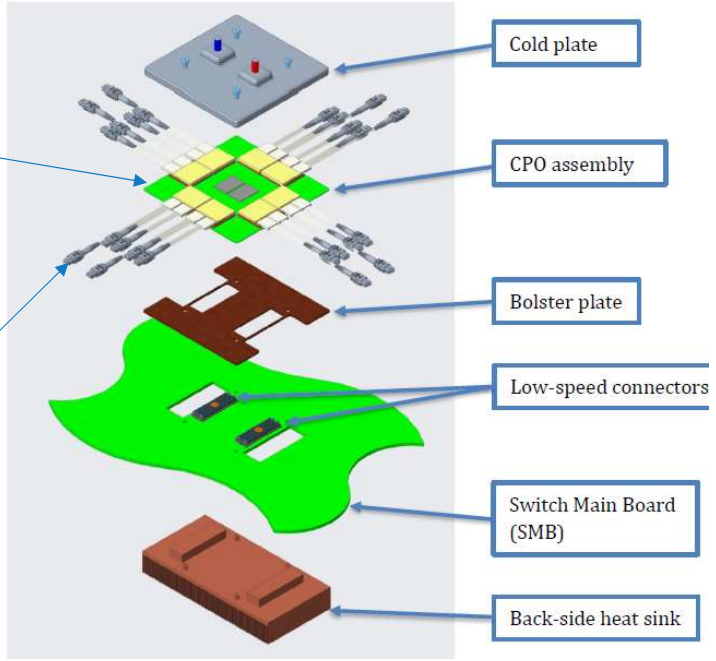
System-level Requirements

- **Switch IC to Optical Electrical Interface**
  - CEI-112G-XSR
- **Optical Fiber Connections**
  - TX/RX fibers 2x (1x8) for 3.2T module
  - ELS fiber 4x for 3.2T
  - Total fiber count : 320
- **Power:**
  - Switch- 51T : 900W
  - Optical: 1024W, 128 x 8W/400G
  - Underside voltage regulators
- **Thermal Considerations**
  - Top surface components cold plate with water-cooled solution
  - Underside heat sink: contact the voltage regulators



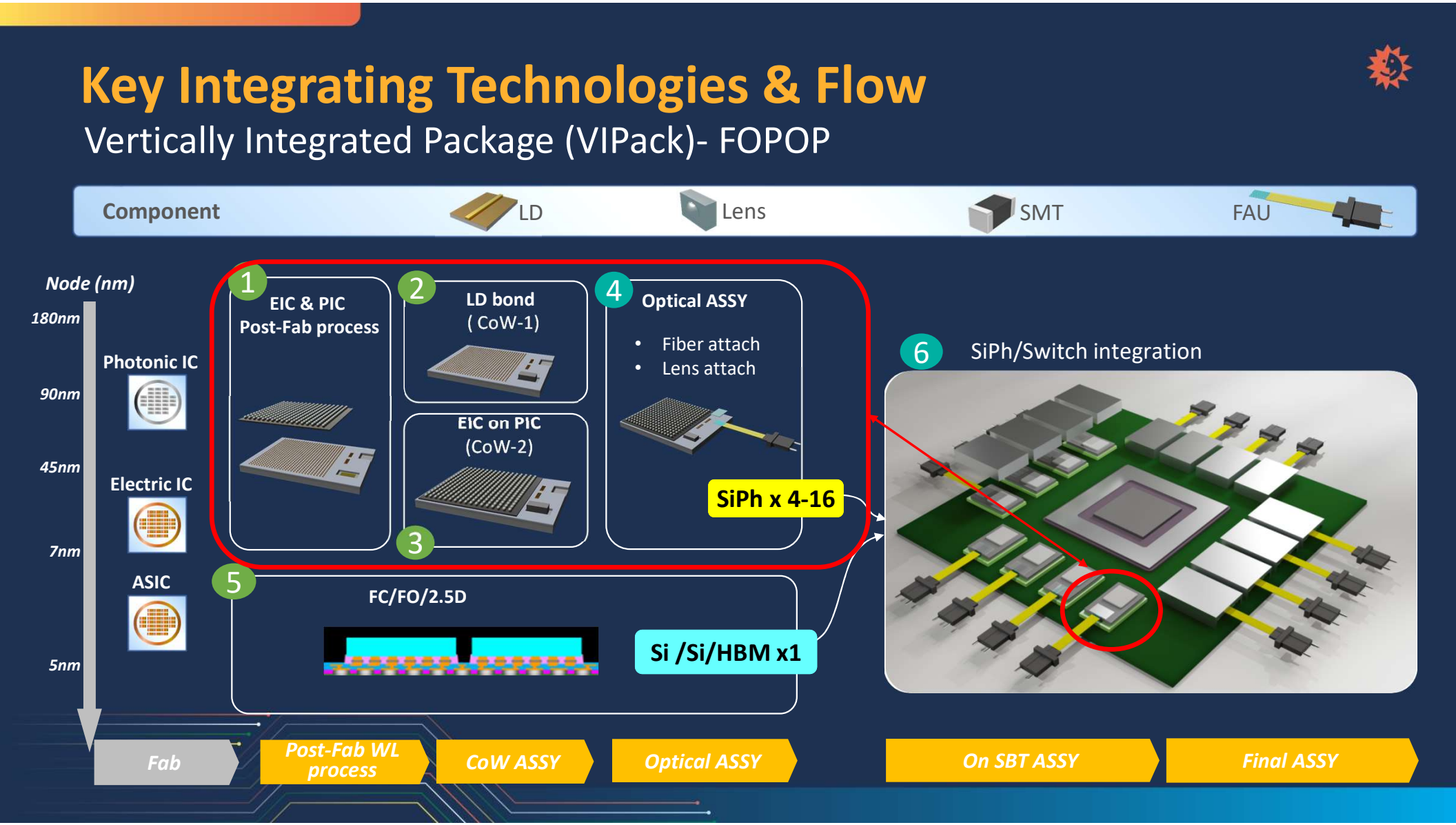


Ref: Co-Packaged Optic Assembly Guidance)
www.copackagedoptics.com



Key Integrating Technologies & Flow

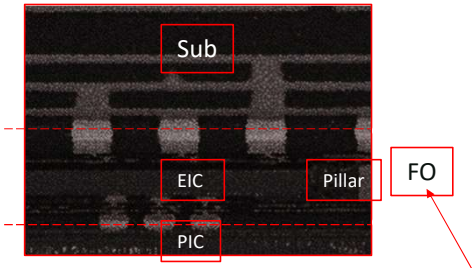
Vertically Integrated Package (VIPack)- FOPOP



Key Integrating Technologies

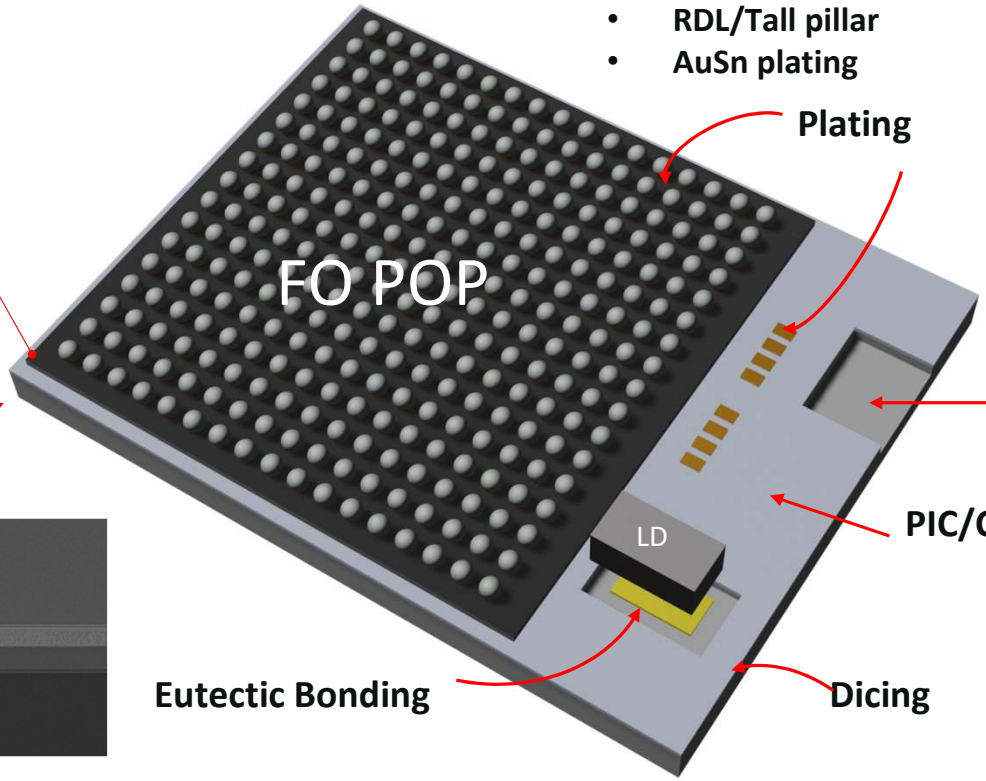
Post-CMOS Process

- **UBM**
- **Cu Pillar**
- **RDL/Tall pillar**
- **AuSn plating**

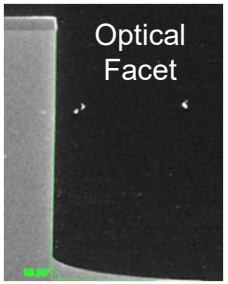


FO

FCB/Reflow
TCB

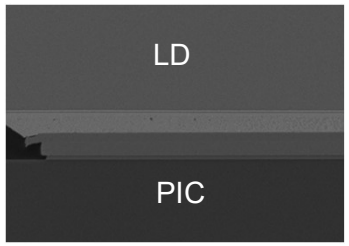


Plating



O/Si Etch

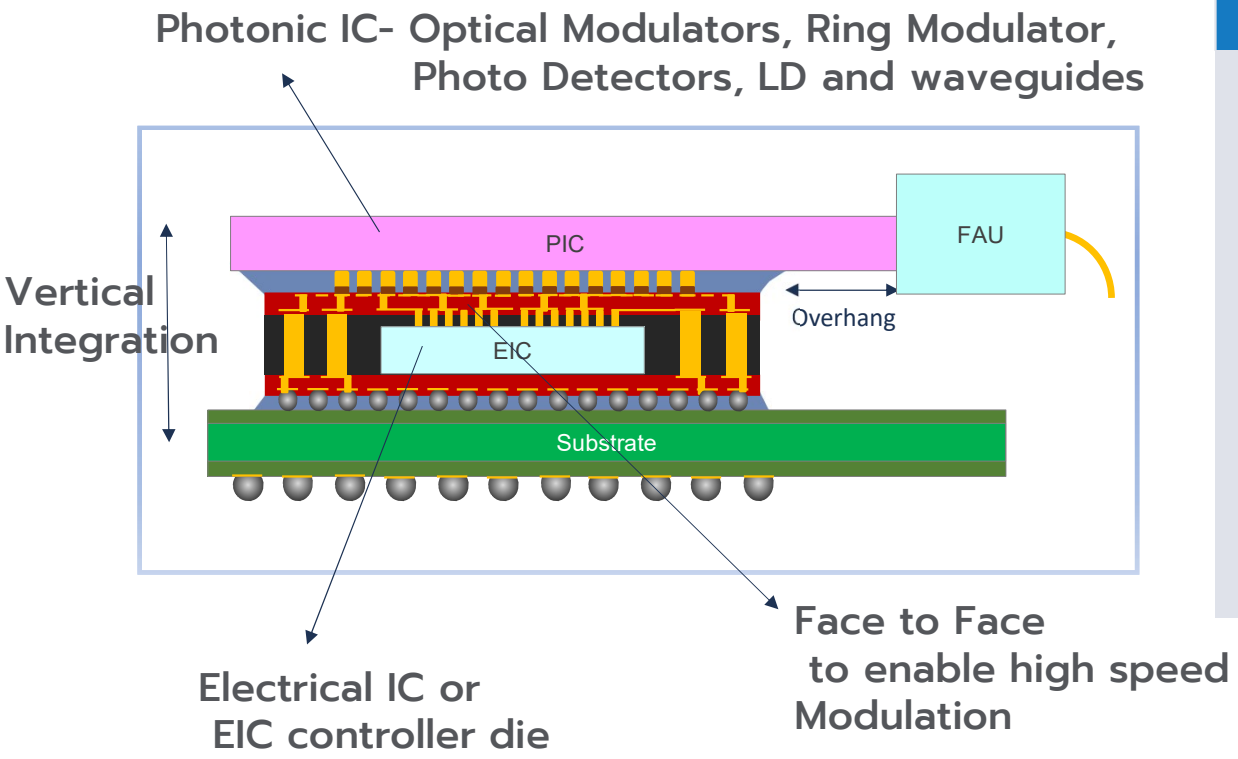
PIC/COW



Eutectic Bonding

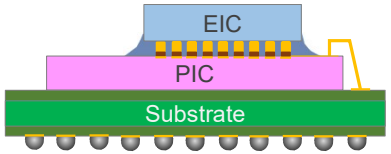
Dicing

Typical Structure Attributes for SiPh FOPoP (Custom By Device)



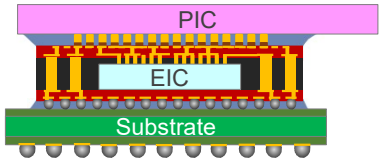
Typical Dimension (Ref: copackagedoptics.com)	
SiPh engine size	~20x20mm
PIC WLCSP overhang	~3mm
FO POP PKG size	16x16mm THK:200um (with T/B CuP bump height)
PIC die size	18x17mm THK:750um
Fiber coupling area	- With or without V-groove - Typical V-groove pitch 200um - Typical V-groove length 2mm - 8-16 channels
PIC Lid	- With overhang or w/o overhang
Bump Pitch	- Typical 130um

SiPh FOPoP - Electrical Simulation (FOPOP vs COW+WB)



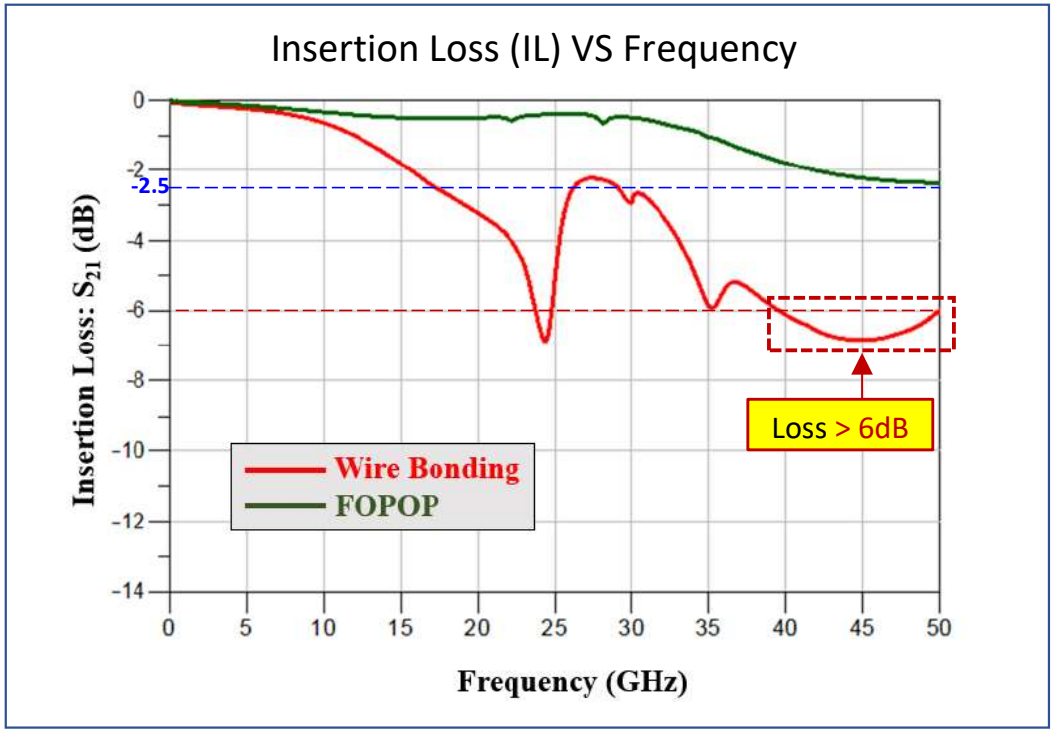
CoW + W/B

Typical pluggable optics
BW <400G

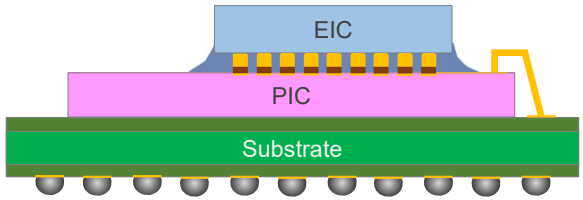
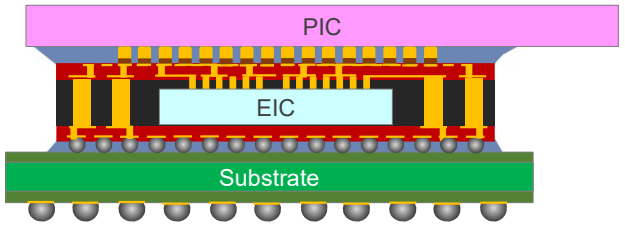
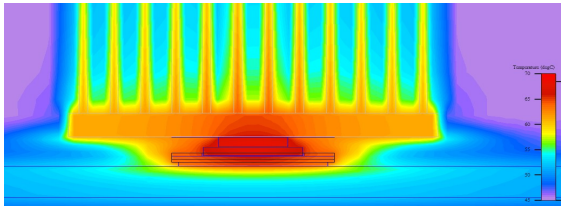
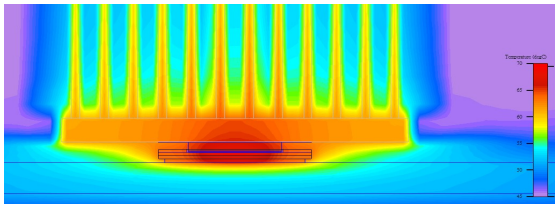


CoW + FOPoP

E-Path ↓ ~3X, BW ↑ ~8X

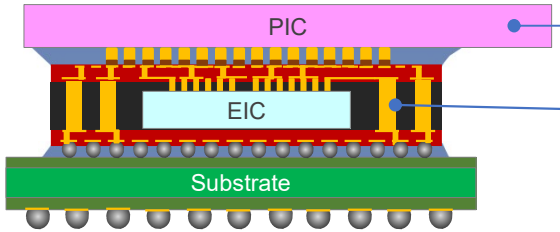


SiPh FOPoP – Thermal Simulation

Package Type		CoW + W/B	CoW + FOPoP
Thickness (a.u.)	EIC	1	0.07
	PIC	1	1
Relative Temperature (°C)	EIC	68.55	69.64
	PIC	67.30	67.43
Structure			
Simulated Data Package with heat sink under 2m/s airflow			

SiPh FOPoP - CTE Mismatches/Warpage Simulation

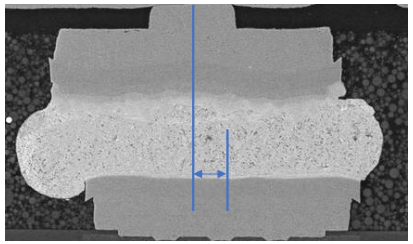
Challenges: CTE Mismatch/Warpage

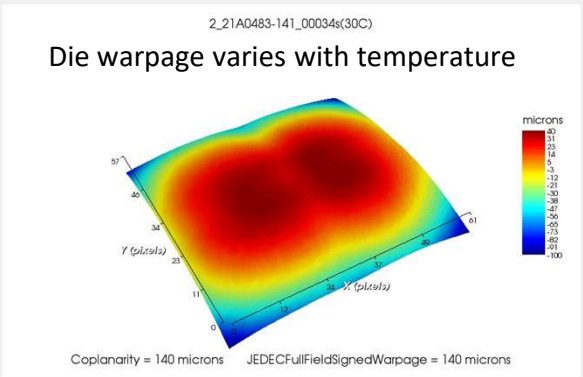


Si CTE: ~3 ppm/degC

Equiv. CTE: 10-15 ppm/degC

ΔCTE: 10 ppm/degC
ΔTemp: >200C
Est. 10mm die would have a 15um bump shift.



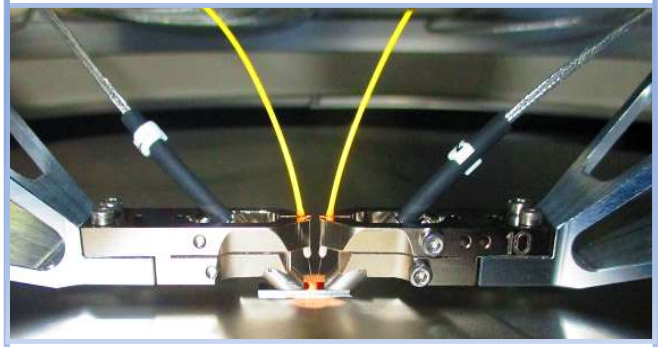


[Mitigation Path]

- Proper fan-out design & consideration
- Material selection
- Proper assembly flow
- Bump joints via localized heating

Wafer-level Optical Testing

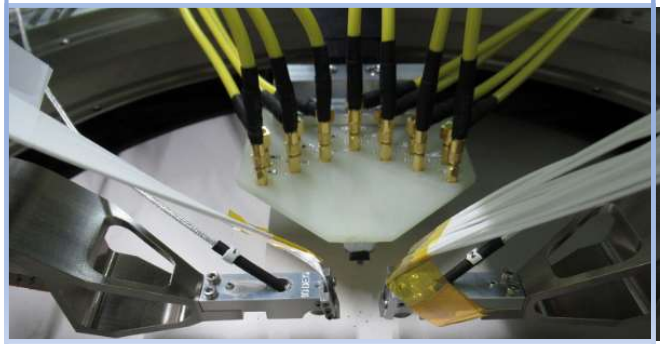
Single Fiber Probing



Probe Type: Single mode fiber

Holder: Single fiber

Fiber Array Probing

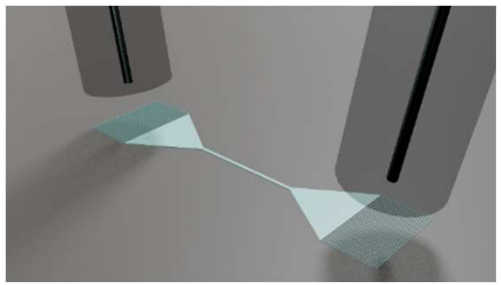


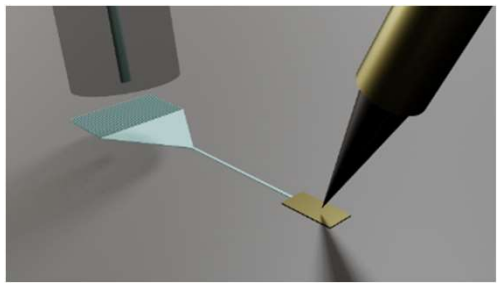
Probe Type: 16ch fiber array

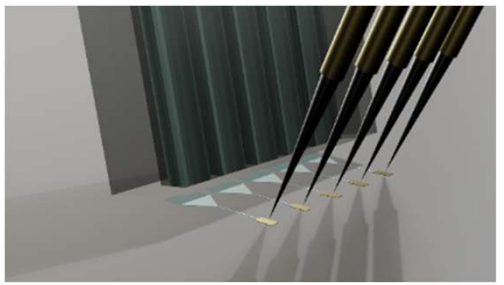
Holder: 8 or 10deg

Wafer-level Optical Testing

Types	Optical Testing	Optoelectronic Testing
DUT	• Waveguide • Splitter	• Diode laser, photodiode, modulator..etc.
Probe	• SMF/FAU for both ports	• SMF/FAU for optical port • Single DC probe/probe card for electrical port.







Conclusion

- The Package-on-Package platform has evolved to enable a next level of performance for both Mobile and Networking through the VIPack FOPOP pillar
- Mobile Application Processors continue to require reduced height while addressing power delivery challenges by leveraging RDL Height benefits and reduced CL.
- Within the Network market space, higher bandwidth density is driving new integration requirements which are being enabled by the VIPack SiPh FOPOP structure
- The more photonic sub-modules that can be integrated, the higher the bandwidth, therefore, size of the Co-Package-Optics module is critical.
- Simulation data shows the SiPh FOPOP shows a reduced insertion loss when compared to the W/B format and showed equivalent thermal performance.
- The VIPack FOPOP and new process enhancements around the photonics die are enabling the next generation of Co-Packaged Optics Network solutions.

Thank you

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