Micro-Transfer Printing for Efficient 3DHI of 100-300mm Wafers and Glass Panels

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Agenda

- **Analog / mixed-signal 3DICs**
  Three-dimensional heterogeneous integration

- **Two levels of efficient 3DHI**
  Three-dimensional heterogeneous integration

- **Conclusions**

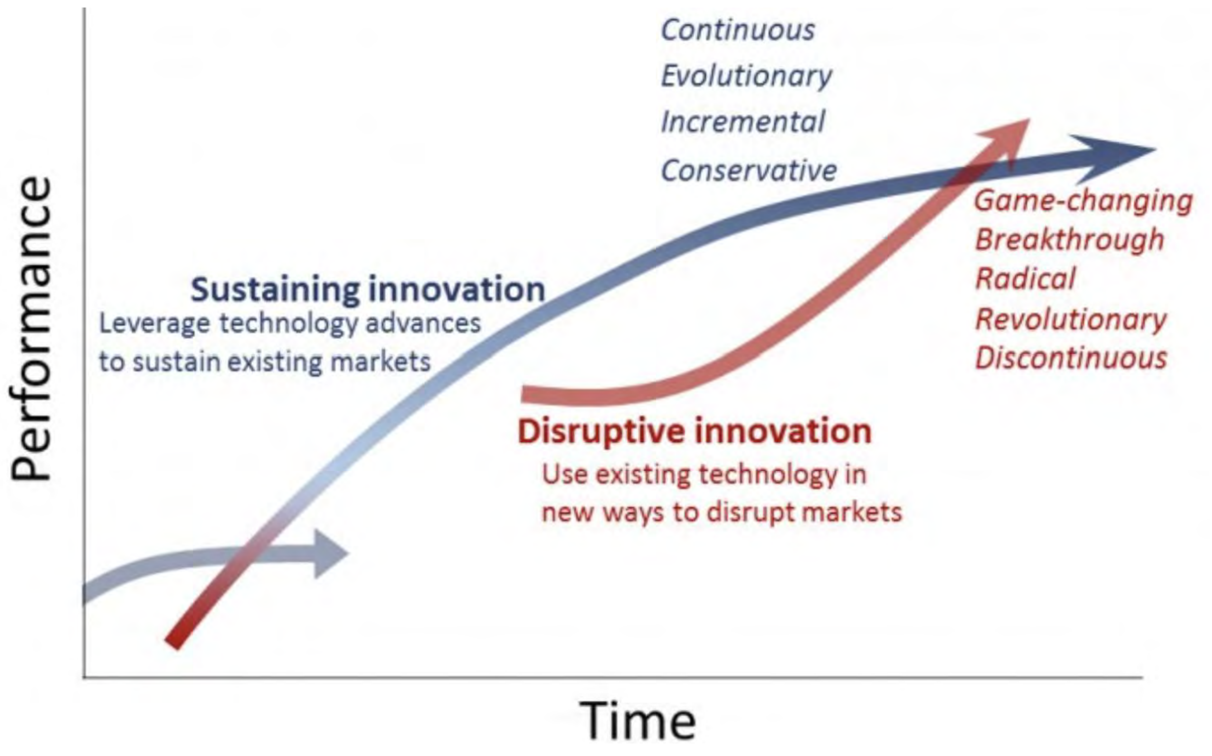
Analog / Mixed Signal 3DICs

- **Many dual use applications**
  High-volume, high-value commercial plus defense
  - 5G/6G wireless communications
  - Satellite communications (Satcom)
  - Power management
    Granular power delivery significantly improves microelectronics energy efficiency
- **Different requirements than "digital"** *(compute & memory)* **applications**
  - Tight integration of large arrays of diverse ultra-thin, transferred chips (x-chips) on glass
    Gallium nitride (GaN), silicon-on-insulator (SOI) and passives
  - Higher power density
  - Lower I/O density
    ~10/10μm L/S (not ultra-fine) interconnects
  - Smaller form factor
    X, Y, Z dimensions
- **Requires disruptive innovation**

Disruptive Innovation

Use existing technology in new ways to disrupt markets

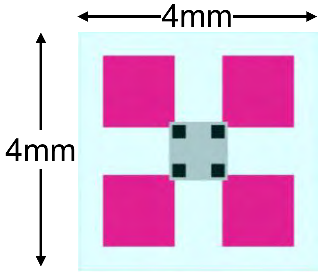
- GaN
- SOI
- Glass
- Micro-transfer printing



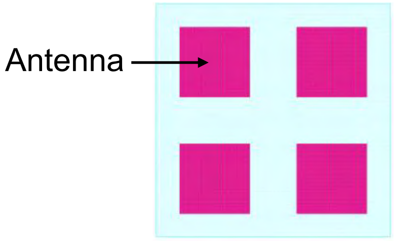
source: *Zaman, Rokon, Incremental Innovation vs Disruptive Innovation, The Waves, July 17, 2020.*

5G/ 6G / Satcom 3DIC

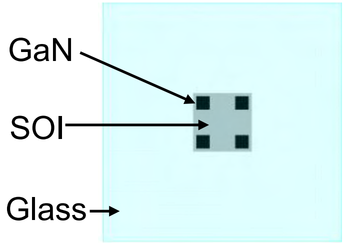
- **Increase efficiency** *(power output, hence, range)*
- **Improve performance** *(linearity)*
- **Reduce cost**
- **Tightly integrate arrays of RF components**
  Readily scalable (4, 16, 32, 64, 128, etc. streams)
  - *GaN power amplifiers*
  - *SOI beam formers*
  - *Patch antennas*
- **Address very large dual-use market**



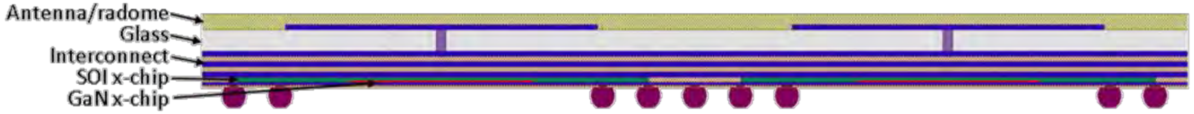
Composite view
Top through glass to bottom



Top view



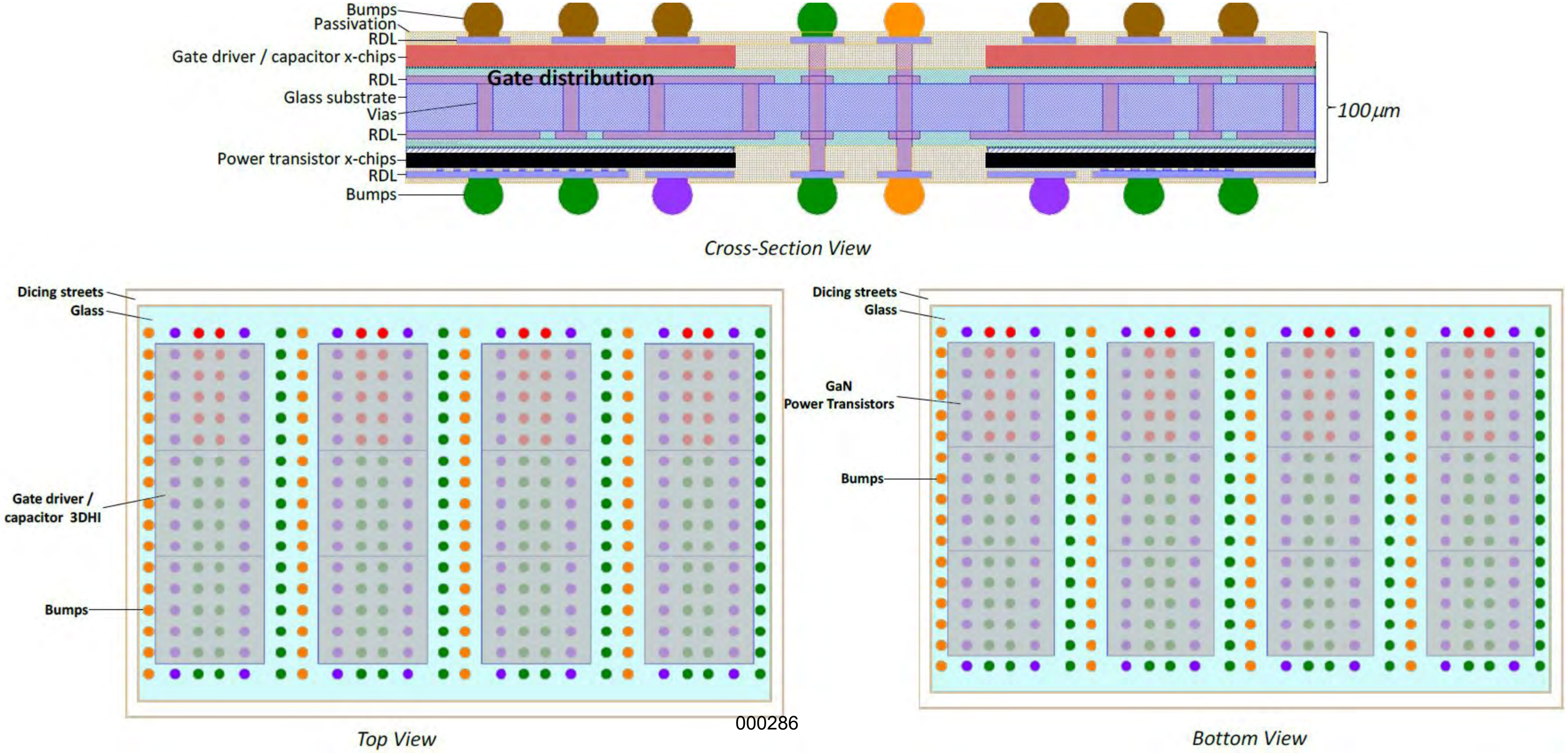
Bottom view



Cross-section view

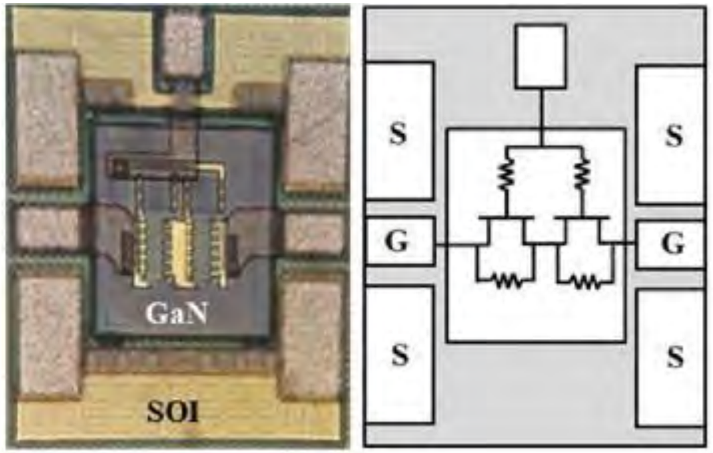
Power 3DIC

- **Leverages GaN-on-SOI 3DIC wireless communications ecosystem**
- **Addresses large markets requiring disruptive improvements in energy efficiency**
  - 48V to 5V bus converters
  - 5V to <1V point-of-load voltage regulators



GaN-on-SOI Example

XFAB



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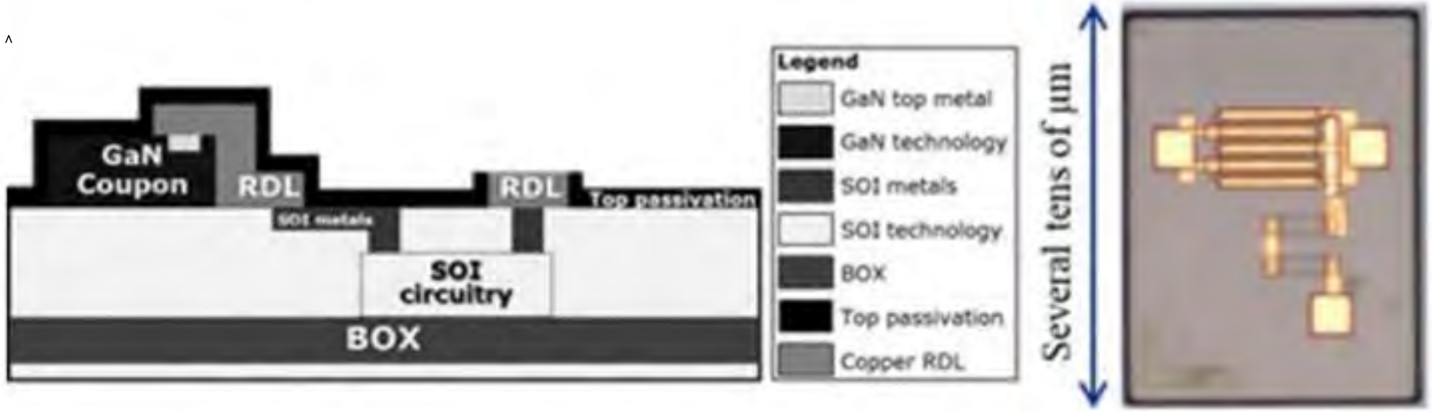
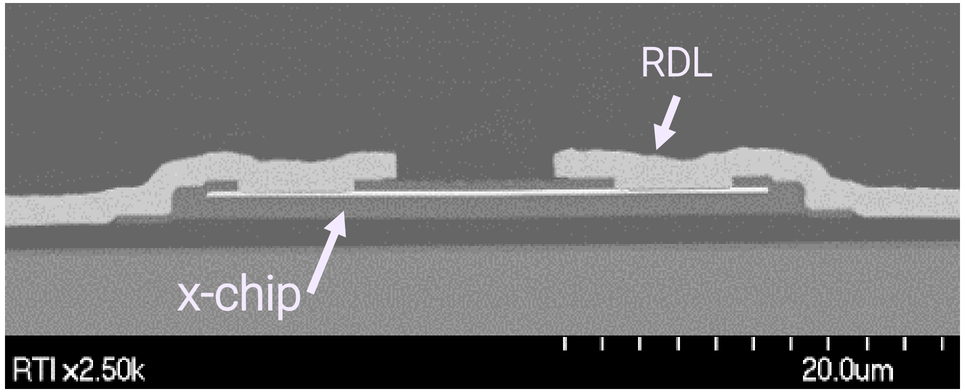


RF Small and large signal characterization of a 3D integrated GaN/RFSOI SPST switch

RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique

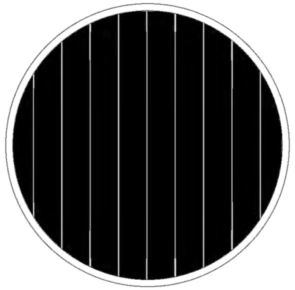


Cross-section view

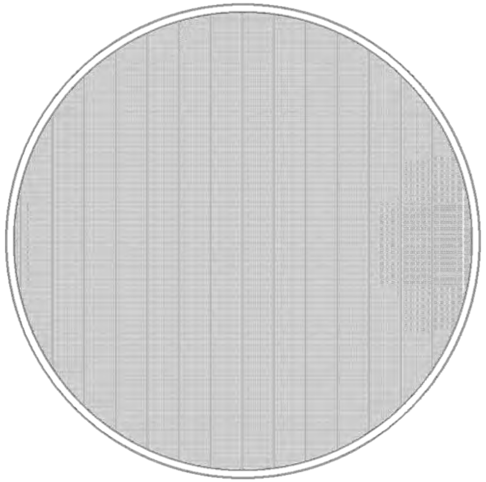
Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing

- **Transferred chips (x-chips) are ultra-thin** <10µm
- **Standard spin-on planarization and thin-film metallization can be used for interconnect**

Two Levels of 3DHI

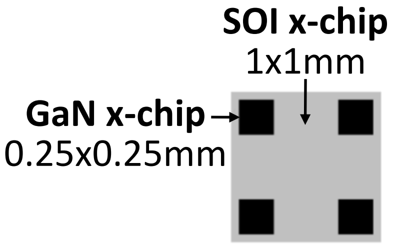


200mm GaN

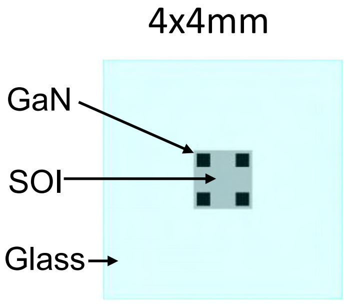


300mm SOI

1) Wafer Fab
<100nm



2) GaN-on-SOI 3DIC



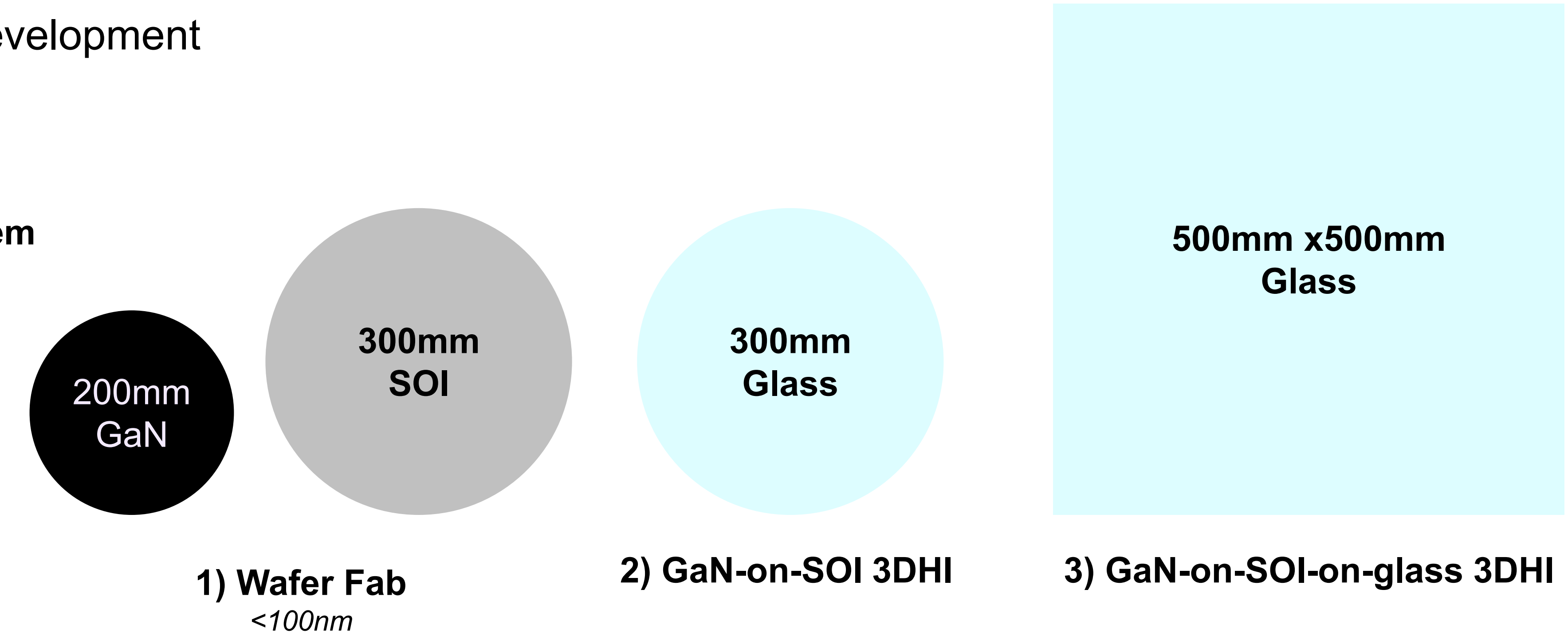
3) GaN-on-SOI-on-glass 3DIC

Analog / Mixed Signal 3DIC Ecosystem

Upgrade existing infrastructure to produce analog / mixed signal 3DICs

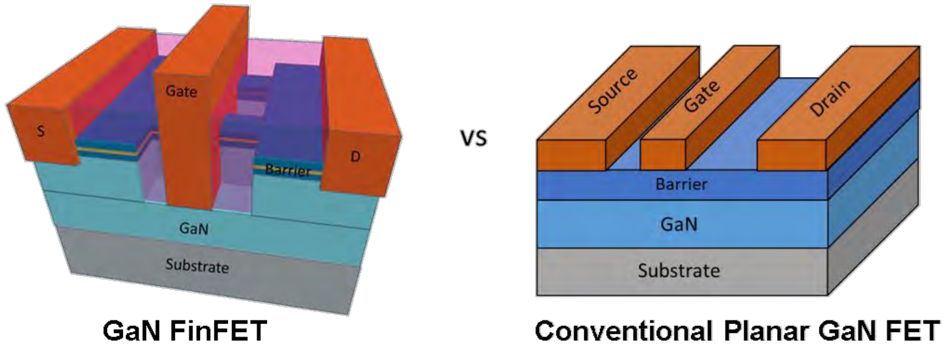
- Achieve economic and national security objectives
- Provide holistic co-design environment
  EDA tools and PDKs
- Stimulate innovation by providing open access rapid prototyping
  Universities, startups, government labs and research institutes
- Facilitate workforce development

Manufacturing ecosystem
- Rapid prototyping
- High volume production



GaN FinFETs

- **3D versus planar structure improves linearity, short channel effects and memory effects**
- **Produced in silicon wafer fabs**
  <100nm nodes provides disruptive f_t, f_{max}, and $R_{DS(on)} \bullet Q_g$
- **Robust**
  High temperature, rad hard

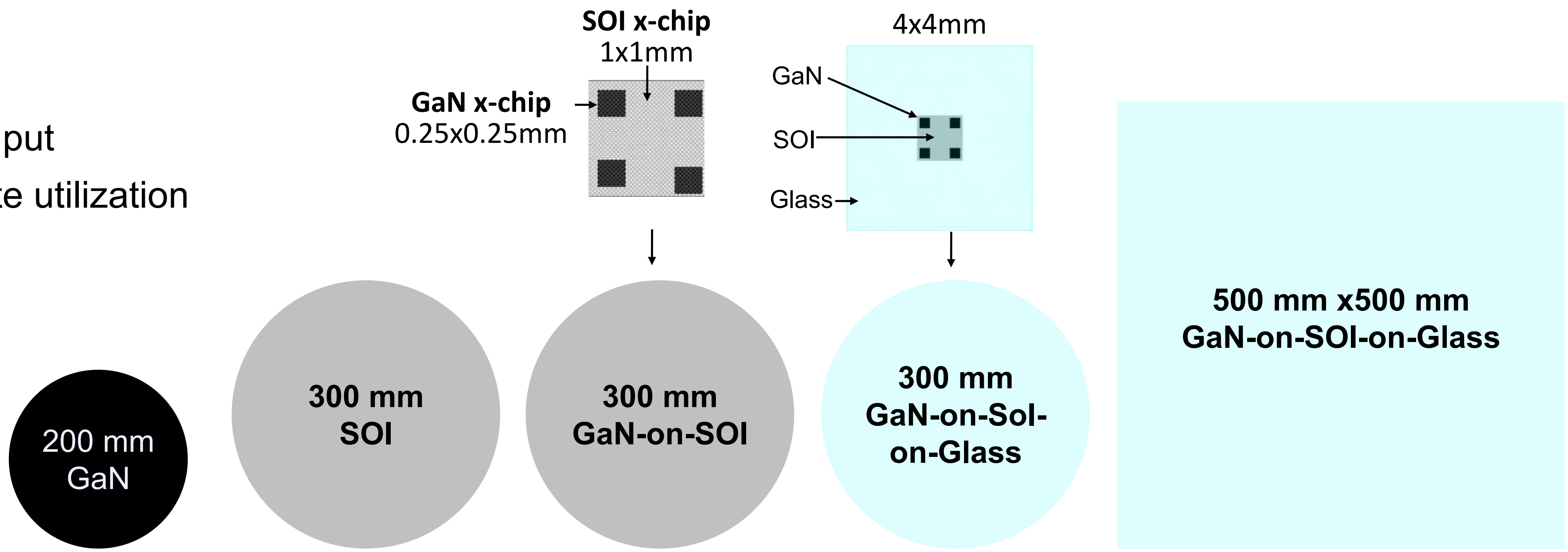


Source: Finwave Semiconductor

Challenges

- Many mismatches
  Substrate sizes, x-chip number, size and pitch
- Interconnects
- Yield
- Cost
  - Capex
  - Opex
  - Throughput
  - Substrate utilization

GaN x-chips located on SOI independently of each other



429,666 x-chips
- *0.25x0.25mm*
- *20μm streets*

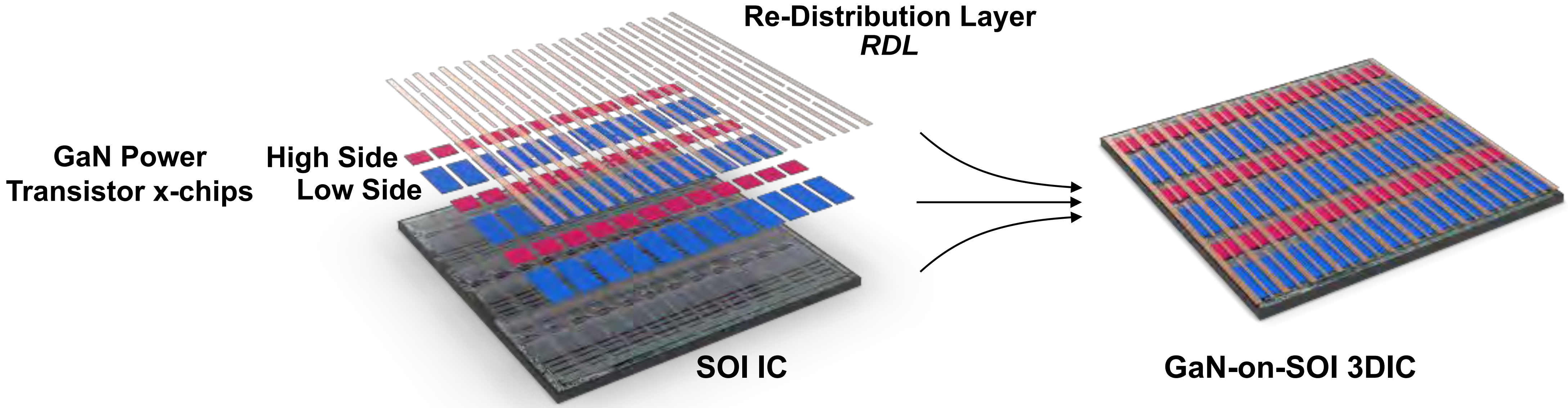
62,174 x-chips
- *1x1mm*
- *20μm streets*

4,019 3DICs
- *4x4mm*
- *80μm streets*

13,920 3DICs
- *4x4mm*
- *80μm streets*

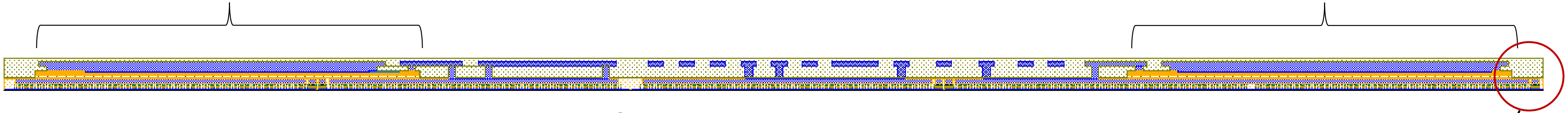
GaN-on-SOI 3DIC

- **Use z-dimension for vertical integration of GaN and SOI**
- **Ultra-thin active-side-up GaN enables RDL interconnection over top**
- **Heterogeneous "known good die" (KGD)**
  - Resembles a monolithic KGD
  - Tested prior to downstream packaging
  - GaN x-chips embedded in SOI's interconnects
  - RDL bridges interconnect gap between wafer fab and packaging

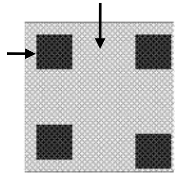


Source: Integrated Power Electronics Components for Integrated Voltage Regulators

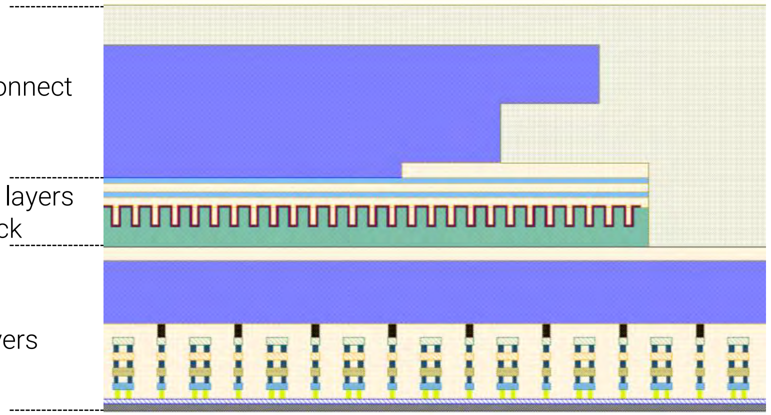
GaN-on-SOI 3DIC



Cross-section view



Top view



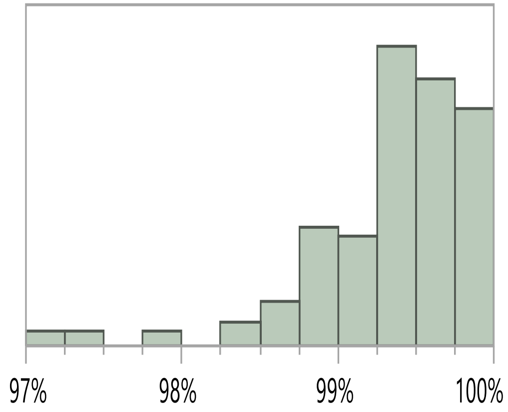
Cross-section view

Employ Micro-Transfer Printing (MTP)

Technology Proven in Concentrator Photovoltaics (CPV)

- **Fabricated surface mountable package with 600x600µm, 3-junction solar cells**
- **Smaller cell provides competitive advantages in CPV**
- **Thousands of target wafers printed in pilot production**
- **Highly reliable package**
  >25 billion cell hours in field, passed rigorous reliability testing

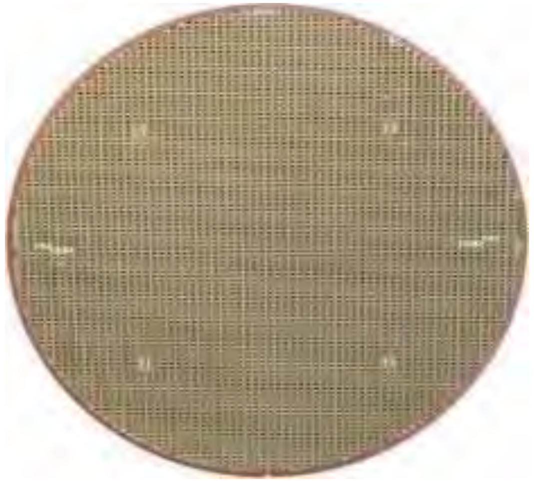
24.5 kW CPV system



Summary Statistics	
Mean	0.993579
Std Dev	0.004993
Std Err Mean	0.0004873
Upper 95% Mean	0.9945453
Lower 95% Mean	0.9926128
N	105

Print Yield Distribution of 105 interposer wafers

- Sample of 105 interposer wafers, 4,866 die per wafer
- Solar cells printed from 150mm GaAs wafer to 150mm ceramic wafer
- Printed with a 24x24 post array stamp, 13 print cycles per target wafer
- Average print yield of 99.3%



150mm ceramic wafer with 4,866 micro-transfer printed solar cells

MTP: Massively Parallel Pick-and-Place

GaN-on-SOI 3DIC heterogeneous integration providing high:

- Flexibility to efficiently handle mismatches
  Wafer sizes, number of x-chips, x-chip sizes, x-chip pitches
- Throughput
- Substrate utilization
  GaN, SOI and glass
- Placement accuracy
  ±1.5µm @ 3σ
- Yield

ASM AMICRA's Nova+ MTP Manufacturing System

X-Display MTP Manufacturing System

Manufacturing Flow

1) GaN wafer fab

With minimal number of metal interconnects

2) SOI wafer fab

With minimal number of metal interconnects

3) Micro-transfer print GaN x-chips on SOI wafer → GaN-on-SOI 3DIC

4) Glass wafer fab

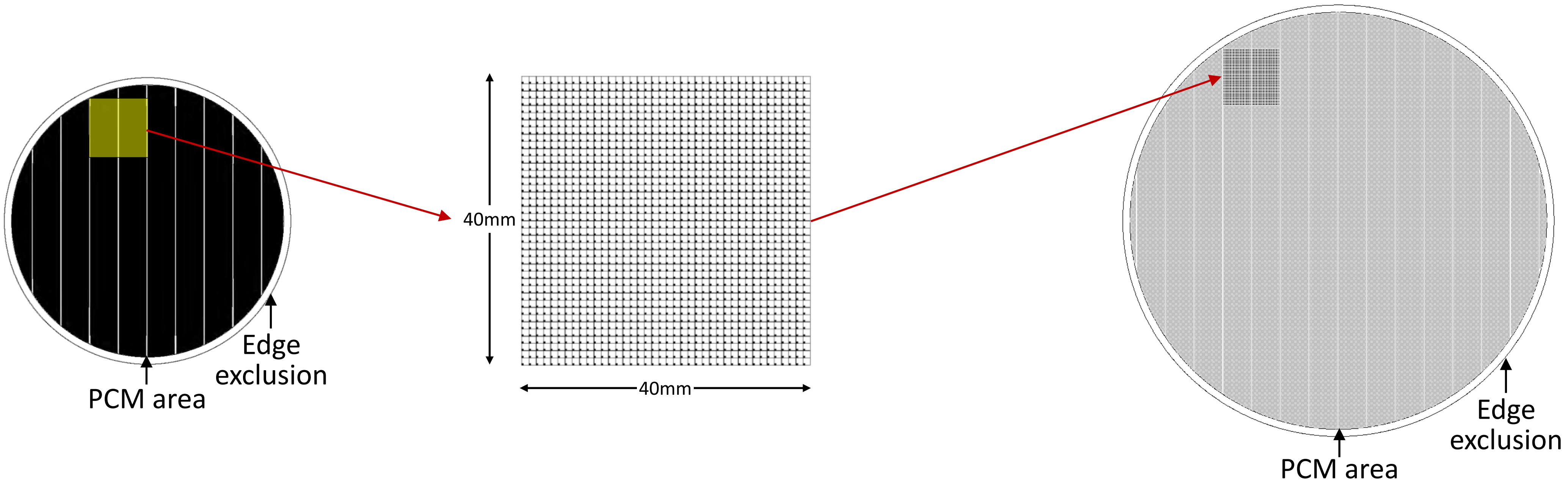
With antenna arrays, passive components, through glass vias, cavities, thick RDL interconnects

5) Micro-transfer print GaN-on-SOI 3DICs on glass → GaN-on-SOI-on-glass 3DIC

6) Form additional RDL interconnects completing GaN-on-SOI-on-glass 3DIC

Mass Transfer GaN X-Chips

From 200mm Wafer to 300mm Wafer



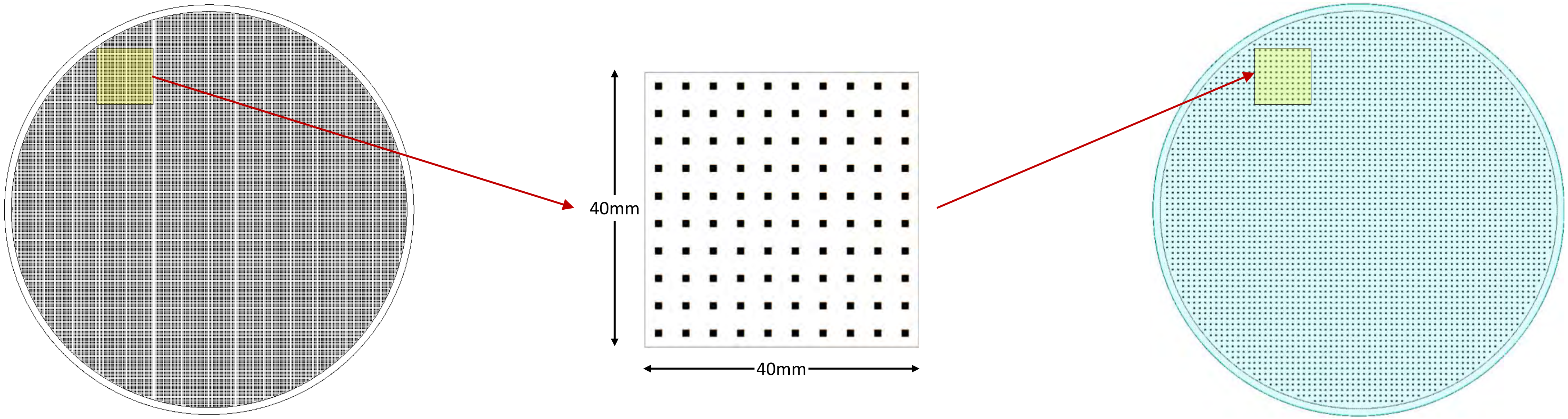
200mm GaN Wafer
- 429,666 x-chips (*0.25x0.25mm each)*
- 95% wafer utilization

MTP Stamp Close-Up
- Transfers 1,520 x-chips
  1,600 (40x40) – 80 for PCM
- 4 transfers per site

300mm SOI Wafer
- 62,174 x-chips (*1x1mm each)*
- 98% wafer utilization
- 0.9 substrates/hour (*4 transfers/site)*
- 225,000 GaN x-chips/hour

Mass Transfer GaN-on-SOI 3DICs

From 300mm Wafer to 300mm Glass Wafer



300mm GaN-on-SOI Wafer

- 62,174 3DICs (*1x1mm each)*
- 99.5% substrate utilization

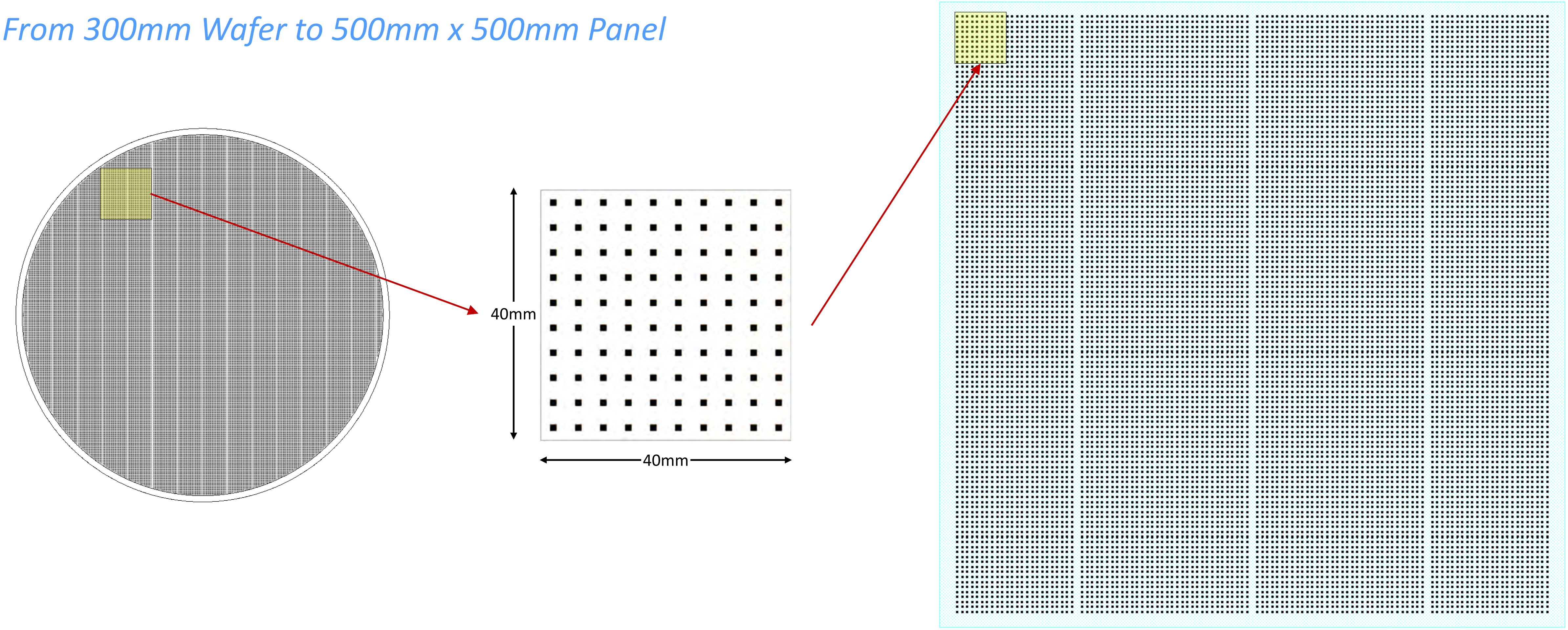
MTP Stamp Close-Up

300mm Glass Wafer

- 4,019 3DICs (*4x4mm each)*
- 100% substrate utilization
- 4 substrates/hour
- 16,000 GaN-on-SOI 3DICs/hour

Mass Transfer GaN-on-SOI 3DICs

From 300mm Wafer to 500mm x 500mm Panel



300mm GaN-on-SOI Wafer

- 62,174 3DICs (*1x1mm each)*
- 96 % substrate utilization

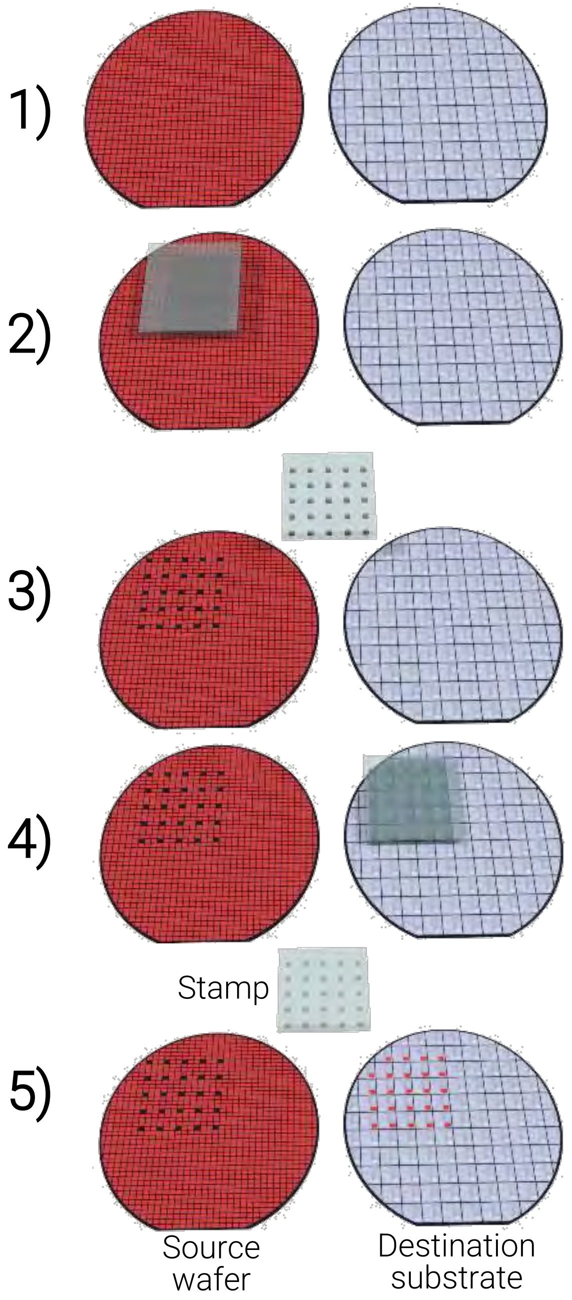
MTP Stamp Close-Up

500 mm x 500mm Glass Panel

- 13,920 3DICs (*4x4mm each)*
- 100% substrate utilization
- 1.3 substrates/hour
- 18,096 GaN-on-SOI 3DICs/hour

MTP System Transfers X-Chips Active-Side Up from Source to Destination

- Stamp's posts adhere to x-chips via van der Waals force
- Stamp's visco-elastic behavior
  - Fast separation speed in pick-up regime
  - Slow separation speed in printing regime
- Stamp pick-up breaks tethers and removes x-chips
- Massively parallel selective pick-and-place of many x-chips
- Readily transfers ultra-thin and fragile x-chips
- Stamp contacts destination substrate and x-chips stick to new surface via:
  - van der Waals force
  - Ultra-thin adhesive
- Placement with controllable pitch and pattern
  Geometric magnification (fan-out)

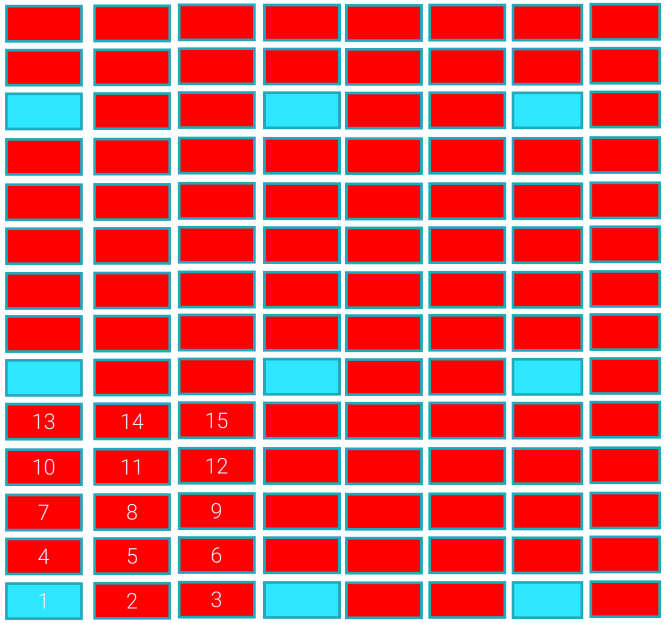


Transfer printing by kinetic control of adhesion to an elastomeric stamp

Stamp’s Post Configuration Matched to X-Chip Spacing on Destination Substrate

For “Geometric Magnification” (Fan-Out)

close-up views

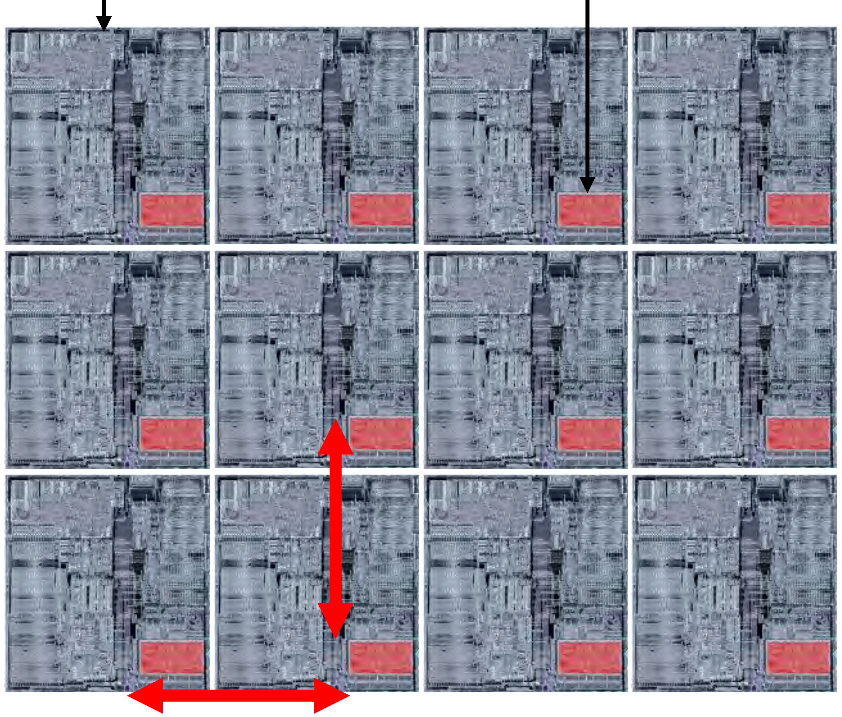


Source wafer

Densely-packed x-chips with pitch matching integral x/y multiples of placement on destination substrate`

MTP stamp

Post configuration matched to x-chip spacing on destination substrate



Destination substrate

Distance between x-chips in x/y determines stamp’s post configuration

MTP vs. W2W vs. D2W Comparison

Cost Factor	MTP	D2W	W2W
Throughput	High	Very low *Ability to handle small, thin, x-chips?*	High
GaN Wafer Utilization	High	High	Very low
SOI Wafer Utilization	High	High	Very low
Yield	High	High	Lower *More process steps*

Conclusions

For wireless communications and power management applications
Two large dual use markets requiring disruptive 3DHI

- **GaN FinFETs meet challenging efficiency, performance and cost targets**
- **Micro-transfer printing enables two levels of efficient 3DHI**
- **GaN 3DICs provide U.S. and allied nations with many opportunities**
  - **Sustainable technological superiority**
  - **High-volume production**
    Defense and commercial dual-use
  - **Workforce development**
    Plus many attractive career oppportunities
  - **Catalyze innovation**
    Universities, government labs, research institutes and start-ups

Appendix

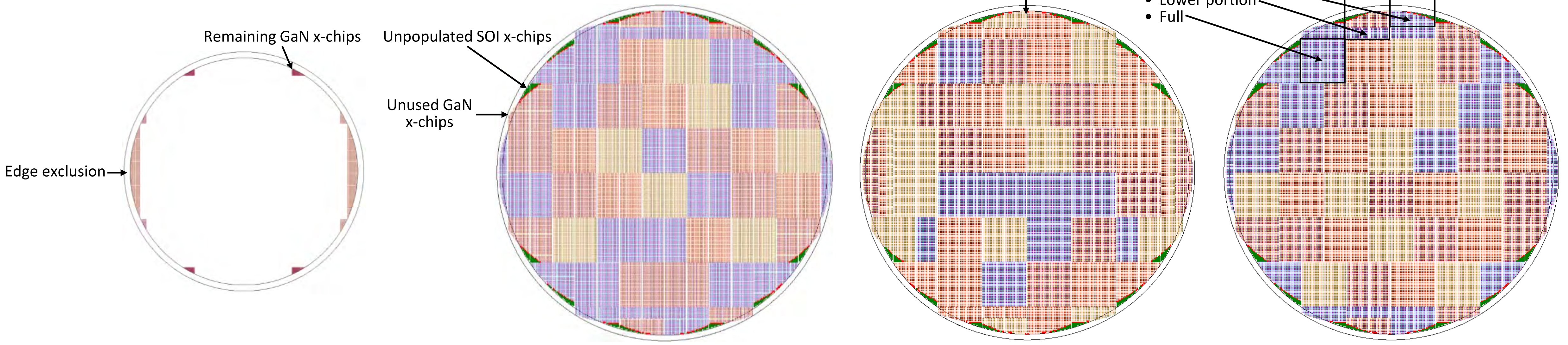
MTP Transfer of GaN X-Chips from 200mm GaN Wafers to 300mm SOI Wafers

High wafer utilization achieved by:

- Populating 11 SOI wafers with 6 GaN wafers
- 40x40mm MTP stamp going over:
    - Edge of wafer
    - Previously transferred sites

      So some MTP transfers are effectively <40x40mm
- Using different sequence of MTP transfers for each wafer

  Sequence repeats after 11 SOI wafers



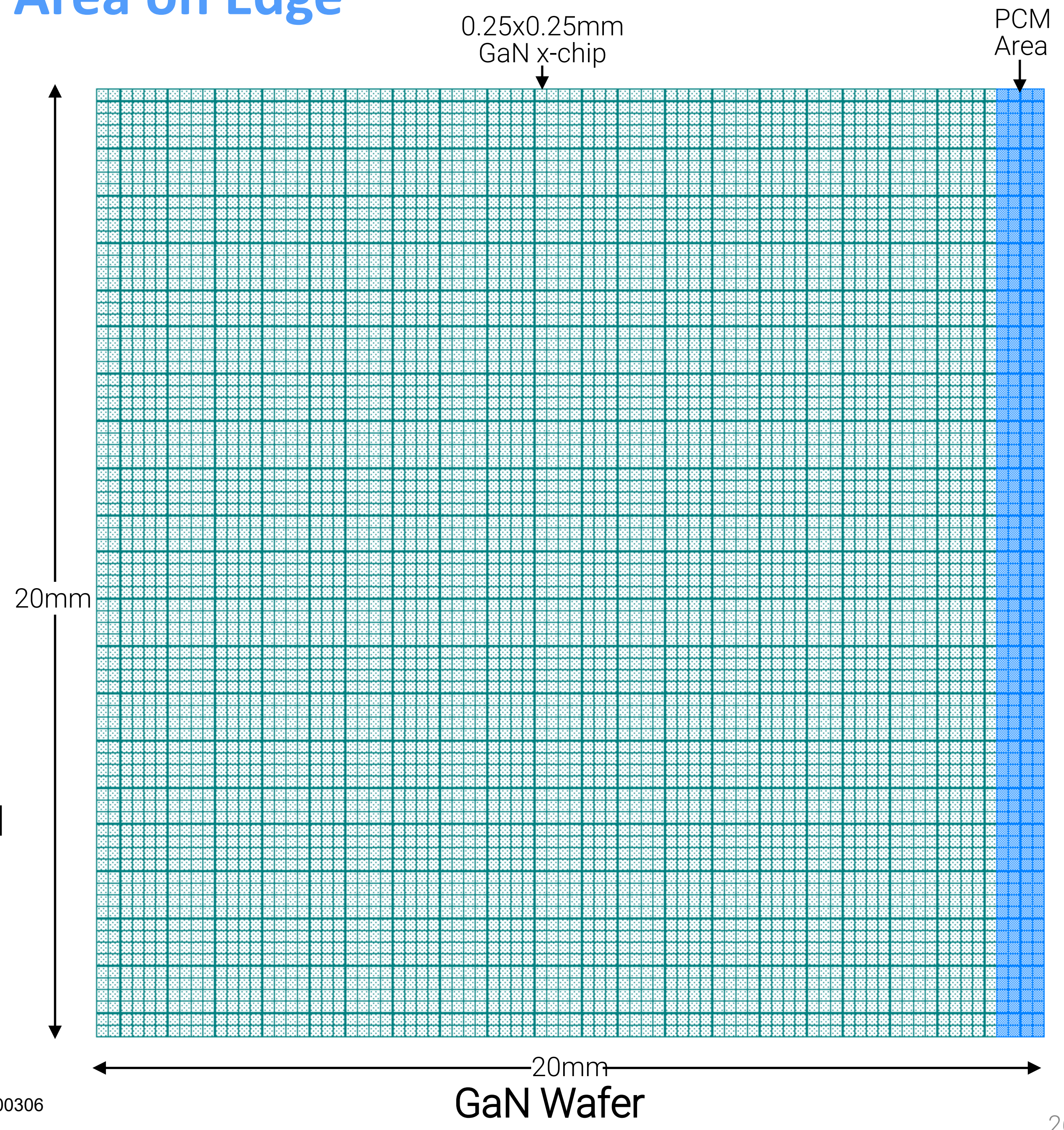
Depleted GaN Wafer | Populated SOI Wafer #1 | Populated SOI Wafer #2 | Populated SOI Wafer #3

MTP transfer sequence is different for each of 11 SOI wafers

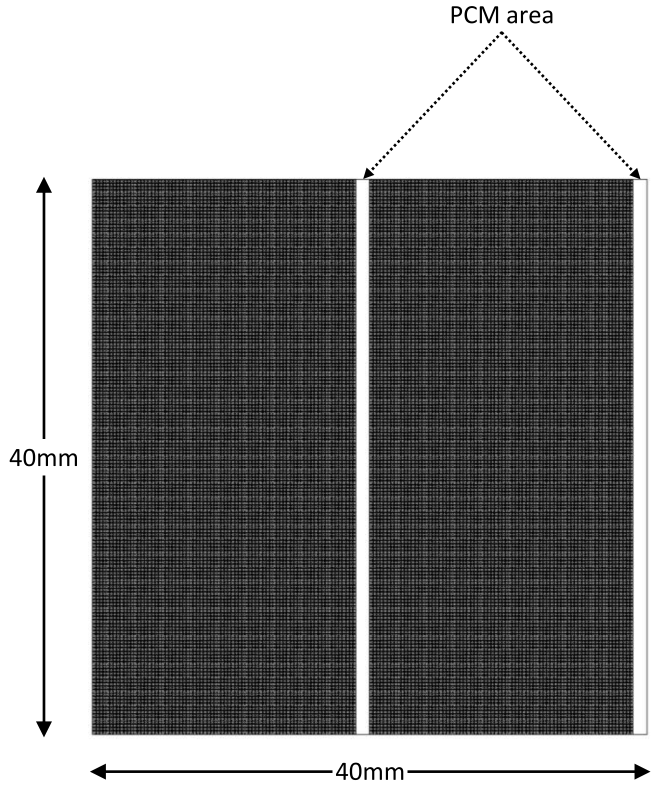
Assume 20mm Reticle With 1mm PCM Area on Edge

For Source and Destination Wafers

- 1mm PCM width equal to width of:
  - 4 GaN x-chips *(0.25x0.25mm each)*
  - 1 SOI x-chip *(1x1mm each)*
- 6,080 (76x80) GaN x-chips
  320 (4x80) GaN x-chips lost due to PCM
- 380 (19x20) SOI x-chips
  20 (1x20) SOI x-chips lost due to PCM
- Stamp has posts not populated with x-chips during MTP transfers
- Different (smaller) PCM areas can be accommodated

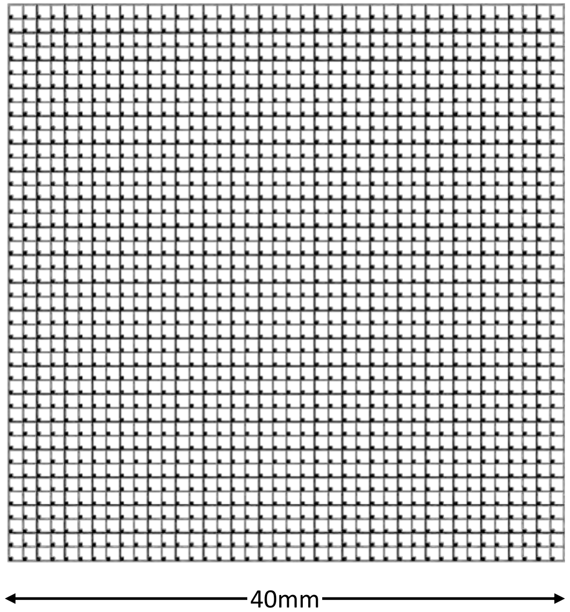


Before Transfer #1



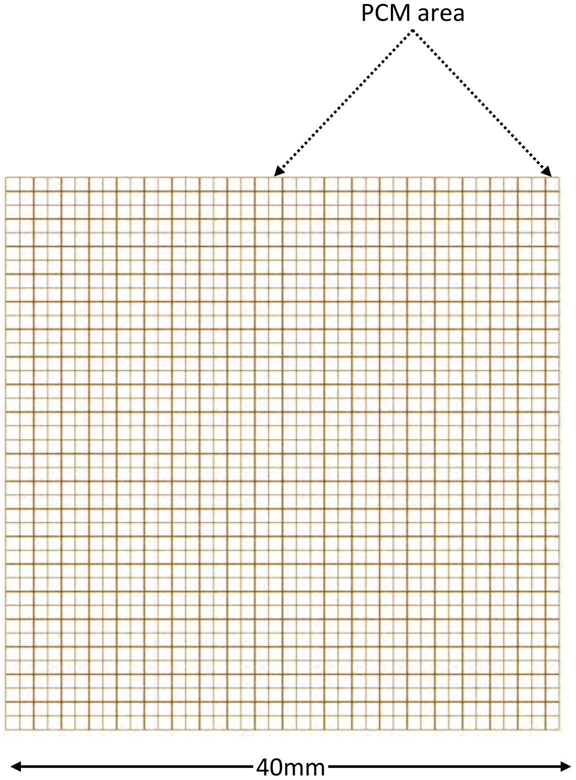
GaN Wafer

0.25x0.25mm GaN x-chips



MTP Stamp

1,600 posts

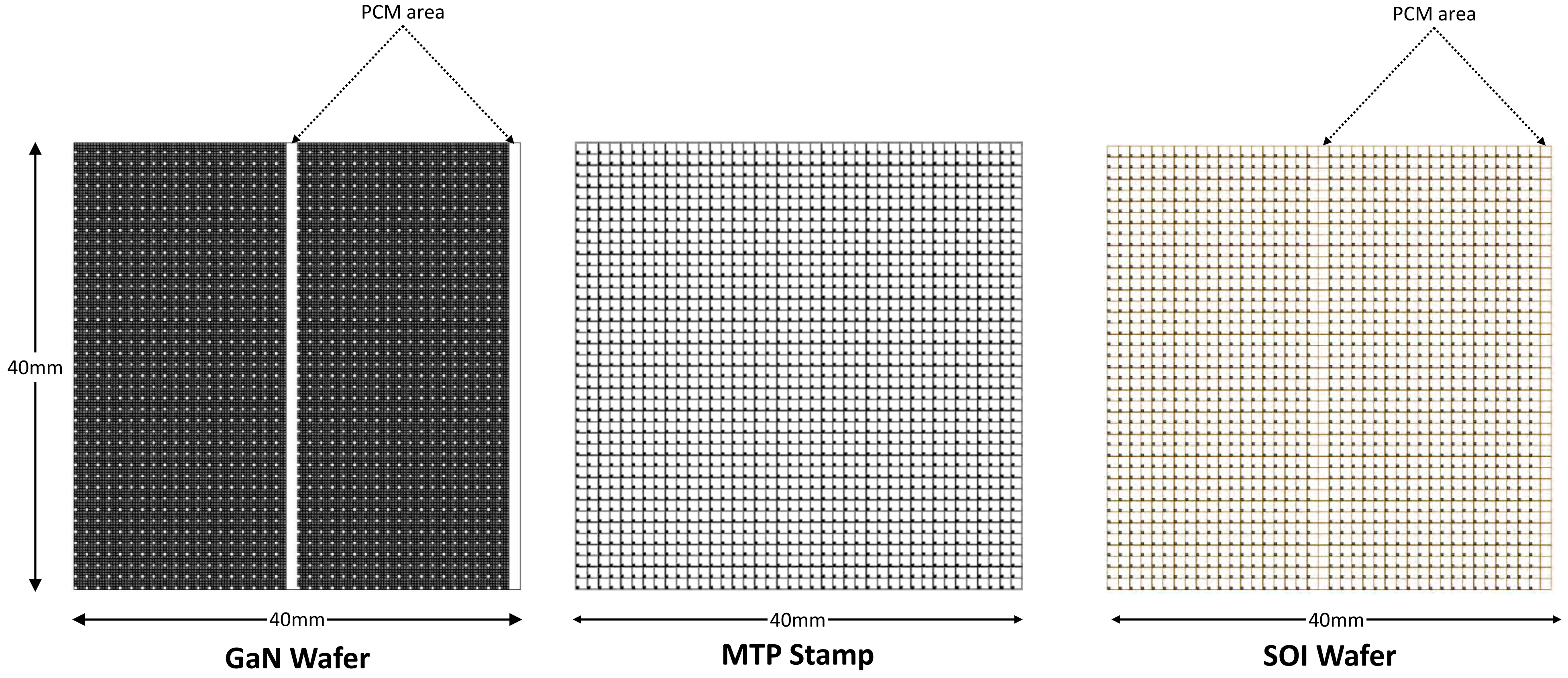


SOI Wafer

1x1mm SOI x-chips

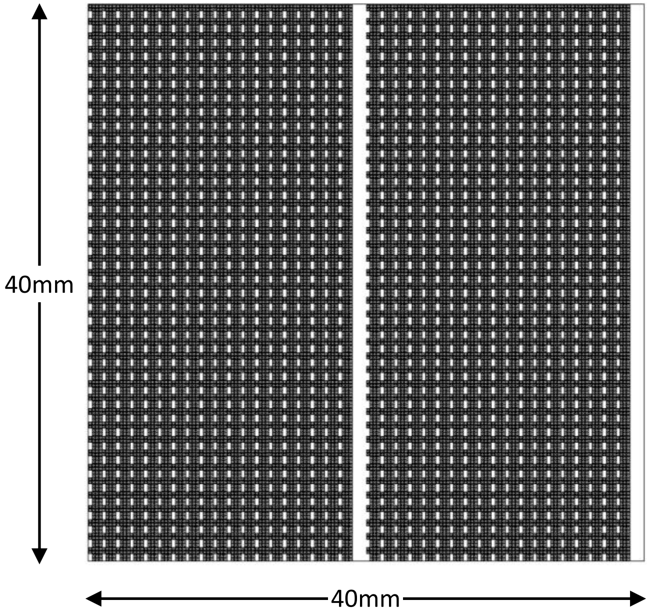
After Transfer #1

Transfer GaN x-chip
in **bottom left**
of each SOI x-chip

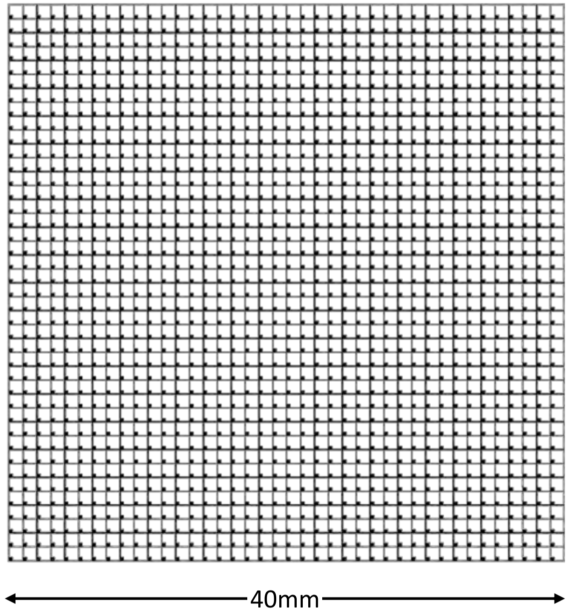


After Transfer #2

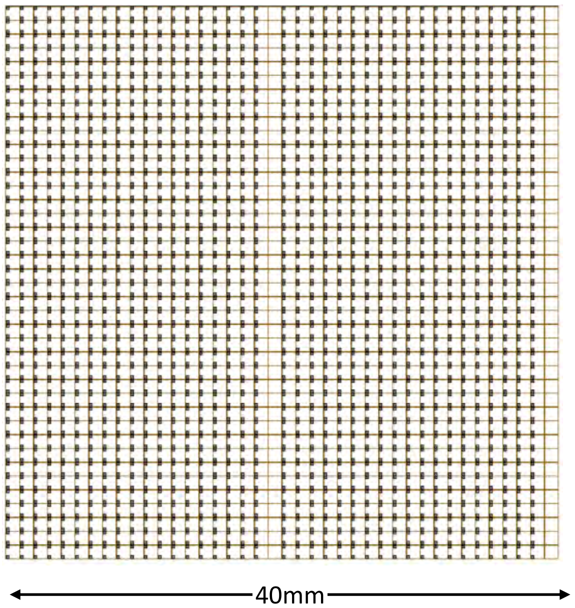
Transfer GaN x-chip
in **upper left**
of each SOI x-chip



GaN Wafer



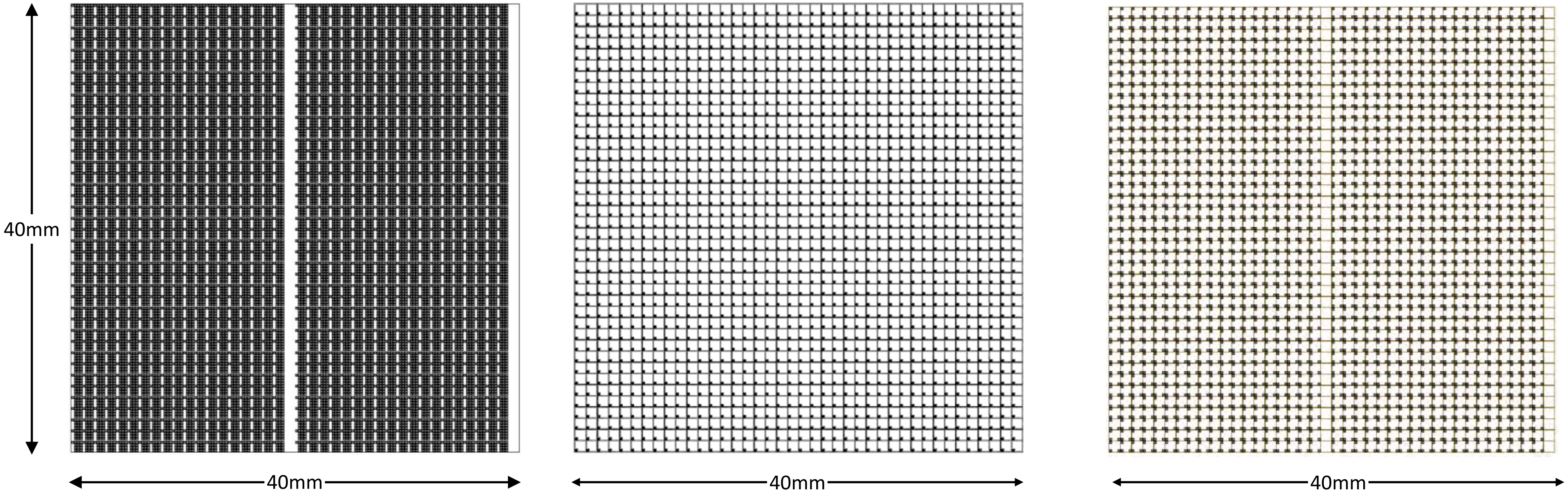
MTP Stamp



SOI Wafer

After Transfer #3

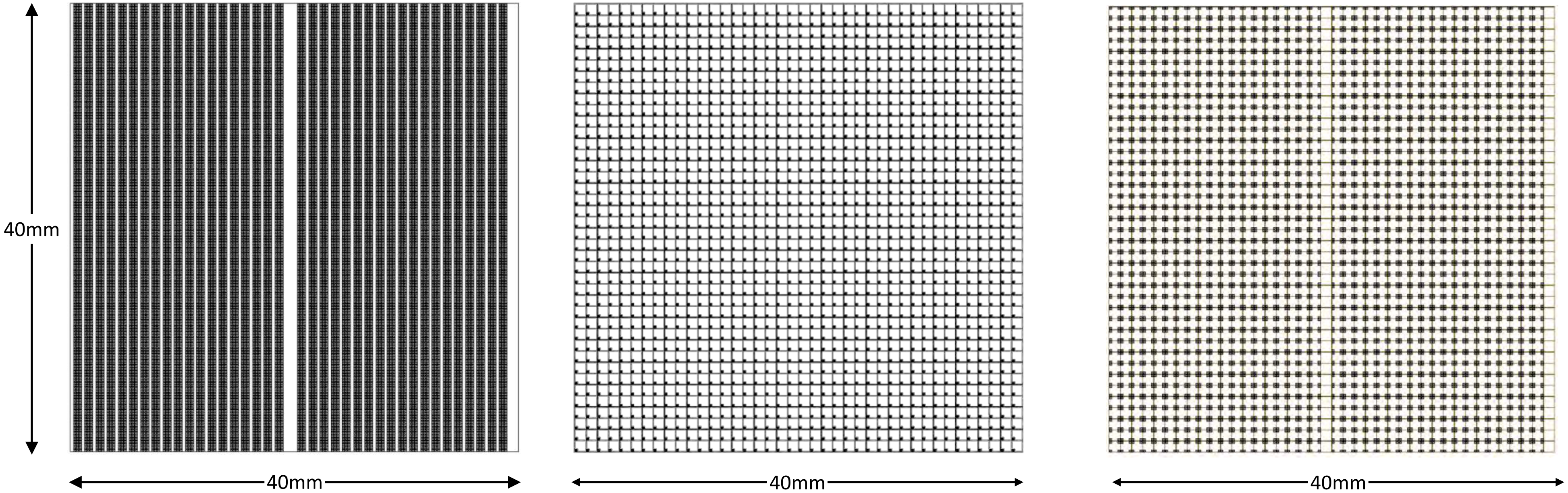
Transfer GaN x-chip
in **lower right**
of each SOI x-chip



GaN Wafer **MTP Stamp** **SOI Wafer**

After Transfer #4

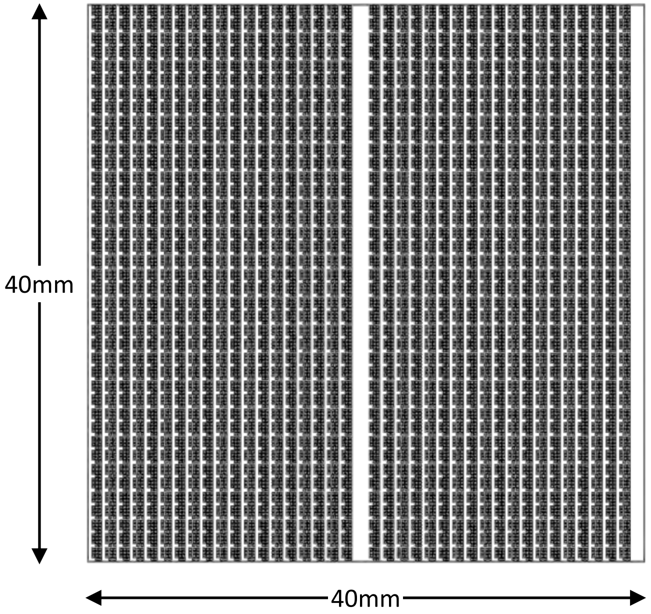
Transfer GaN x-chip
in **upper right**
of each SOI x-chip



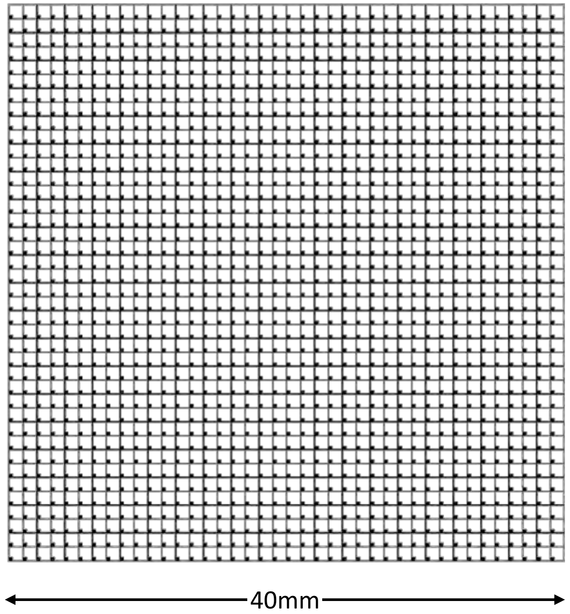
GaN Wafer **MTP Stamp** **SOI Wafer**

After Transfer #5

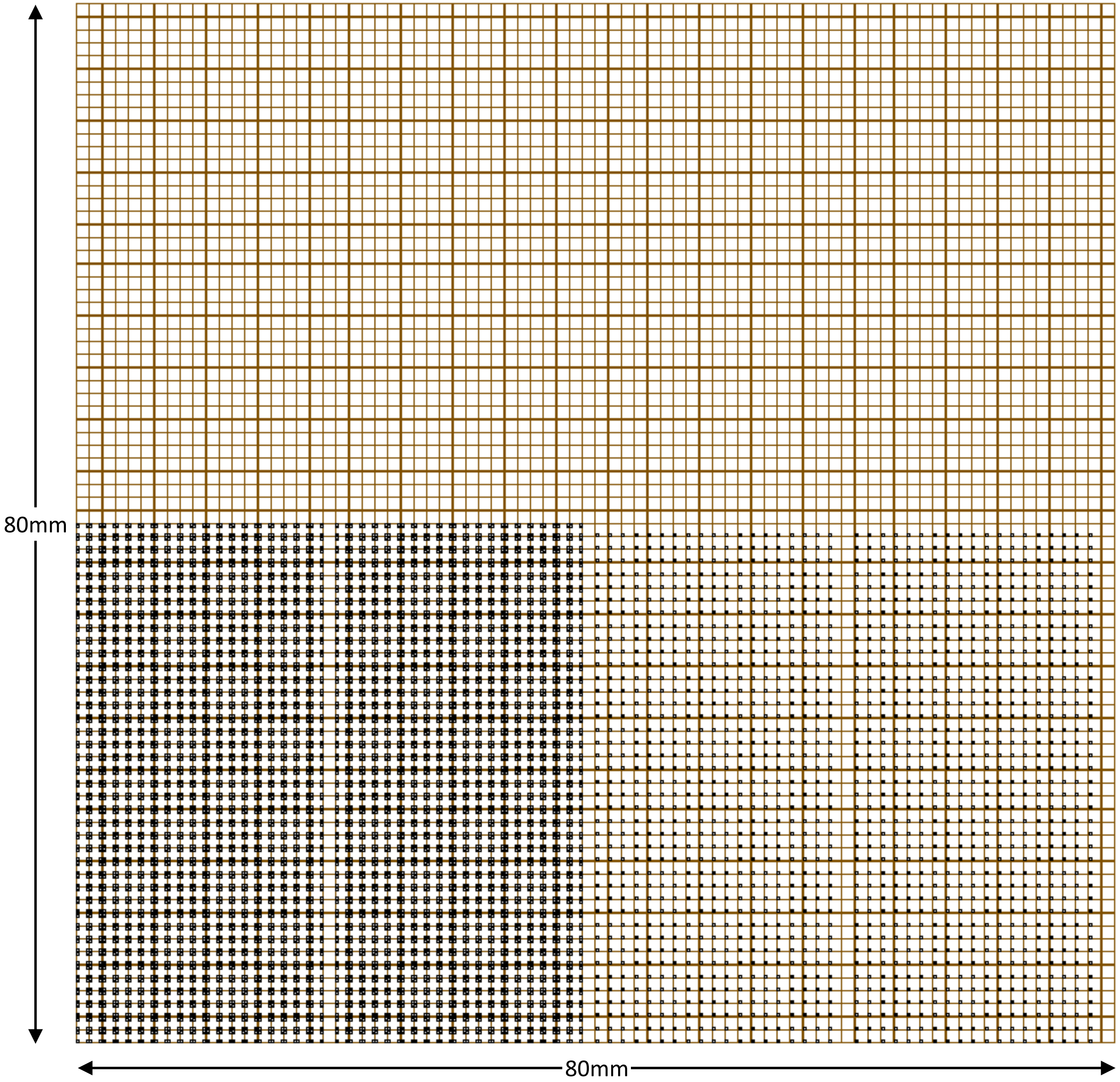
Transfer GaN x-chips to next site on SOI wafer



GaN Wafer

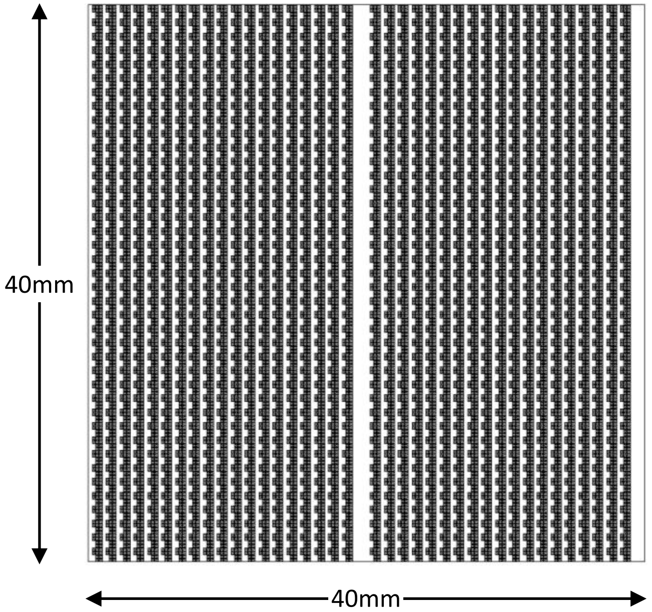


MTP Stamp

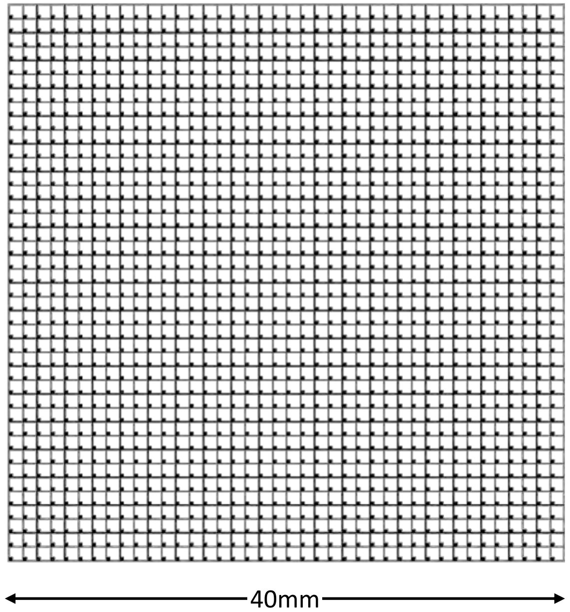


SOI Wafer

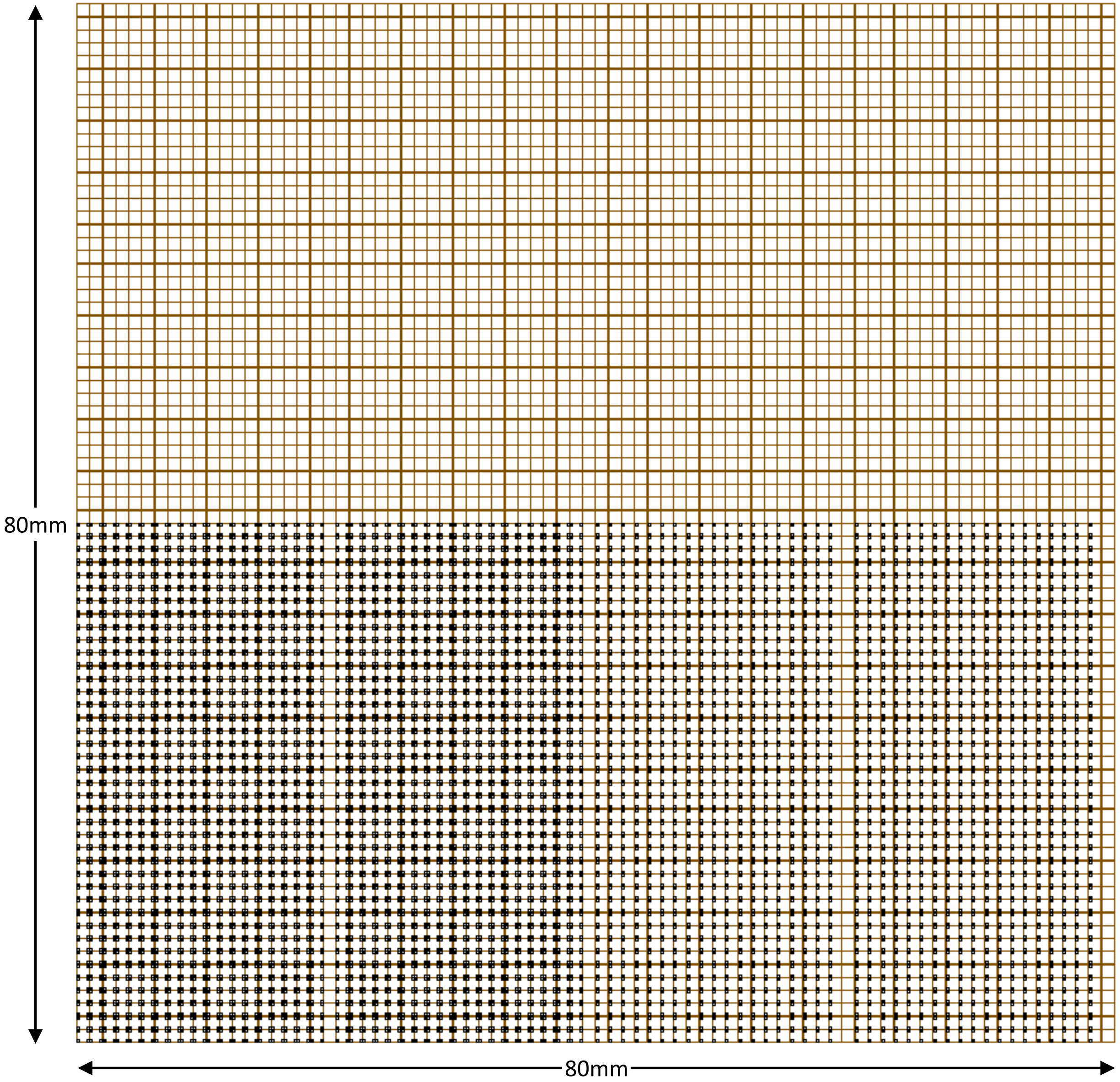
After Transfer #6



GaN Wafer

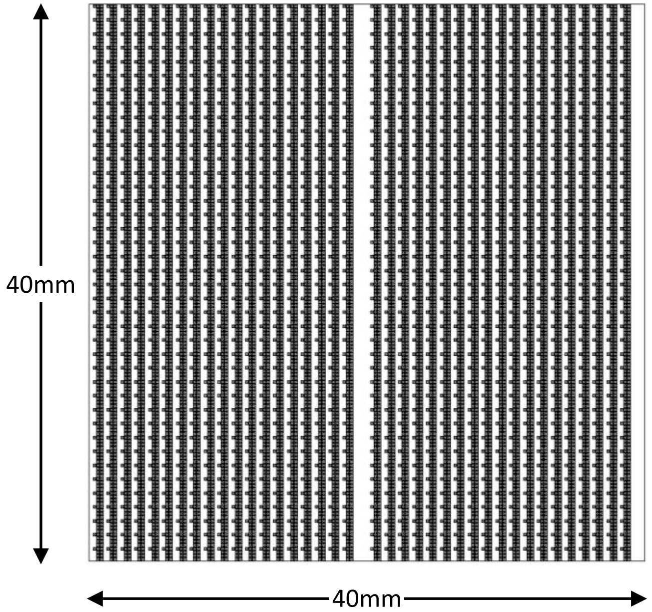


MTP Stamp

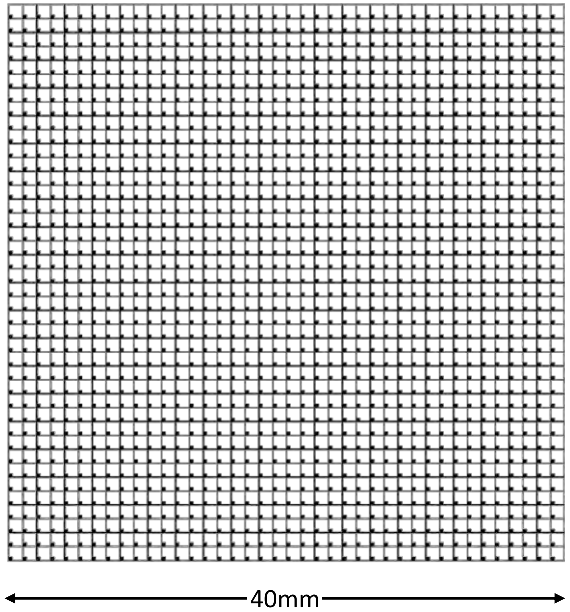


SOI Wafer

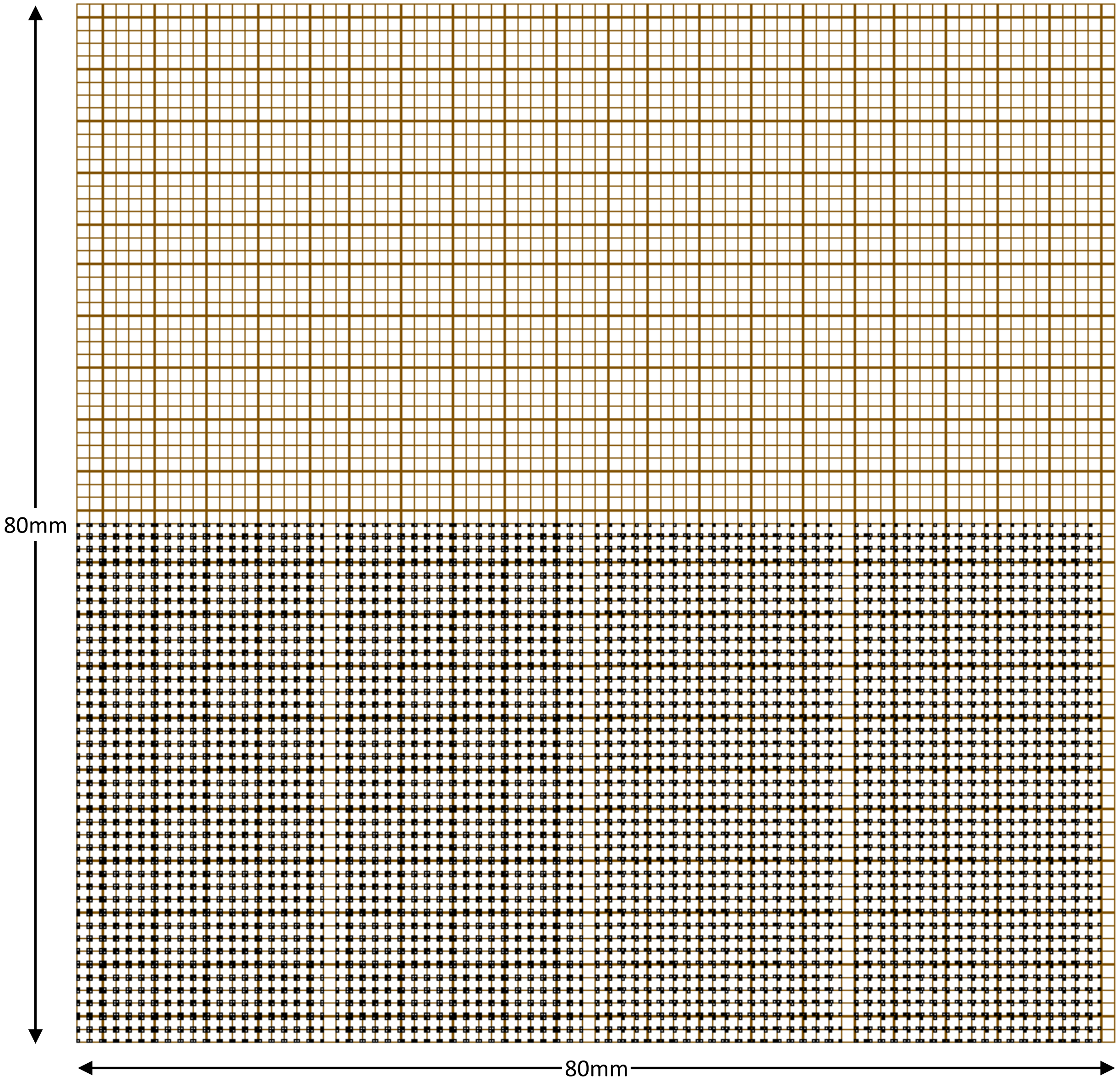
After Transfer #7



GaN Wafer

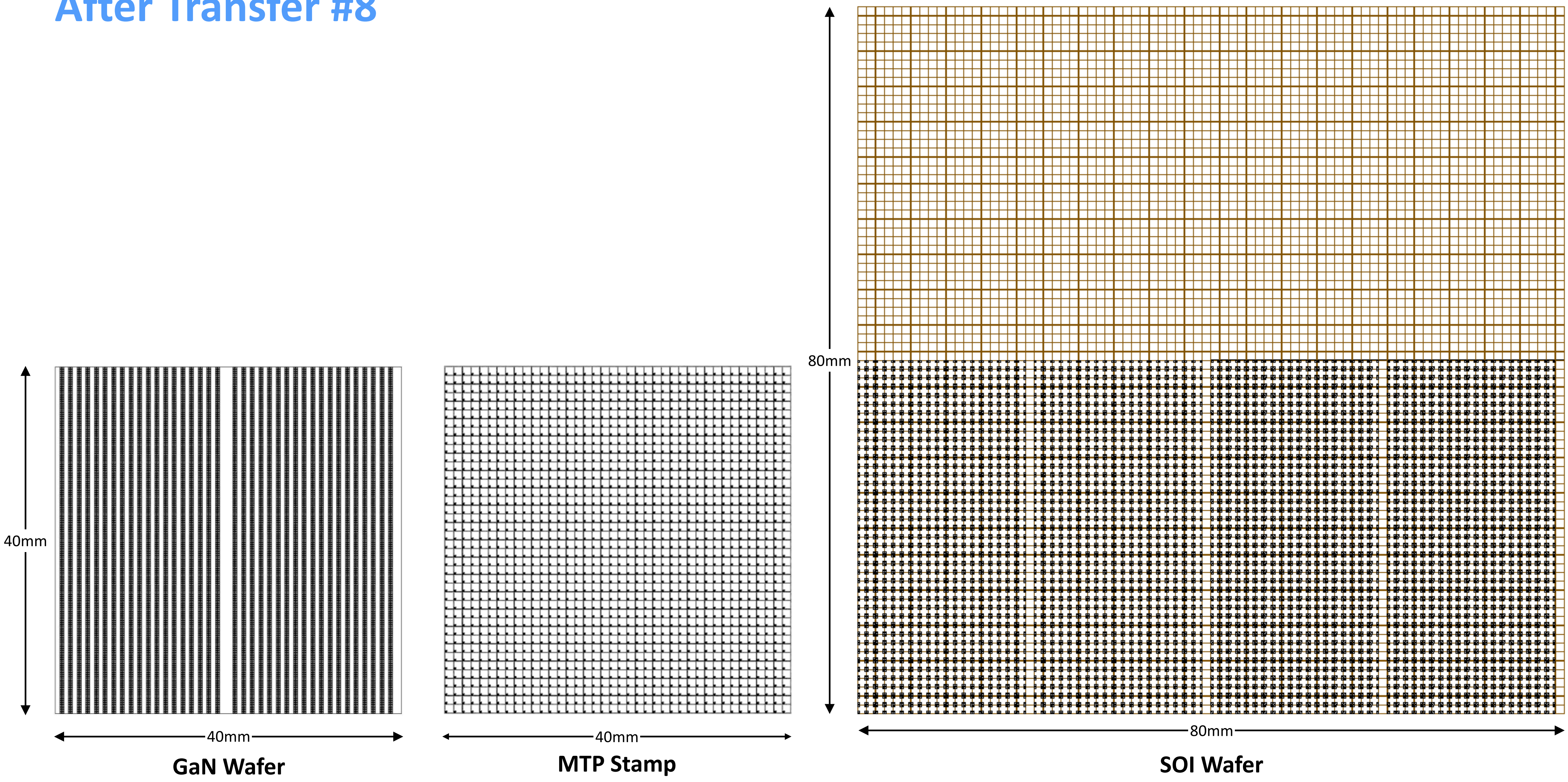


MTP Stamp

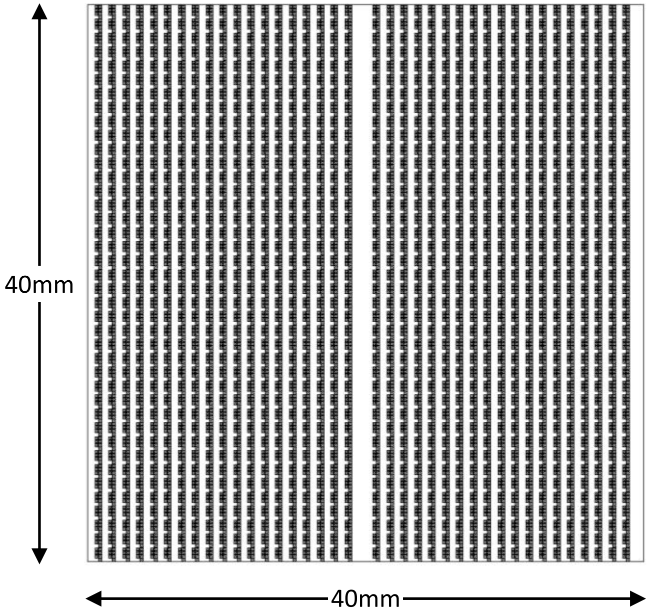


SOI Wafer

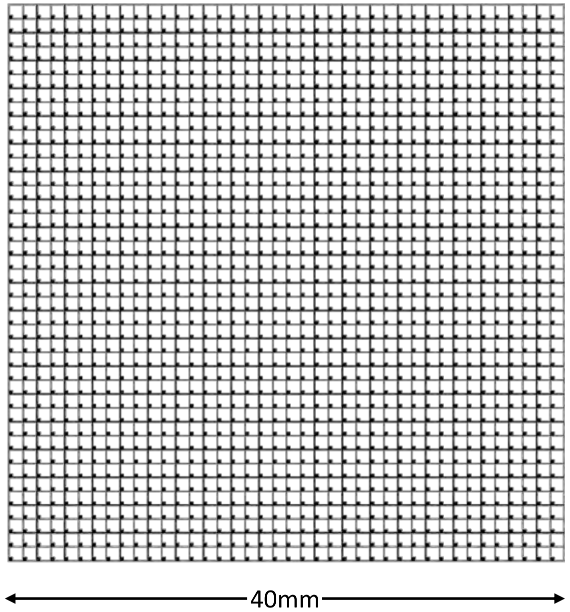
After Transfer #8



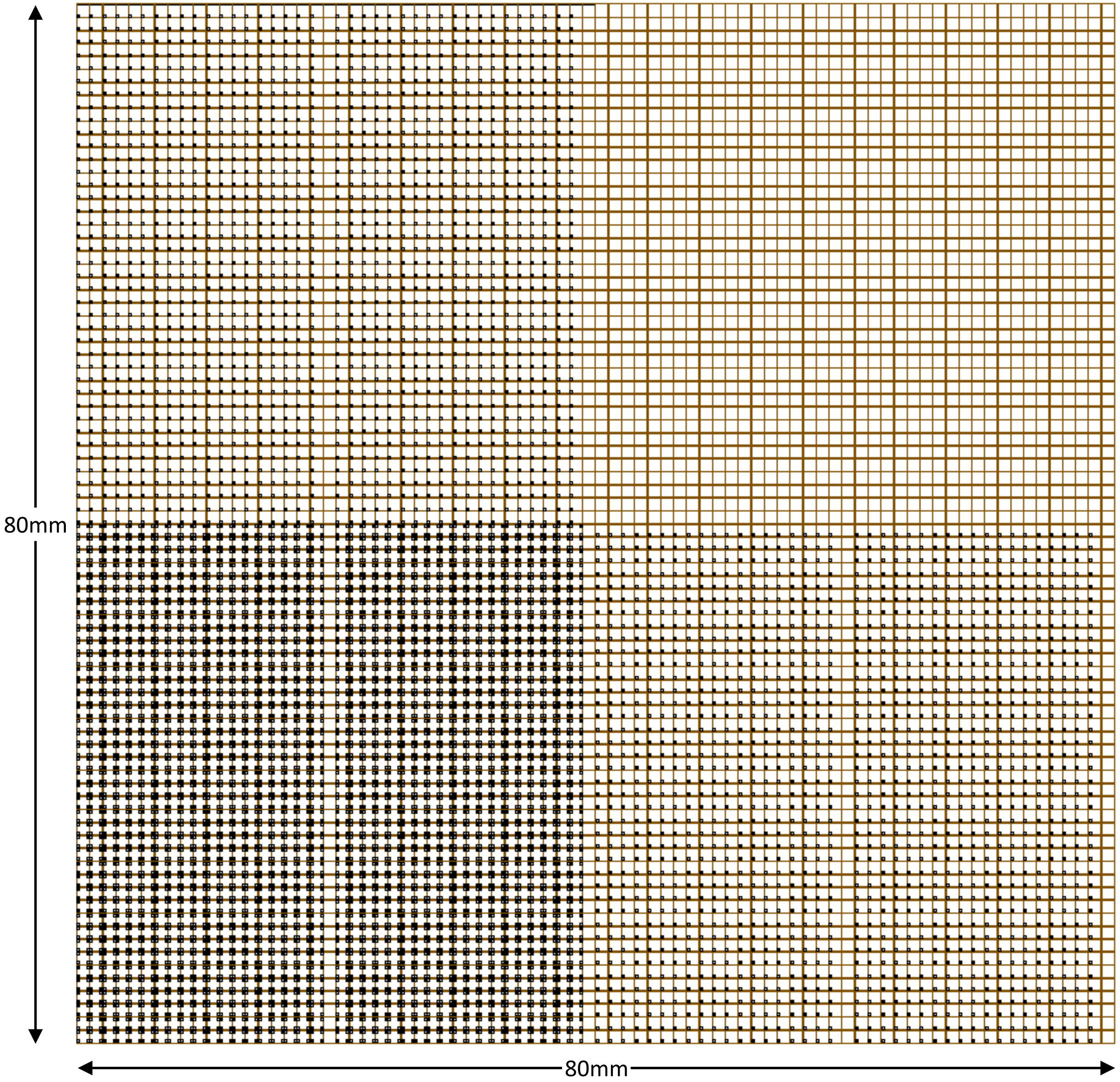
After Transfer #9



GaN Wafer

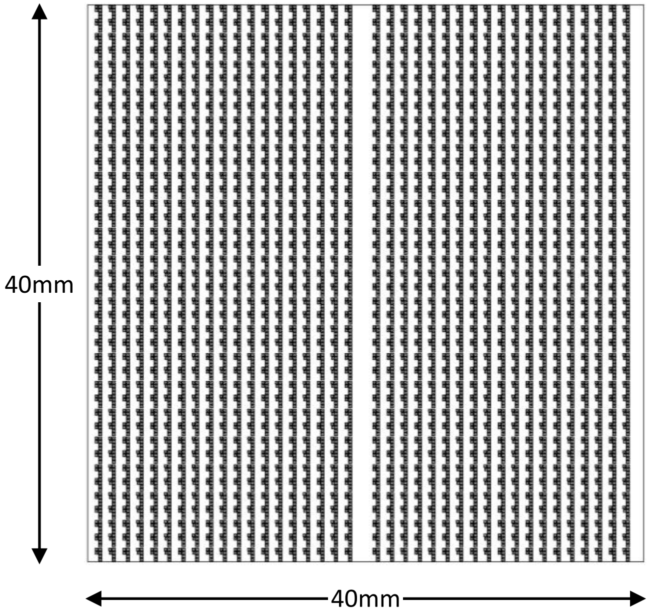


MTP Stamp

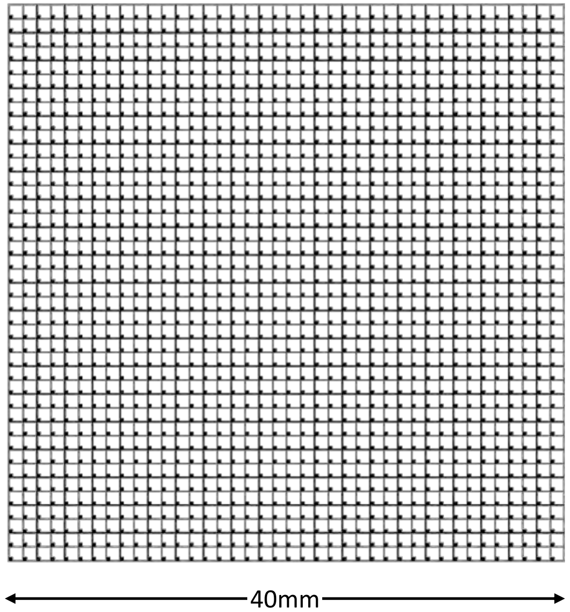


SOI Wafer

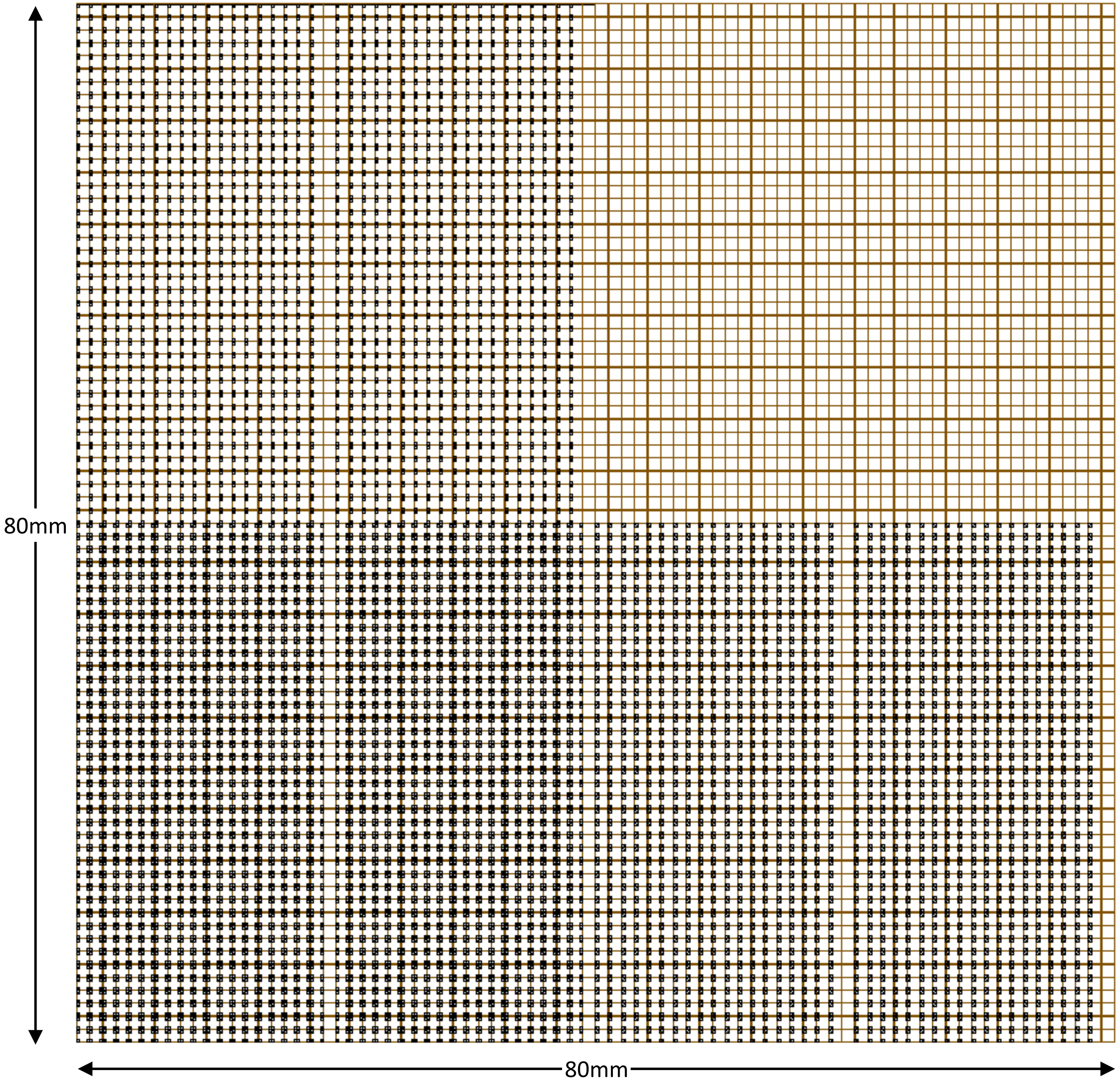
After Transfer #10



GaN Wafer

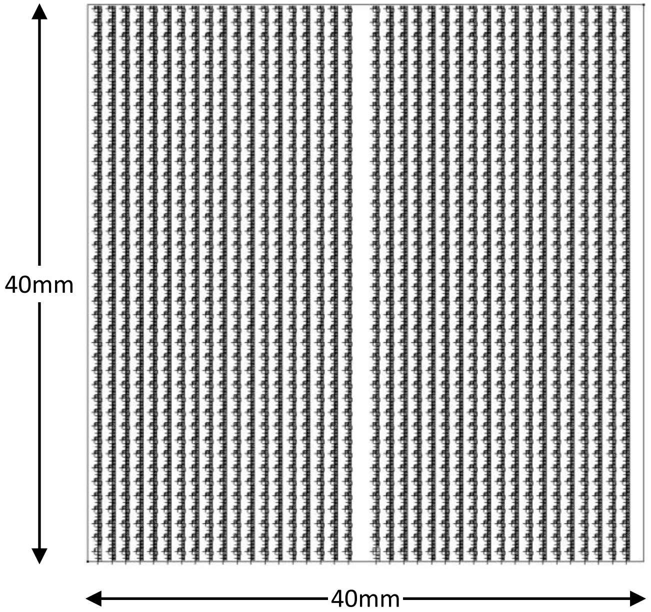


MTP Stamp

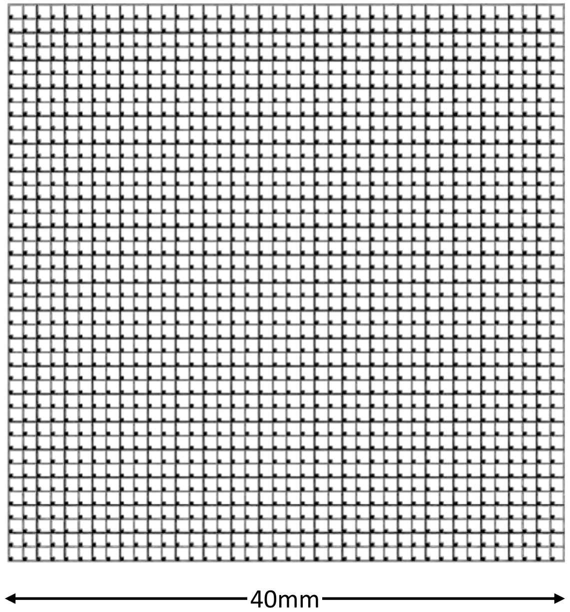


SOI Wafer

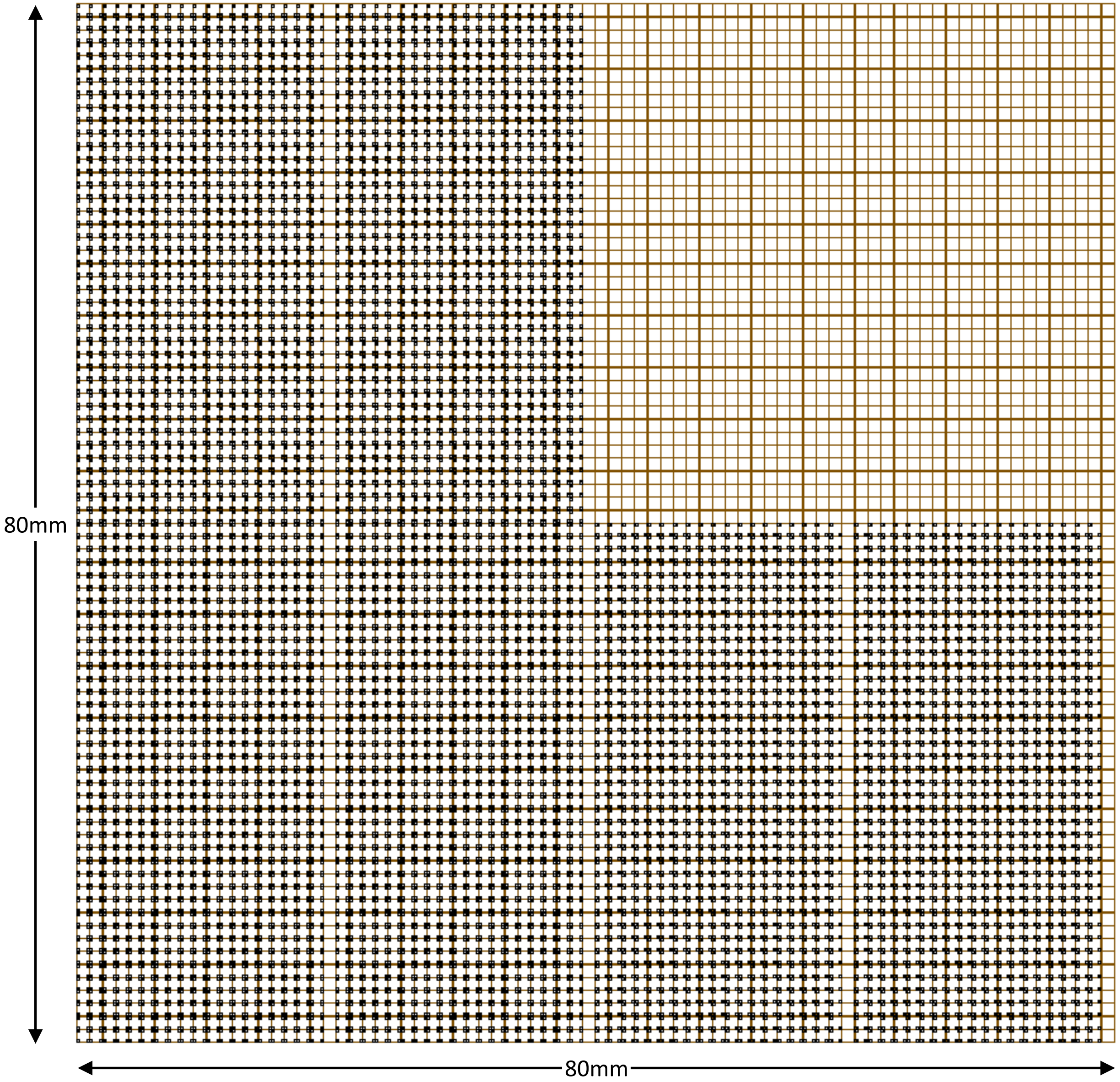
After Transfer #11



GaN Wafer

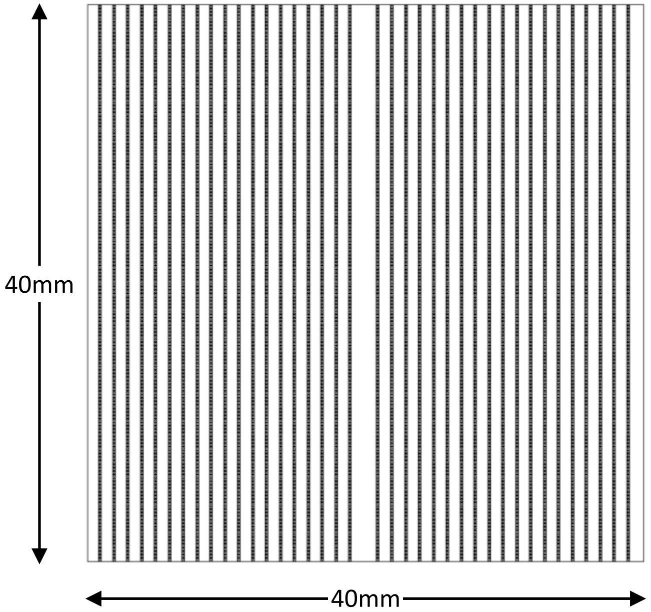


MTP Stamp

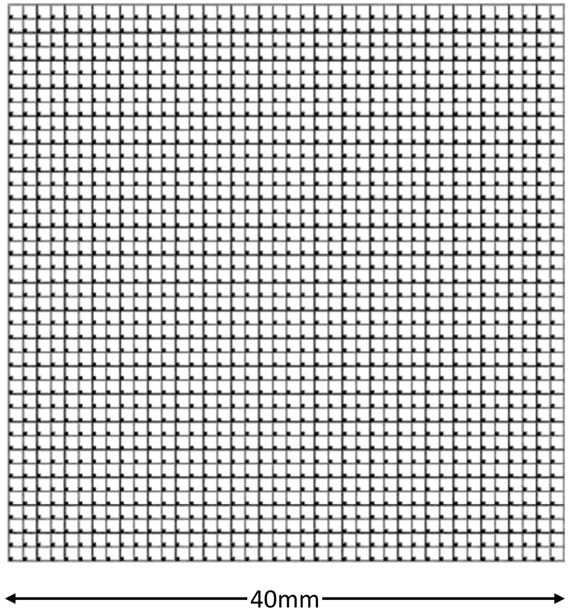


SOI Wafer

After Transfer #12



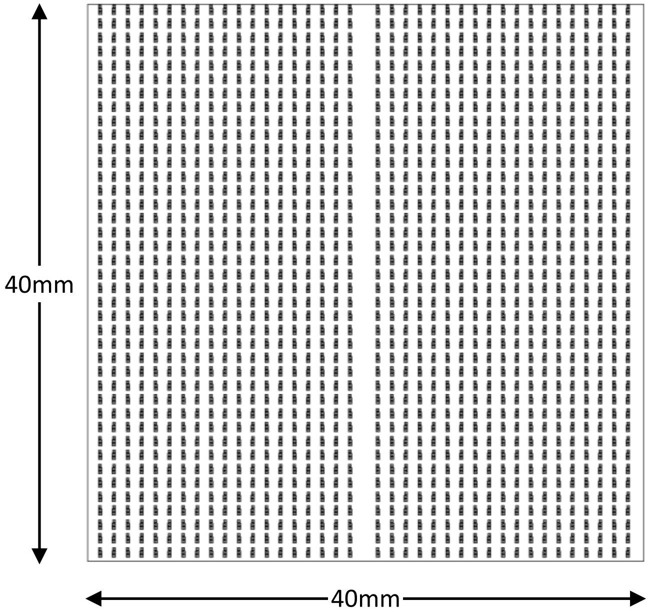
GaN Wafer



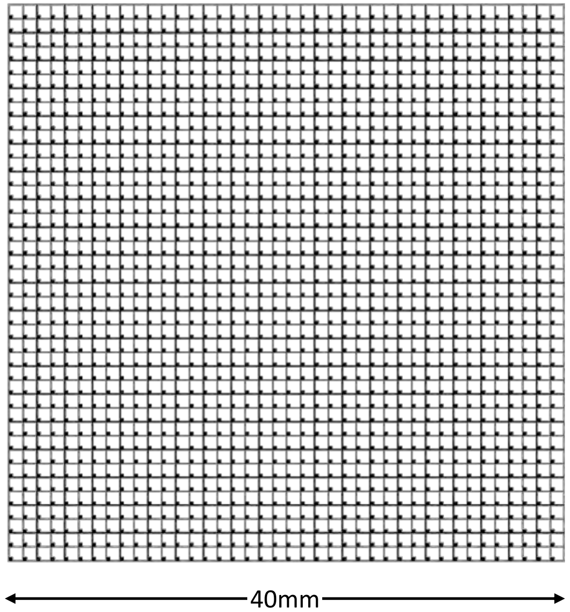
MTP Stamp

SOI Wafer

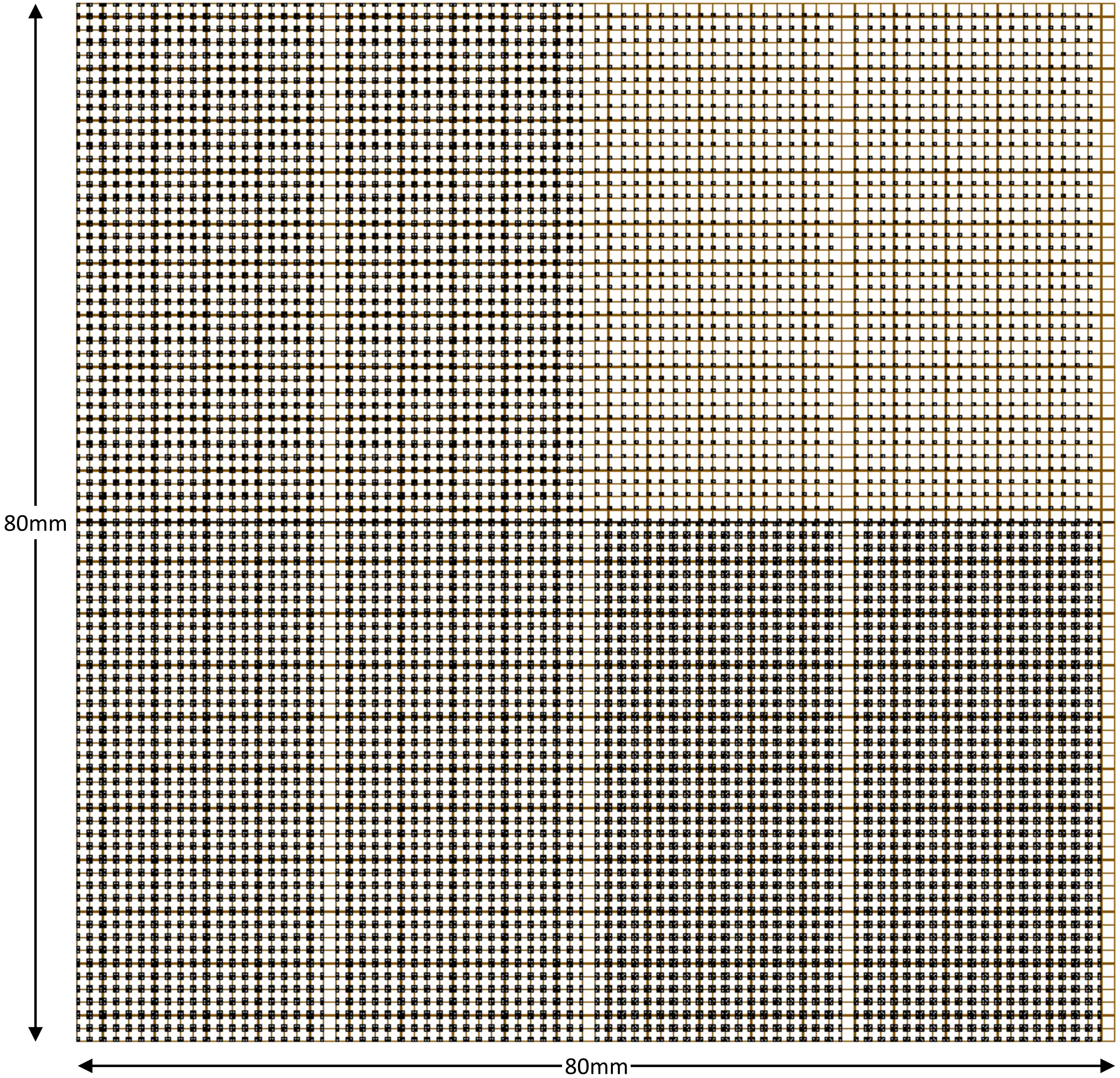
After Transfer #13



GaN Wafer

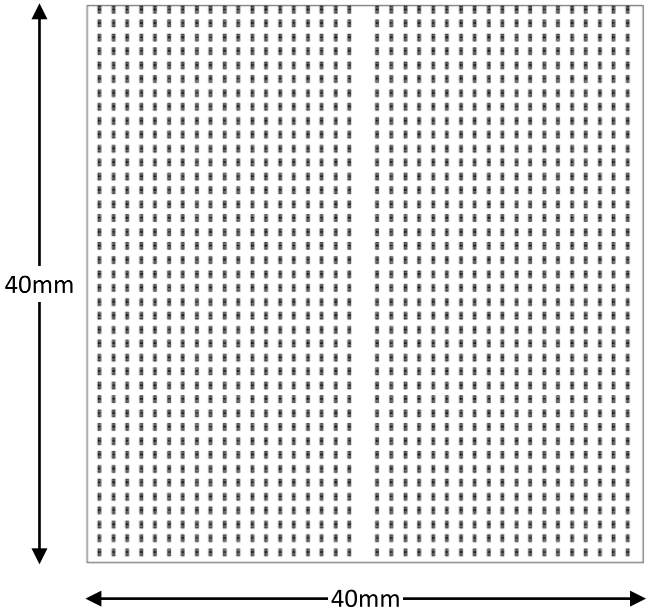


MTP Stamp

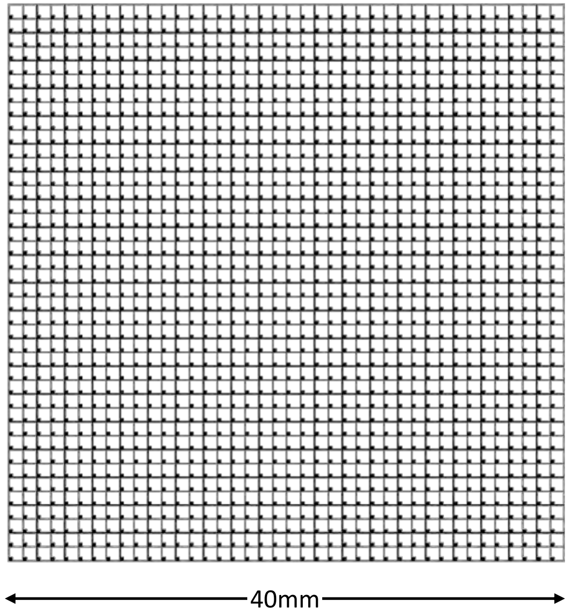


SOI Wafer

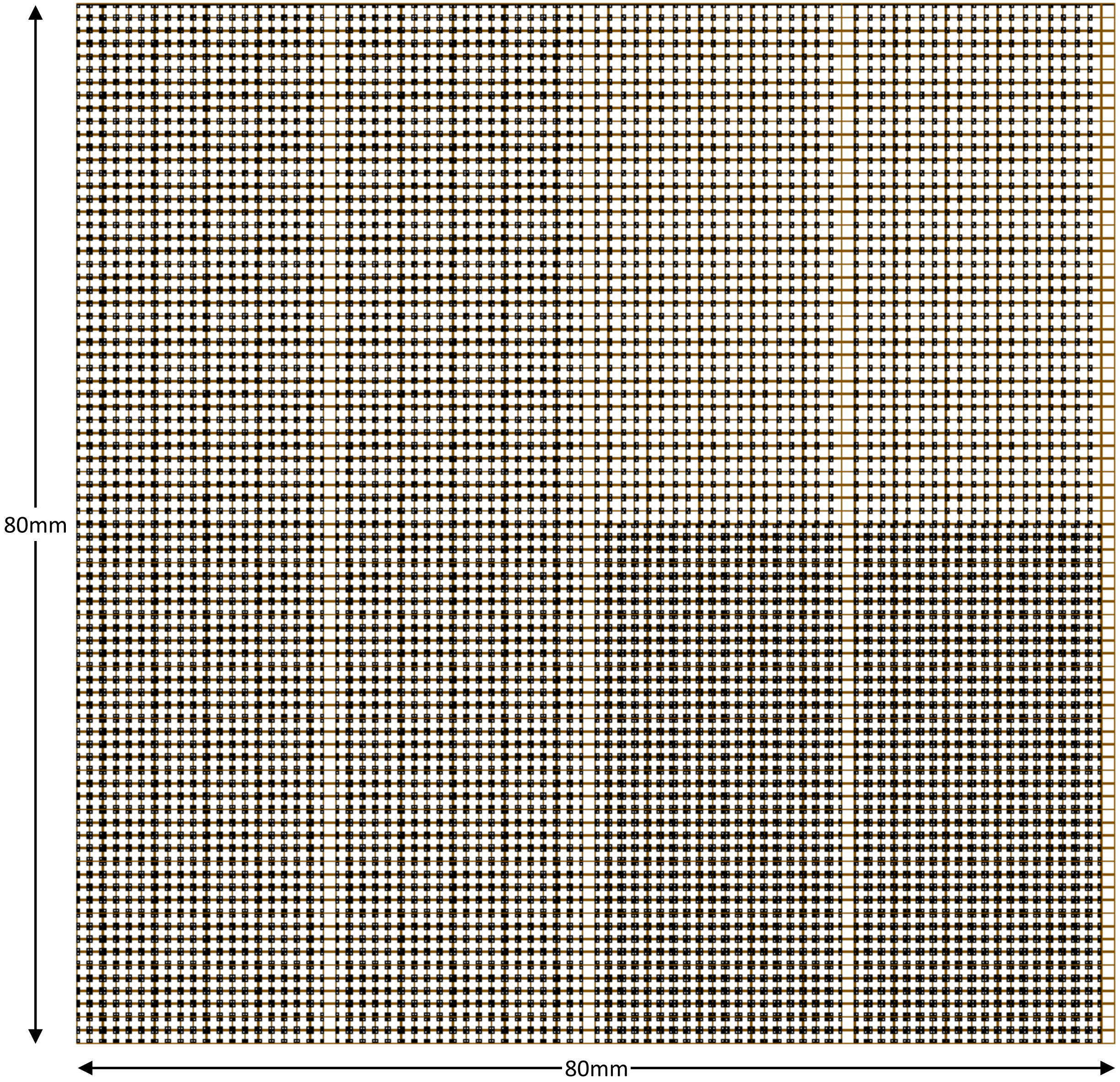
After Transfer #14



GaN Wafer

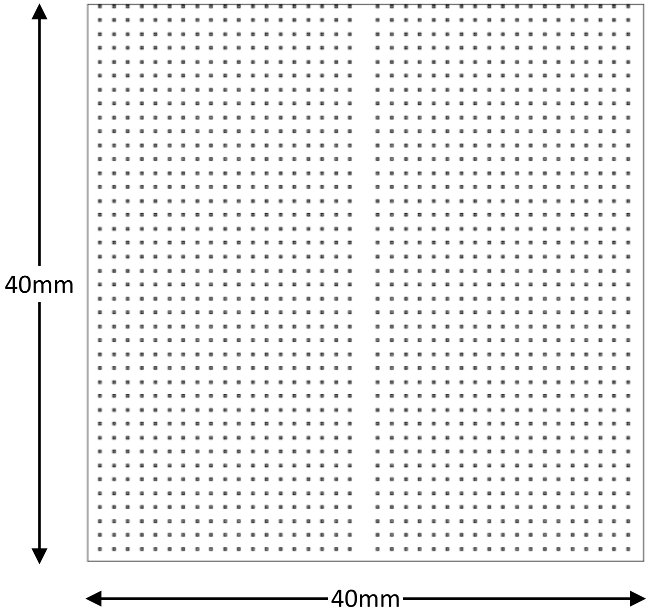


MTP Stamp

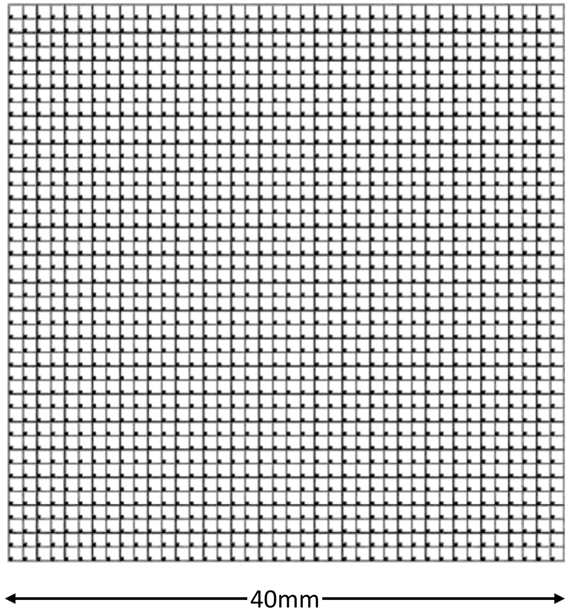


SOI Wafer

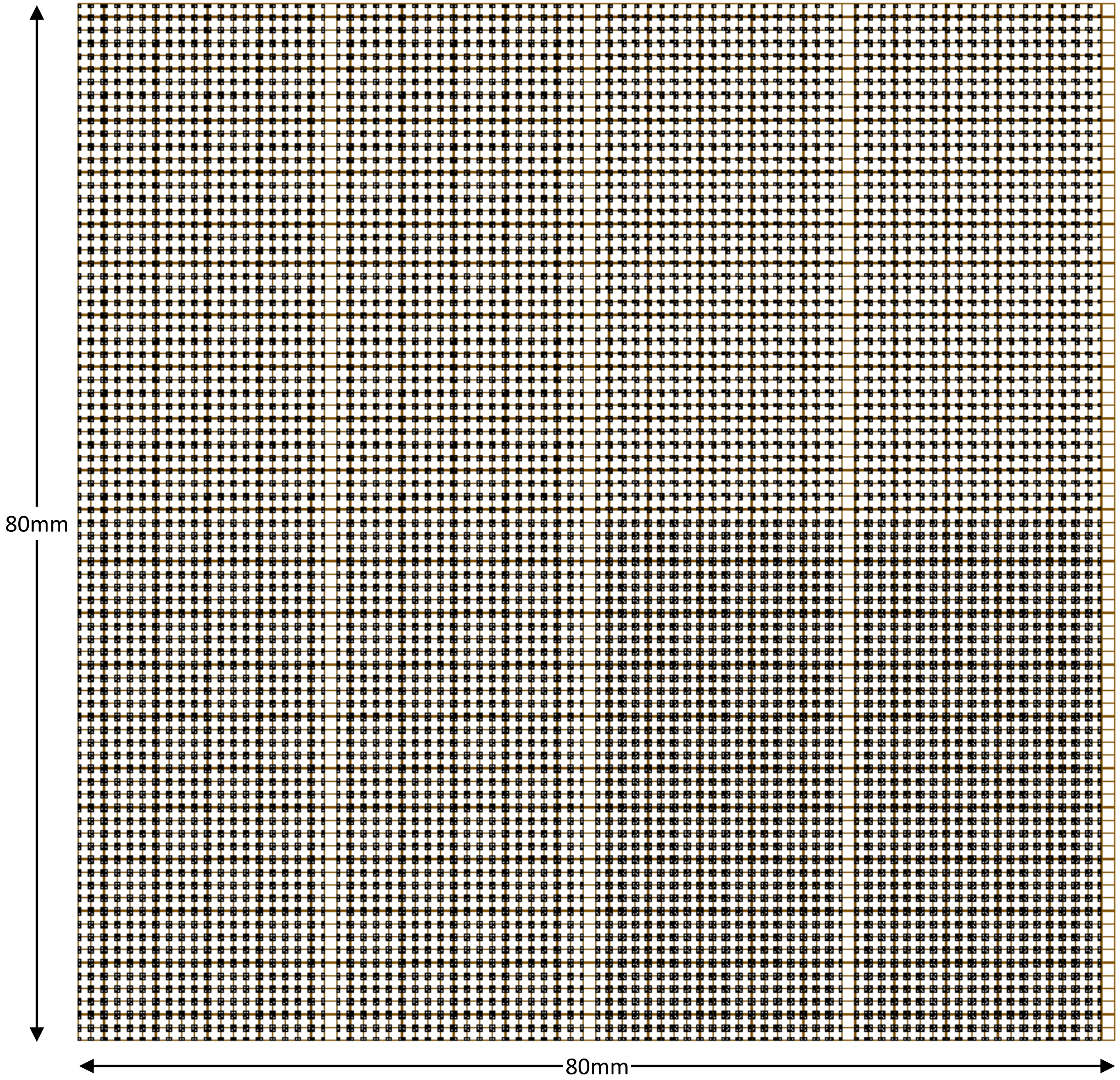
After Transfer #15



GaN Wafer

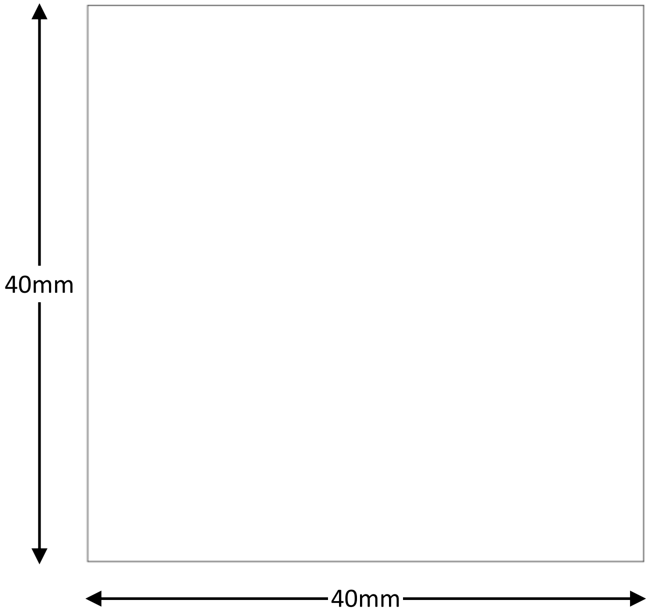


MTP Stamp

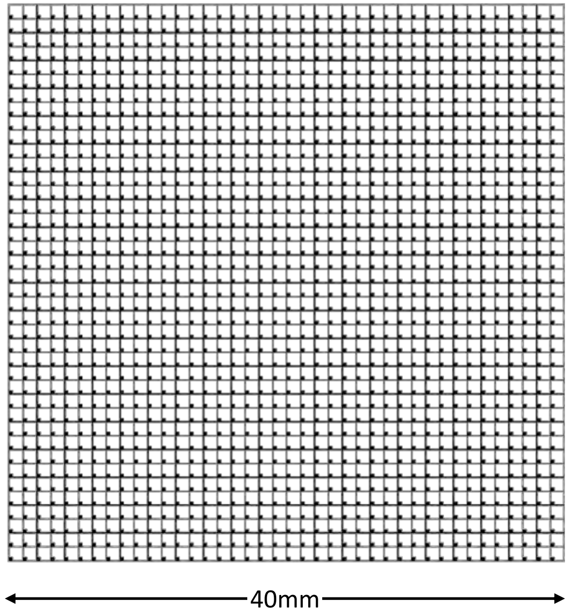


SOI Wafer

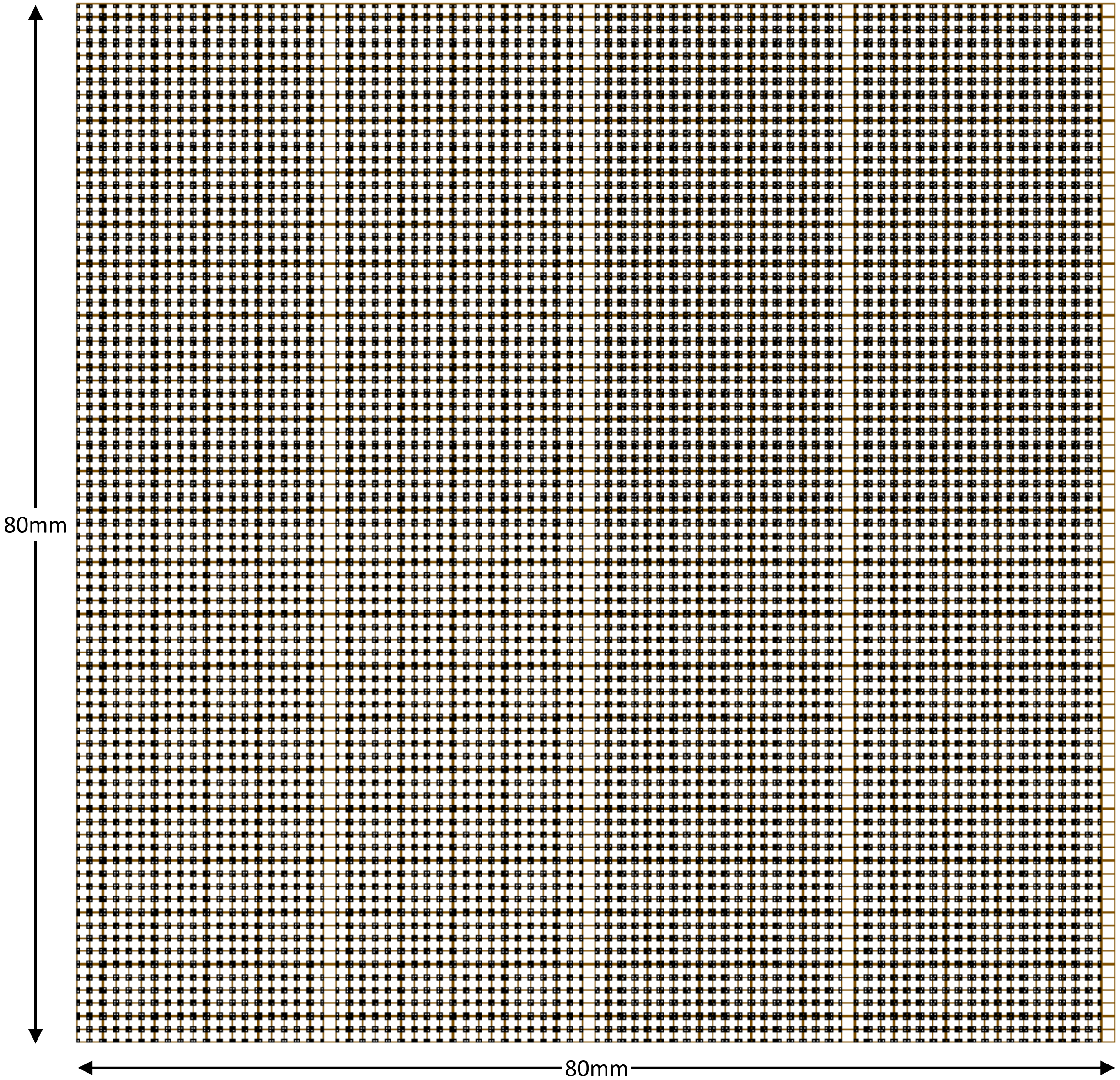
After Transfer #16



GaN Wafer

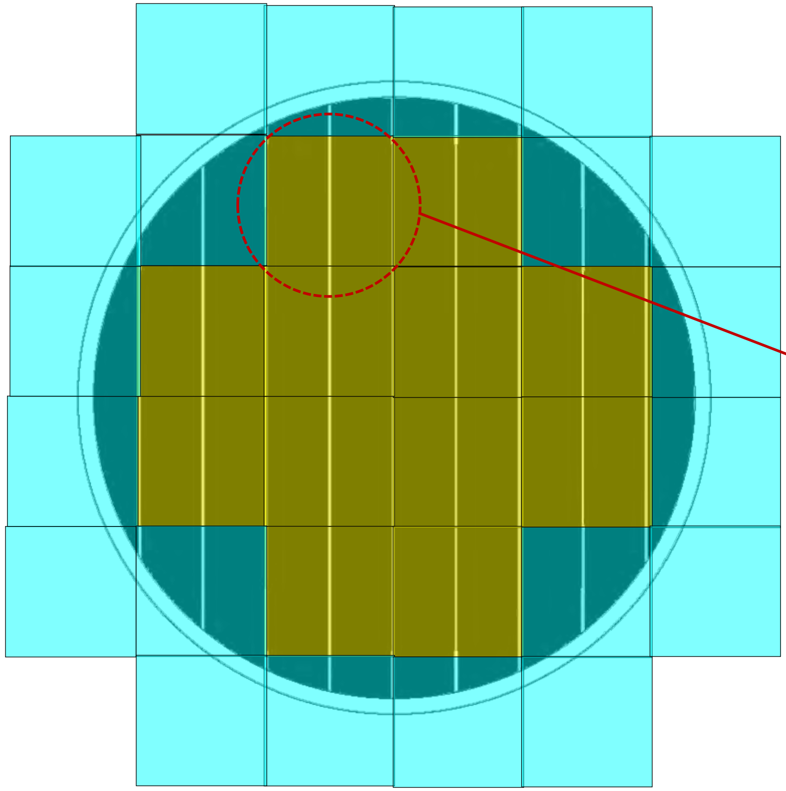


MTP Stamp



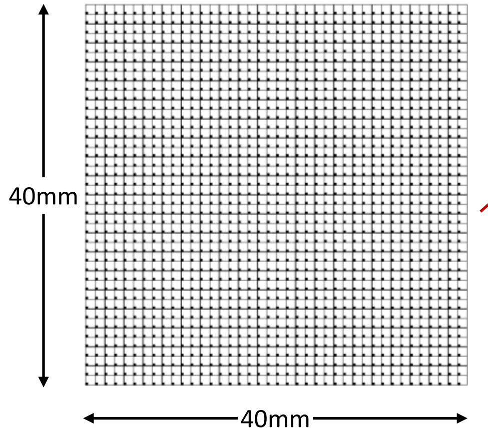
SOI Wafer

40x40mm MTP Stamp



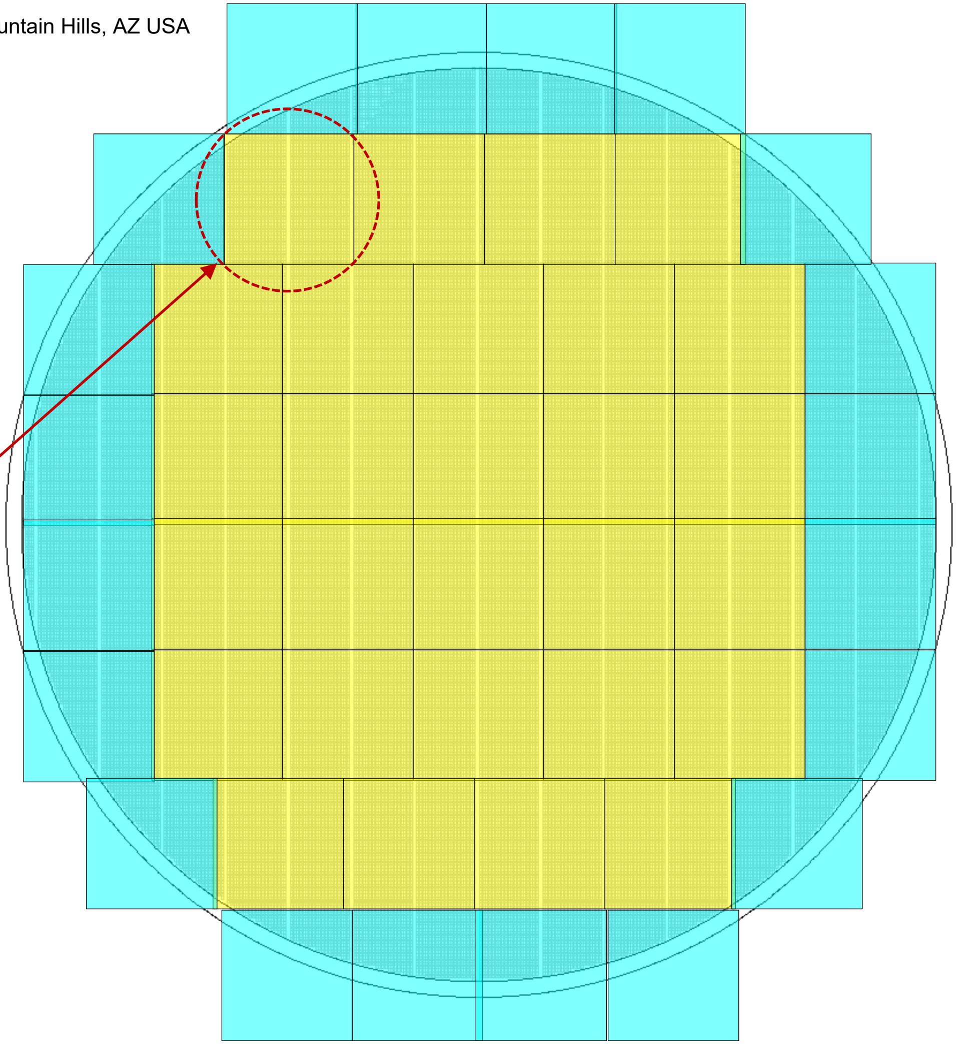
GaN Wafer

- 32 sites/wafer
  - 12 full
  - 20 edge
- 16 transfers / site
- Populates 1.8 SOI wafers
  - GaN x-chips are spread out
  - Each GaN site populates 4 SOI sites



MTP Stamp Close-Up

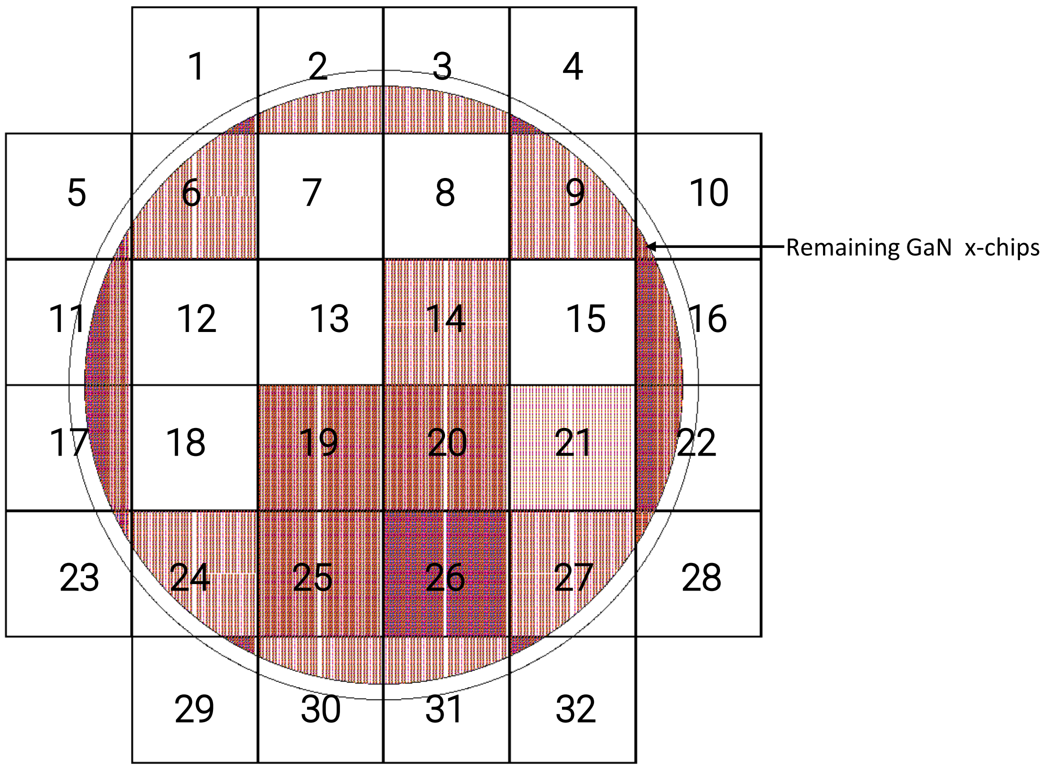
- Transfers 1,520 x-chips
  1,600 (40x40) – 80 for PCM
- 4 transfers per site



SOI Wafer

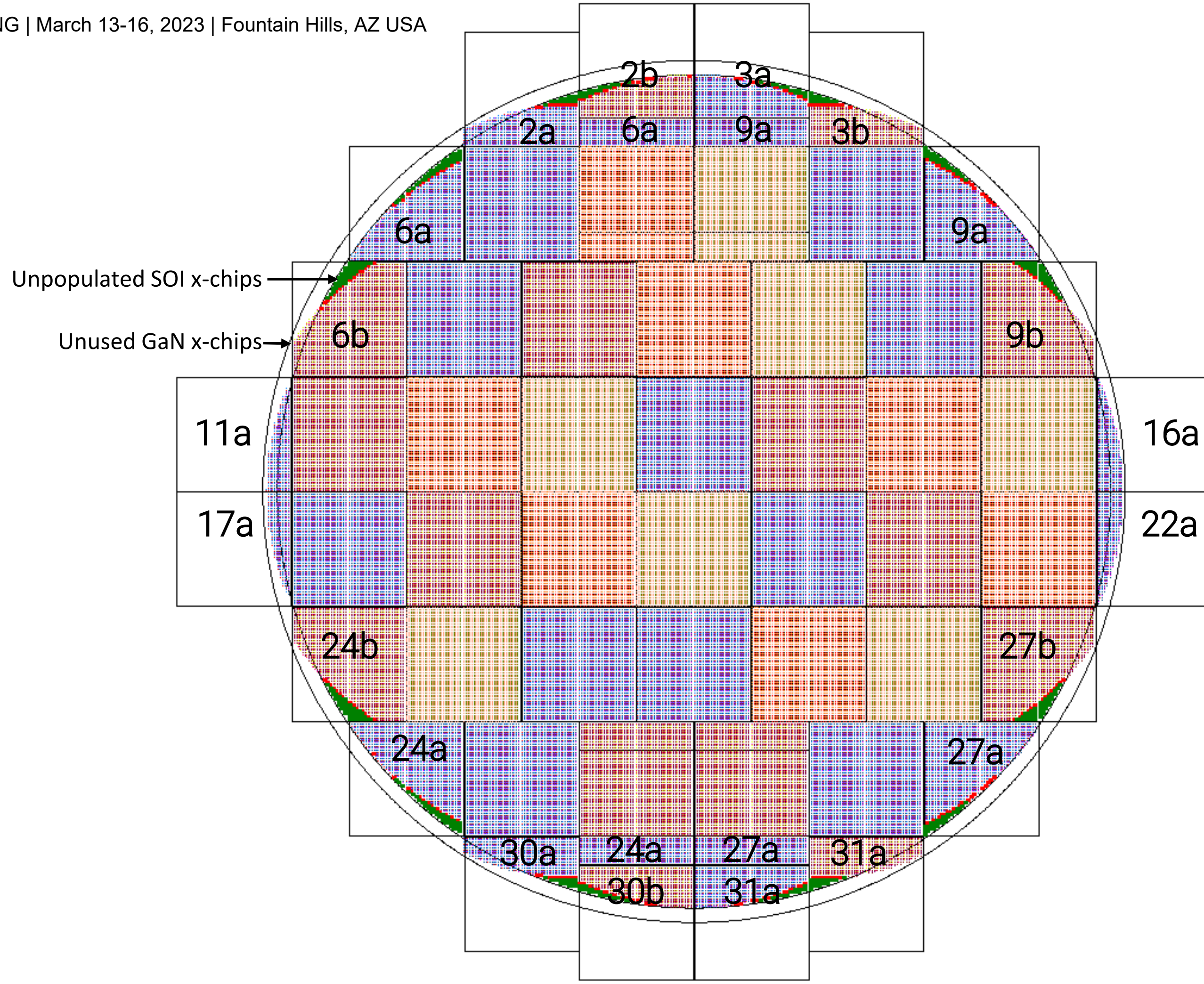
- 48 sites/wafer
  - 28 full
  - 20 edge
- 4 transfers / site

GaN Wafer #1 → SOI Wafer #1



GaN Wafer #1

Remaining GaN x-chips populate next SOI wafer



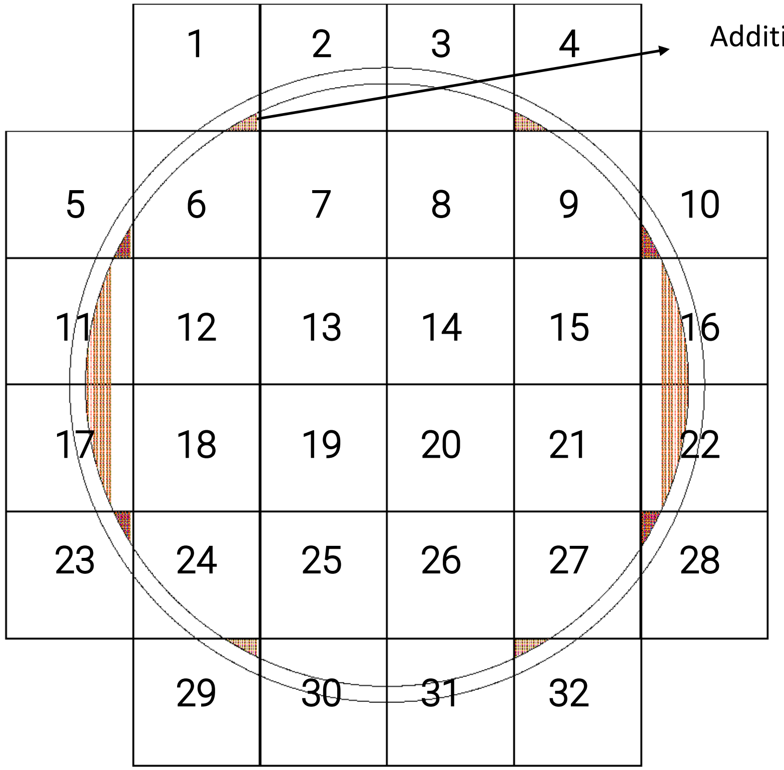
SOI Wafer #1

61,446 populated sites

98.83% Utilization

224 transfers
- 208 single
- 16 double

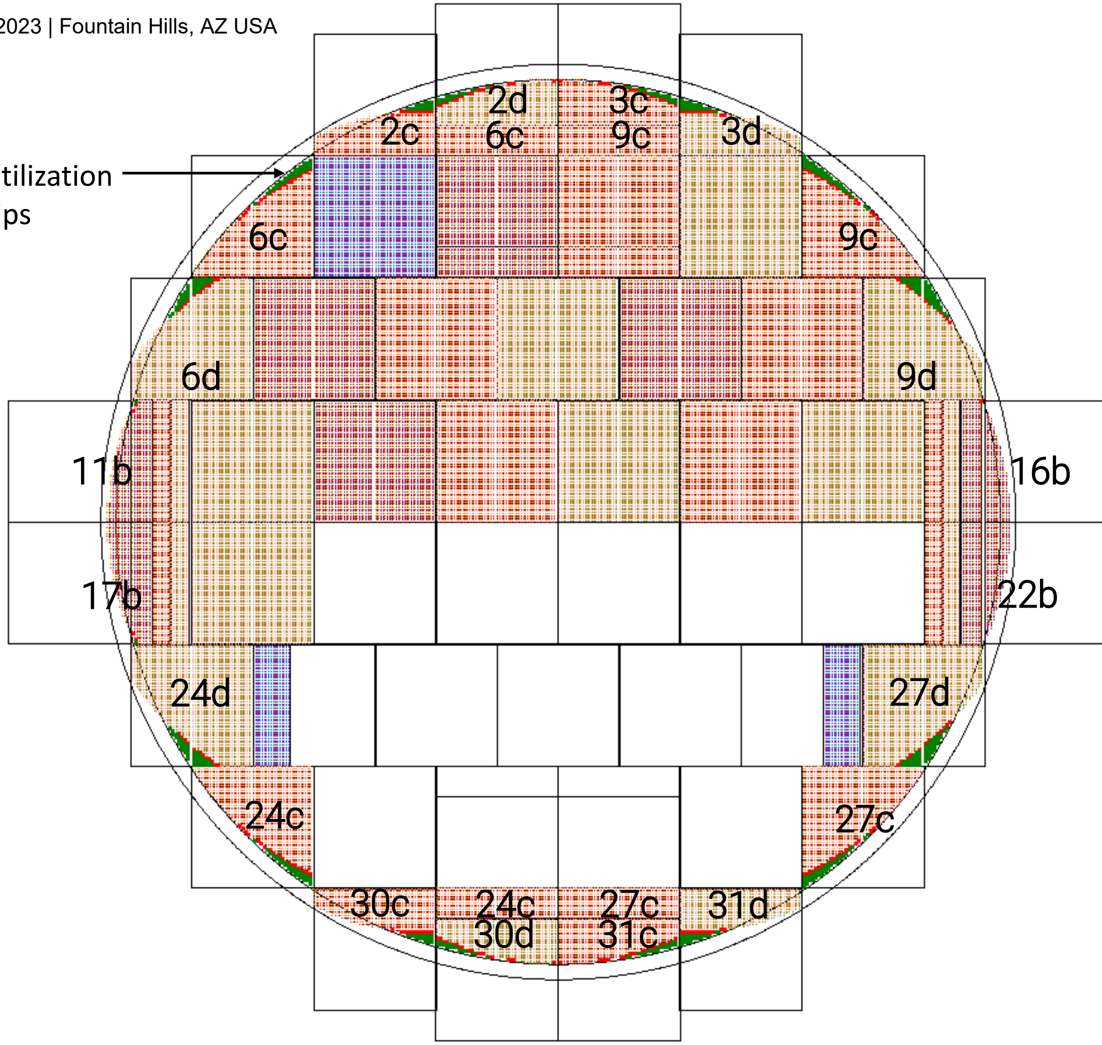
GaN Wafer #1 → SOI Wafer #2



GaN Wafer #1

Depleted with 95.45% wafer utilization

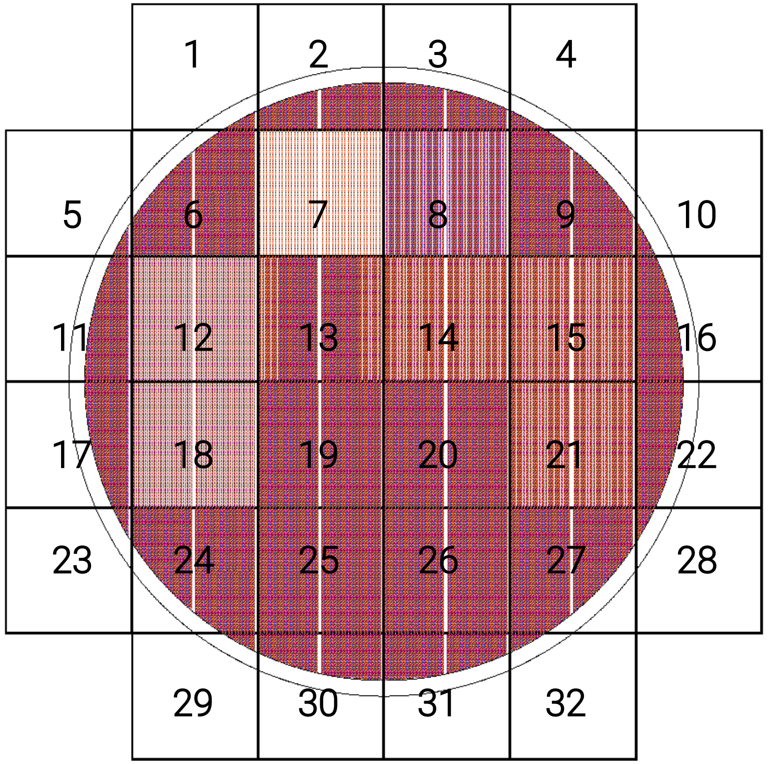
Additional transfers can further increase wafer utilization by transferring some remaining GaN x-chips to unpopulated SOI sites



SOI Wafer #2

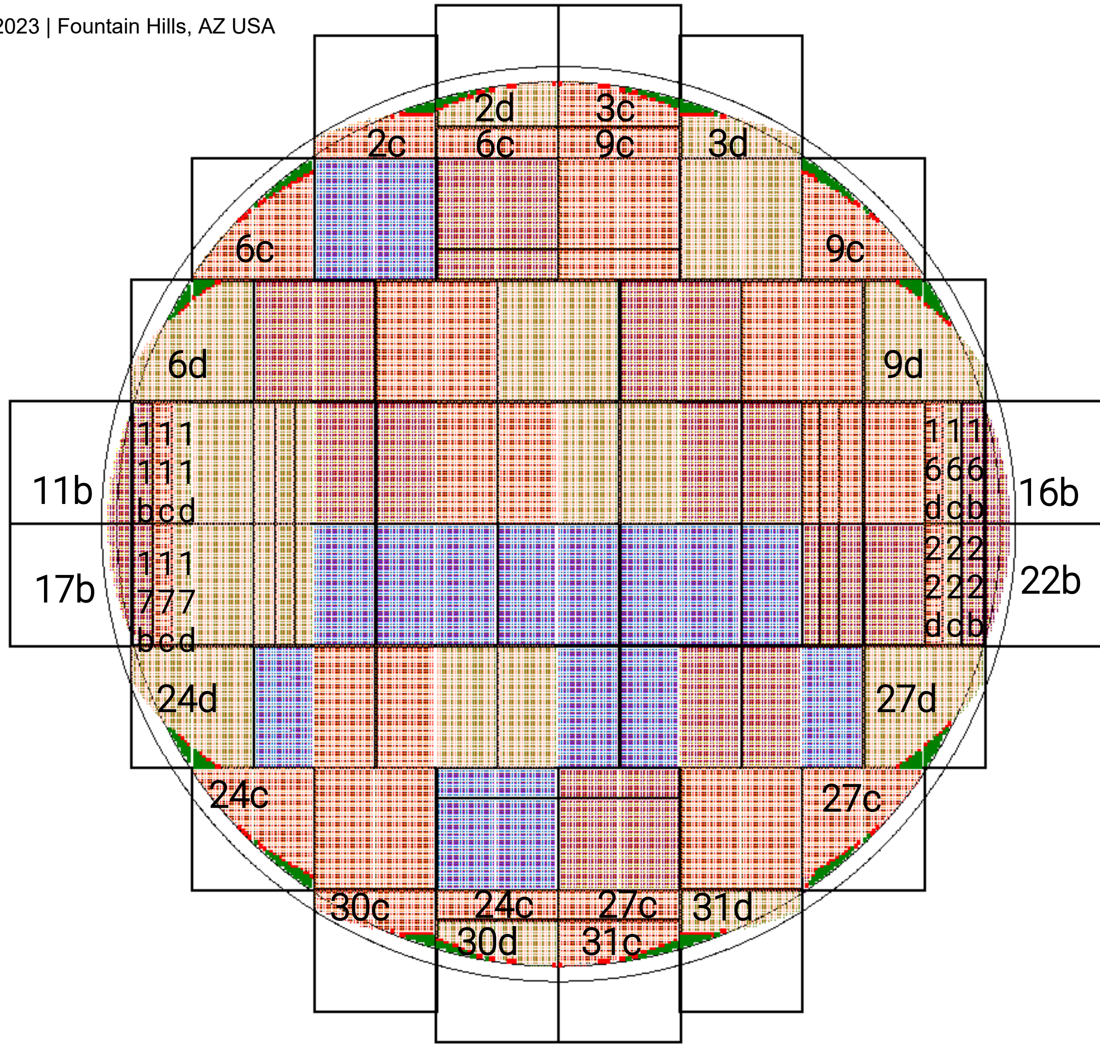
224 transfers

GaN Wafer #2 → SOI Wafer #2



GaN Wafer #2

Remaining GaN x-chips populate next SOI wafer



SOI Wafer #2

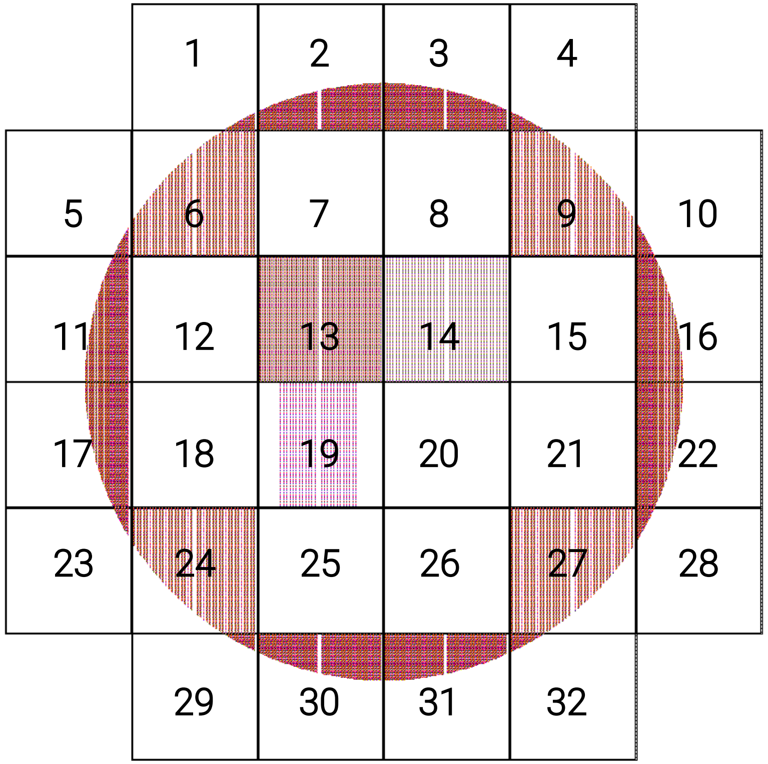
61,437 populated sites

98.81% Utilization

284 transfers

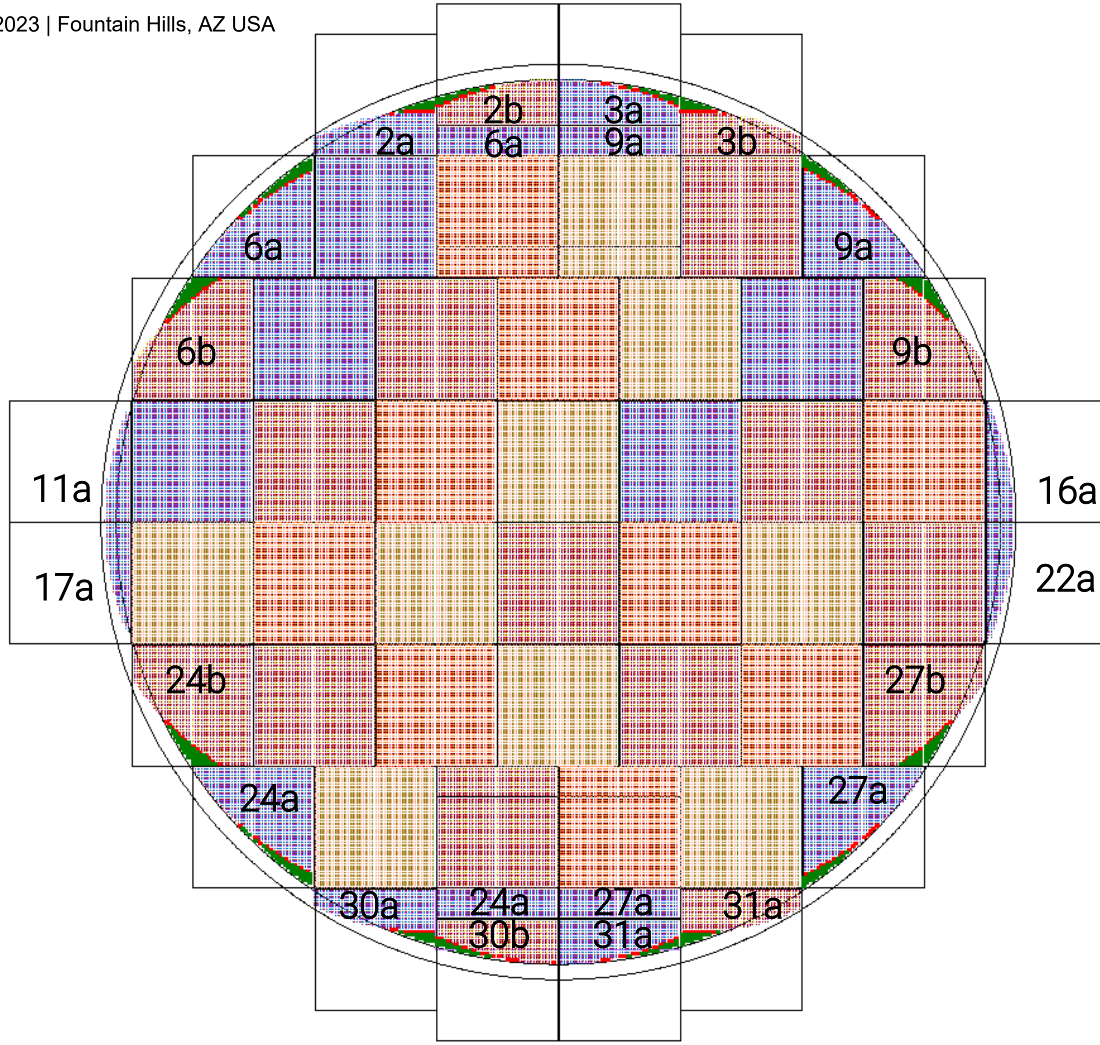
- 268 single
- 16 double

GaN Wafer #2 → SOI Wafer #3



GaN Wafer #2

Remaining GaN x-chips populate next SOI wafer



SOI Wafer #3

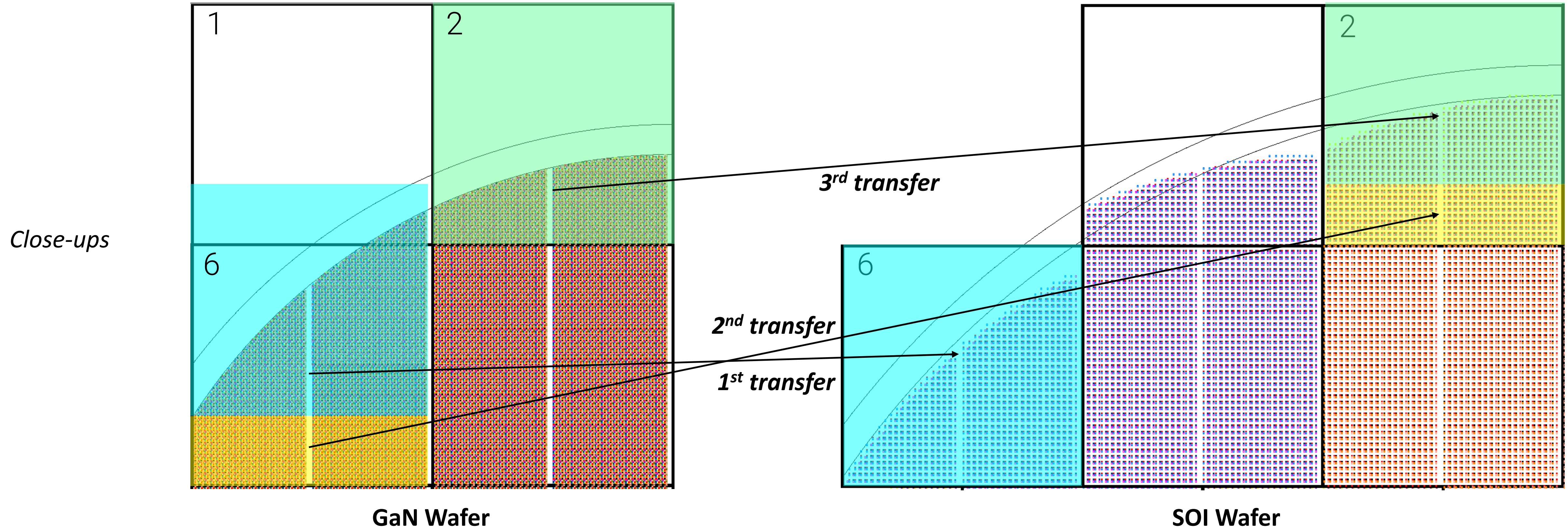
61,455 populated sites

98.84% Utilization

224 transfers
- 208 single
- 16 double

And so forth through SOI wafer #11 then MTP sequence repeats

Double Transfer Example

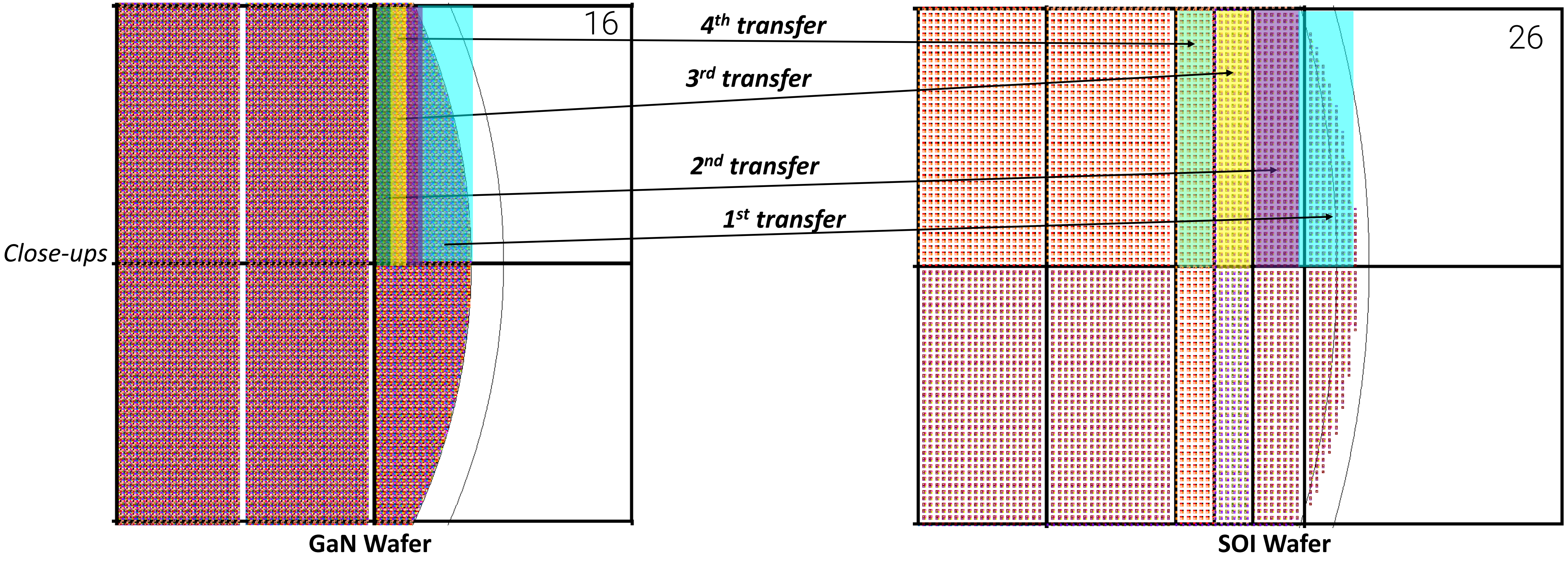


- Problem – a single transfer from:
  - GaN wafer site 2 to SOI wafer site 2 results in low SOI utilization
  - GaN wafer site 6 to SOI wafer site 6 wastes GaN x-chips (which fall outside useful SOI)
- Solution – improve wafer utliation by:
  - 1st transfer from GaN wafer site 1 and 6's upper portion to SOI wafer site 6
  - 2nd transfer from GaN wafer site 6's bottom portion to SOI wafer site 2's bottom portion
  - 3rd transfer from GaN wafer site 2 to SOI wafer site 2's upper portion
- Repeat for GaN Wafer sites #9, #24 and #27

FINWAVE

Multi Transfer Example

Site 16 to Site 26



The purple, yellow, and green highlighted regions above extend the full 40mm

Repeat for GaN Wafer sites #11, #17 and #22