Micro-Transfer Printing for Efficient 3DHI of 100-300mm Wafers and Glass Panels

Bob Conner
bconner@finwavesemi.com
(919) 757-6825
Celebrity (previously)

Bill Batchelor
bbatchelor@x-celeprint.com
(919) 522-5487

David Gomez
dgomez@x-celeprint.com
(512) 680-1459
Agenda

• Analog / mixed-signal 3DICs
  Three-dimensional heterogeneous integration

• Two levels of efficient 3DHI
  Three-dimensional heterogeneous integration

• Conclusions
Analog / Mixed Signal 3DICs

• Many dual use applications
  *High-volume, high-value commercial plus defense*
  - 5G/6G wireless communications
  - Satellite communications (Satcom)
  - Power management
    *Granular power delivery significantly improves microelectronics energy efficiency*

• Different requirements than “digital” (compute & memory) applications
  - Tight integration of large arrays of diverse ultra-thin, transferred chips (x-chips) on glass
    *Gallium nitride (GaN), silicon-on-insulator (SOI) and passives*
  - Higher power density
  - Lower I/O density
    ~10/10μm L/S (not ultra-fine) interconnects
  - Smaller form factor
    X, Y, Z dimensions

• Requires disruptive innovation
Disruptive Innovation

Use existing technology in new ways to disrupt markets

- GaN
- SOI
- Glass
- Micro-transfer printing

5G/ 6G / Satcom 3DIC

• **Increase efficiency** (*power output, hence, range*)

• **Improve performance** (*linearity*)

• **Reduce cost**

• **Tightly integrate arrays of RF components**
  *Readily scalable (4, 16, 32, 64, 128, etc. streams)*
  - GaN power amplifiers
  - SOI beam formers
  - Patch antennas

• **Address very large dual-use market**
Power 3DIC

• Leverages GaN-on-SOI 3DIC wireless communications ecosystem
• Addresses large markets requiring disruptive improvements in energy efficiency
  - 48V to 5V bus converters
  - 5V to <1V point-of-load voltage regulators
GaN-on-SOI Example

Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing

- Transferred chips (x-chips) are ultra-thin <10μm
- Standard spin-on planarization and thin-film metallization can be used for interconnect

RF Small and large signal characterization of a 3D integrated GaN/RFSOI SPST switch
RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique
Two Levels of 3DHI

1) Wafer Fab
   <100nm

2) GaN-on-SOI 3DIC
   GaN x-chip
   0.25x0.25mm
   SOI x-chip
   1x1mm

3) GaN-on-SOI-on-glass 3DIC
   4x4mm
   SOI
   Glass
   GaN
Analog / Mixed Signal 3DIC Ecosystem

Upgrade existing infrastructure to produce analog / mixed signal 3DICs

• Achieve economic and national security objectives

• Provide holistic co-design environment
  EDA tools and PDKs

• Stimulate innovation by providing open access rapid prototyping
  Universities, startups, government labs and research institutes

• Facilitate workforce development

Manufacturing ecosystem
• Rapid prototyping
• High volume production

1) Wafer Fab <100nm
2) GaN-on-SOI 3DHI
3) GaN-on-SOI-on-glass 3DHI

500mm x500mm Glass
GaN FinFETs

• 3D versus planar structure improves linearity, short channel effects and memory effects

• Produced in silicon wafer fabs
  <100nm nodes provides disruptive $f_t$, $f_{max}$, and $R_{DS(on)} \cdot Q_g$

• Robust
  High temperature, rad hard

Source: Finwave Semiconductor
Challenges

• Many mismatches
  * Substrate sizes, x-chip number, size and pitch

• Interconnects

• Yield

• Cost
  - Capex
  - Opex
  - Throughput
  - Substrate utilization

GaN x-chips located on SOI independently of each other

GaN x-chip 0.25x0.25mm

SOI x-chip 1x1mm

GaN

SOI

Glass

4x4mm

500 mm x 500 mm GaN-on-SOI-on-Glass

200 mm GaN

300 mm SOI

300 mm GaN-on-SOI

300 mm GaN-on-SOI-on-Glass

429,666 x-chips
  - 0.25x0.25mm
  - 20μm streets

62,174 x-chips
  - 1x1mm
  - 20μm streets

4,019 3DICs
  - 4x4mm
  - 80μm streets

13,920 3DICs
  - 4x4mm
  - 80μm streets

IMAPS 19th Conference on DEVICE PACKAGING | March 13-16, 2023 | Fountain Hills, AZ USA

FINWAVE

000291
GaN-on-SOI 3DIC

- Use z-dimension for vertical integration of GaN and SOI
- Ultra-thin active-side-up GaN enables RDL interconnection over top
- Heterogeneous “known good die” (KGD)
  - Resembles a monolithic KGD
  - Tested prior to downstream packaging
  - GaN x-chips embedded in SOI’s interconnects
  - RDL bridges interconnect gap between wafer fab and packaging

Source: Integrated Power Electronics Components for Integrated Voltage Regulators
GaN-on-SOI 3DIC

250µm GaN

Cross-section view

SOI x-chip 1x1mm

GaN x-chip 0.25x0.25mm

Top view

Cross-section view

3µm interconnect layer

GaN 2 Metal layers 5µm thick

SOI 5 metal layers 8.5µm

FINWAVE
Employ Micro-Transfer Printing (MTP) Technology Proven in Concentrator Photovoltaics (CPV)

- Fabricated surface mountable package with 600x600µm, 3-junction solar cells
- Smaller cell provides competitive advantages in CPV
- Thousands of target wafers printed in pilot production
- Highly reliable package
  >25 billion cell hours in field, passed rigorous reliability testing

Summary Statistics:

<table>
<thead>
<tr>
<th>Statistic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>0.933579</td>
</tr>
<tr>
<td>Std Dev</td>
<td>0.004993</td>
</tr>
<tr>
<td>Std Err Mean</td>
<td>0.0004873</td>
</tr>
<tr>
<td>Upper 95% Mean</td>
<td>0.9945453</td>
</tr>
<tr>
<td>Lower 95% Mean</td>
<td>0.9926128</td>
</tr>
<tr>
<td>N</td>
<td>105</td>
</tr>
</tbody>
</table>

Print Yield Distribution of 105 interposer wafers

- Sample of 105 interposer wafers, 4,866 die per wafer
- Solar cells printed from 150mm GaAs wafer to 150mm ceramic wafer
- Printed with a 24x24 post array stamp, 13 print cycles per target wafer
- Average print yield of 99.3%

24.5 kW CPV system

150mm ceramic wafer with 4,866 micro-transfer printed solar cells
MTP: Massively Parallel Pick-and-Place

GaN-on-SOI 3DIC heterogeneous integration providing high:

• Flexibility to efficiently handle mismatches
  *Wafer sizes, number of x-chips, x-chip sizes, x-chip pitches*

• Throughput

• Substrate utilization
  *GaN, SOI and glass*

• Placement accuracy
  *±1.5µm @ 3σ*

• Yield

ASAM AMICRA’s Nova+ MTP Manufacturing System

X-Display MTP Manufacturing System
Manufacturing Flow

1) GaN wafer fab
   With minimal number of metal interconnects

2) SOI wafer fab
   With minimal number of metal interconnects

3) Micro-transfer print GaN x-chips on SOI wafer → GaN-on-SOI 3DIC

4) Glass wafer fab
   With antenna arrays, passive components, through glass vias, cavities, thick RDL interconnects

5) Micro-transfer print GaN-on-SOI 3DICs on glass → GaN-on-SOI-on-glass 3DIC

6) Form additional RDL interconnects completing GaN-on-SOI-on-glass 3DIC
Mass Transfer GaN X-Chips
From 200mm Wafer to 300mm Wafer

200mm GaN Wafer
• 429,666 x-chips (0.25x0.25mm each)
• 95% wafer utilization

MTP Stamp Close-Up
• Transfers 1,520 x-chips
  1,600 (40x40) – 80 for PCM
• 4 transfers per site

300mm SOI Wafer
• 62,174 x-chips (1x1mm each)
• 98% wafer utilization
• 0.9 substrates/hour (4 transfers/site)
• 225,000 GaN x-chips/hour
Mass Transfer GaN-on-SOI 3DICs

From 300mm Wafer to 300mm Glass Wafer

- **300mm GaN-on-SOI Wafer**
  - 62,174 3DICs (1x1mm each)
  - 99.5% substrate utilization

- **MTP Stamp Close-Up**

- **300mm Glass Wafer**
  - 4,019 3DICs (4x4mm each)
  - 100% substrate utilization
  - 4 substrates/hour
  - 16,000 GaN-on-SOI 3DICs/hour
Mass Transfer GaN-on-SOI 3DICs

From 300mm Wafer to 500mm x 500mm Panel

300mm GaN-on-SOI Wafer
- 62,174 3DICs (1x1mm each)
- 96% substrate utilization

500 mm x 500mm Glass Panel
- 13,920 3DICs (4x4mm each)
- 100% substrate utilization
- 1.3 substrates/hour
- 18,096 GaN-on-SOI 3DICs/hour
MTP System Transfers X-Chips Active-Side Up from Source to Destination

• Stamp’s posts adhere to x-chips via van der Waals force
• Stamp’s visco-elastic behavior
  - Fast separation speed in pick-up regime
  - Slow separation speed in printing regime
• Stamp pick-up breaks tethers and removes x-chips
• Massively parallel selective pick-and-place of many x-chips
• Readily transfers ultra-thin and fragile x-chips
• Stamp contacts destination substrate and x-chips stick to new surface via:
  - van der Waals force
  - Ultra-thin adhesive
• Placement with controllable pitch and pattern
  Geometric magnification (fan-out)

Transfer printing by kinetic control of adhesion to an elastomeric stamp
Stamp’s Post Configuration Matched to X-Chip Spacing on Destination Substrate
For “Geometric Magnification” (Fan-Out)

close-up views

Source wafer
Densely-packed x-chips with pitch matching integral x/y multiples of placement on destination substrate

MTP stamp
Post configuration matched to x-chip spacing on destination substrate

Destination substrate
Distance between x-chips in x/y determines stamp's post configuration

IC on destination substrate
x-chip face up on top
## MTP vs. W2W vs. D2W Comparison

<table>
<thead>
<tr>
<th></th>
<th>MTP</th>
<th>D2W</th>
<th>W2W</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cost Factor</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Throughput</strong></td>
<td>High</td>
<td><strong>Very low</strong></td>
<td>High</td>
</tr>
<tr>
<td><strong>GaN Wafer Utilization</strong></td>
<td>High</td>
<td>High</td>
<td><strong>Very low</strong></td>
</tr>
<tr>
<td><strong>SOI Wafer Utilization</strong></td>
<td>High</td>
<td>High</td>
<td><strong>Very low</strong></td>
</tr>
<tr>
<td><strong>Yield</strong></td>
<td>High</td>
<td>High</td>
<td><strong>Lower</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Ability to handle small, thin, x-chips?</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>More process steps</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Conclusions

For wireless communications and power management applications

*Two large dual use markets requiring disruptive 3DHI*

- GaN FinFETs meet challenging efficiency, performance and cost targets
- Micro-transfer printing enables two levels of efficient 3DHI
- GaN 3DICs provide U.S. and allied nations with many opportunities
  - Sustainable technological superiority
  - High-volume production
    *Defense and commercial dual-use*
  - Workforce development
    *Plus many attractive career opportunities*
  - Catalyze innovation
    *Universities, government labs, research institutes and start-ups*
Appendix
MTP Transfer of GaN X-Chips from 200mm GaN Wafers to 300mm SOI Wafers

High wafer utilization achieved by:
• Populating 11 SOI wafers with 6 GaN wafers
• 40x40mm MTP stamp going over:
  - Edge of wafer
  - Previously transferred sites
    So some MTP transfers are effectively <40x40mm
• Using different sequence of MTP transfers for each wafer
  Sequence repeats after 11 SOI wafers

MTP transfer sequence is different for each of 11 SOI wafers

Blue area shows portion of site populated by 40x40mm stamp:
• Lower portion
• Lower portion
• Full

Unused GaN x-chips

Depleted GaN Wafer

Remaining GaN x-chips

Unpopulated SOI x-chips

Populated SOI Wafer #1

Populated SOI Wafer #2

Populated SOI Wafer #3

PCM area
Assume 20mm Reticle With 1mm PCM Area on Edge
For Source and Destination Wafers

1mm PCM width equal to width of:
- 4 GaN x-chips (0.25x0.25mm each)
- 1 SOI x-chip (1x1mm each)

6,080 (76x80) GaN x-chips
320 (4x80) GaN x-chips lost due to PCM

380 (19x20) SOI x-chips
20 (1x20) SOI x-chips lost due to PCM

Stamp has posts not populated with x-chips during MTP transfers

Different (smaller) PCM areas can be accommodated
Before Transfer #1

- **GaN Wafer**
  - 0.25x0.25mm GaN x-chips

- **MTP Stamp**
  - 1,600 posts

- **SOI Wafer**
  - 1x1mm SOI x-chips
After Transfer #1

Transfer GaN x-chip in **bottom left** of each SOI x-chip

GaN Wafer

MTP Stamp

SOI Wafer

PCM area
After Transfer #2

Transfer GaN x-chip in upper left of each SOI x-chip
After Transfer #3

Transfer GaN x-chip in lower right of each SOI x-chip

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #4

Transfer GaN x-chip
in upper right
of each SOI x-chip
After Transfer #5

Transfer GaN x-chips to next site on SOI wafer
After Transfer #6

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #7

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #8

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #9

- **GaN Wafer**: 40mm x 40mm
- **MTP Stamp**: 40mm x 40mm
- **SOI Wafer**: 80mm x 80mm
After Transfer #10

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #11

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #12

GaN Wafer

MTP Stamp

SOI Wafer

40mm

40mm

80mm

80mm

FINWAVE
After Transfer #13

GaN Wafer

MTP Stamp

SOI Wafer

40mm

80mm
After Transfer #14

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #15

GaN Wafer

MTP Stamp

SOI Wafer
After Transfer #16

GaN Wafer

MTP Stamp

SOI Wafer

40mm

80mm
40x40mm MTP Stamp

GaN Wafer
- 32 sites/wafer
  - 12 full
  - 20 edge
- 16 transfers / site
- Populates 1.8 SOI wafers
  - GaN x-chips are spread out
  - Each GaN site populates 4 SOI sites

SOI Wafer
- 48 sites/wafer
  - 28 full
  - 20 edge
- 4 transfers / site

MTP Stamp Close-Up
- Transfers 1,520 x-chips
  1,600 (40x40) – 80 for PCM
- 4 transfers per site
GaN Wafer #1 $\rightarrow$ SOI Wafer #1

Remaining GaN x-chips populate next SOI wafer

---

224 transfers
- 208 single
- 16 double

---

SOI Wafer #1
61,446 populated sites
98.83% Utilization
GaN Wafer #1 → SOI Wafer #2

Additional transfers can further increase wafer utilization by transferring some remaining GaN x-chips to unpopulated SOI sites.

GaN Wafer #1
Depleted with 95.45% wafer utilization

224 transfers
GaN Wafer #2 $\rightarrow$ SOI Wafer #2

Remaining GaN x-chips populate next SOI wafer

284 transfers
- 268 single
- 16 double

SOI Wafer #2
61,437 populated sites
98.81% Utilization
GaN Wafer #2 ➔ SOI Wafer #3

Remaining GaN x-chips populate next SOI wafer

224 transfers
• 208 single
• 16 double

And so forth through SOI wafer #11 then MTP sequence repeats

SOI Wafer #3
61,455 populated sites
98.84% Utilization
Double Transfer Example

• Problem – a single transfer from:
  - GaN wafer site 2 to SOI wafer site 2 results in low SOI utilization
  - GaN wafer site 6 to SOI wafer site 6 wastes GaN x-chips (which fall outside useful SOI)

• Solution – improve wafer utilization by:
  - 1st transfer from GaN wafer site 1 and 6’s upper portion to SOI wafer site 6
  - 2nd transfer from GaN wafer site 6’s bottom portion to SOI wafer site 2’s bottom portion
  - 3rd transfer from GaN wafer site 2 to SOI wafer site 2’s upper portion

• Repeat for GaN Wafer sites #9, #24 and #27
Multi Transfer Example

Site 16 to Site 26

1st transfer

2nd transfer

3rd transfer

4th transfer

GaN Wafer

SOI Wafer

Close-ups

The purple, yellow, and green highlighted regions above extend the full 40mm

Repeat for GaN Wafer sites #11, #17 and #22