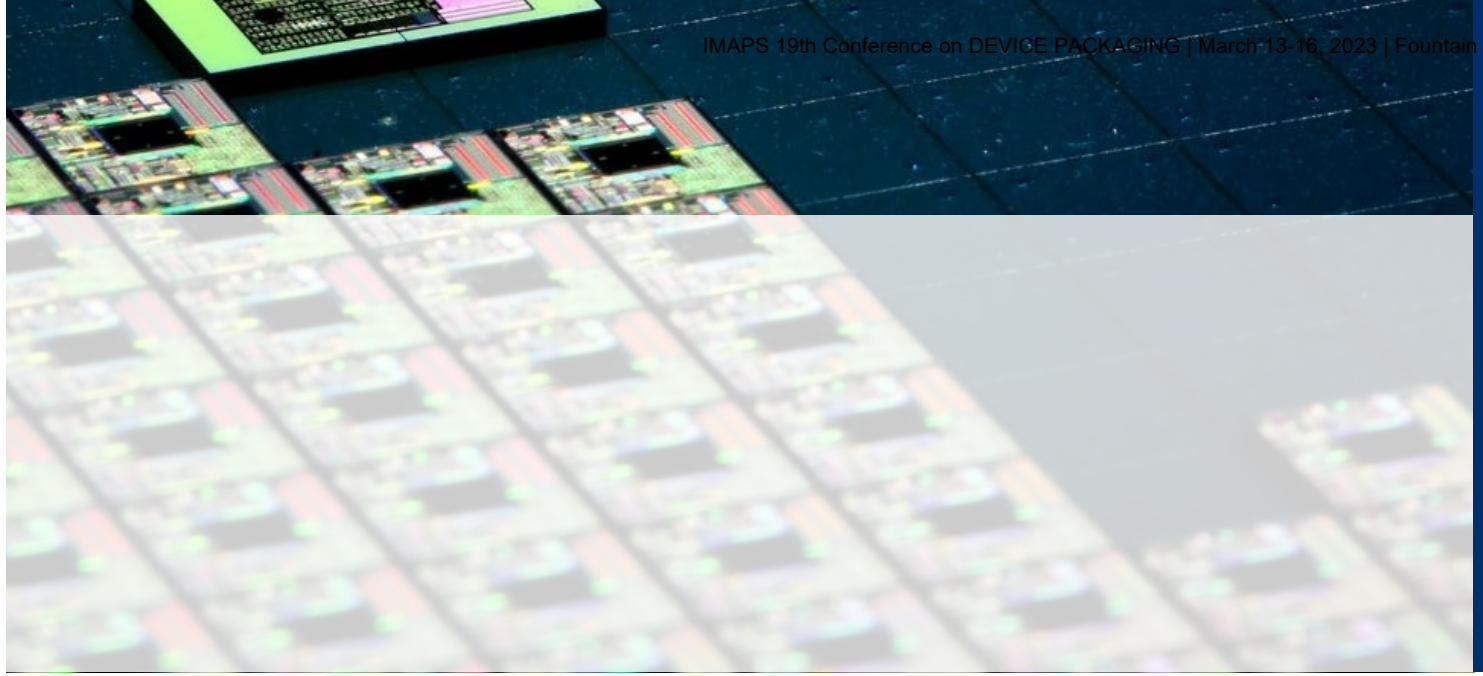

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ASSEMBLY SOLUTIONS FOR COST-EFFECTIVE HETEROGENEOUS INTEGRATION WITH DISPARATE DIE TYPES

GLENN FARRIS, VP CORPORATE STRATEGY, DEVELOPMENT, MARKETING

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BUILD. SMARTER.

ABOUT THE AUTHOR

Glenn Farris has enjoyed more than 30 years in the electronics industry, starting as a research engineer at NASA and transitioning to leading marketing organizations for multiple technology companies. He is experienced in advanced simulation technology, semiconductor test and measurement, enterprise hardware and software platforms, and nanoscale MEMS applications, and dealing with clients in consumer, automotive, medical, networking industries.

Glenn has a broad vision of market trends and deep understanding of technology challenges. He joined Universal in 2013 as Vice President, Marketing and has been instrumental in leading the company into developing strategic relationship with some of the world's largest technology leaders.

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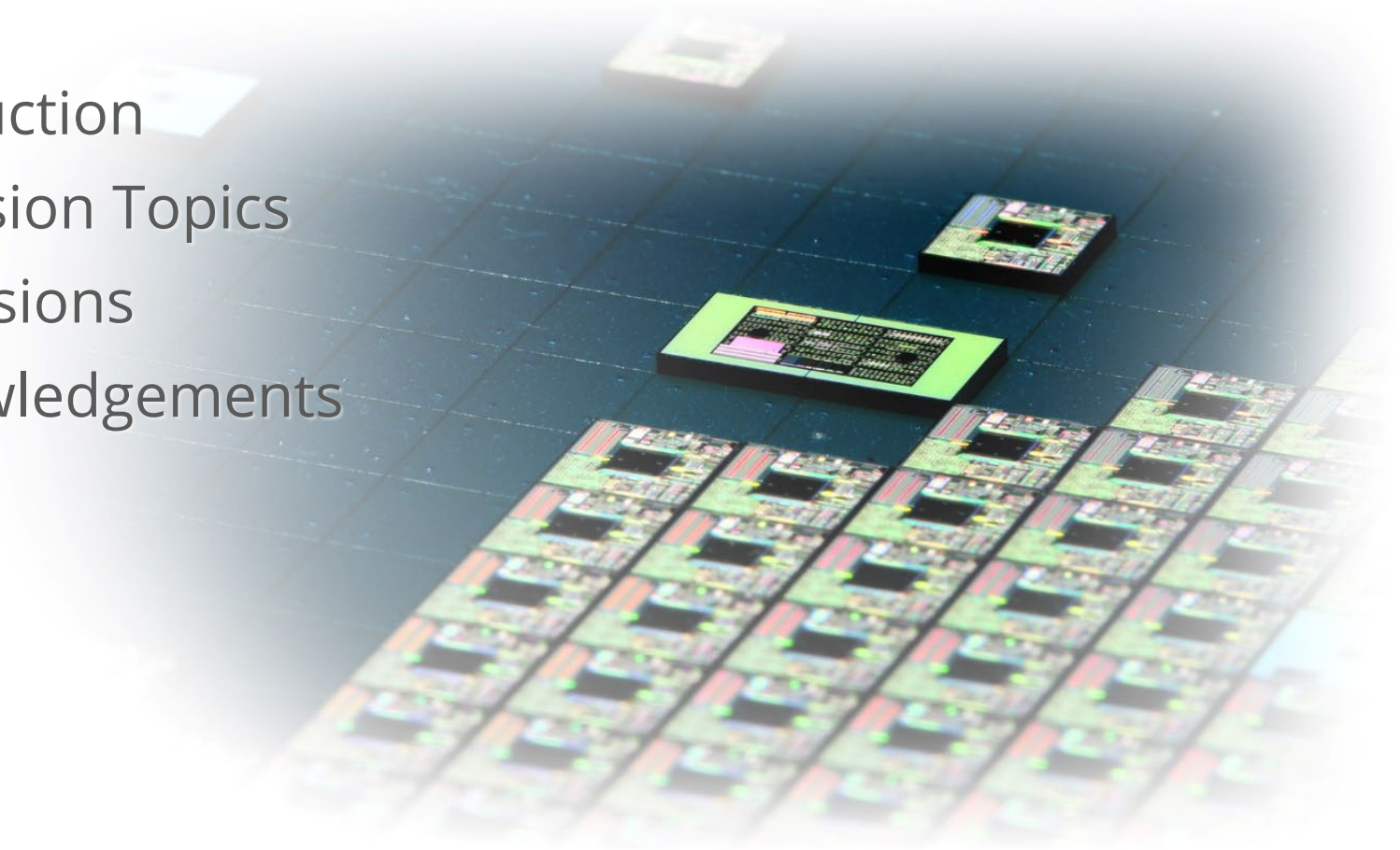
OUTLINE/AGENDA

- Introduction
- Discussion Topics
- Conclusions
- Acknowledgements
- Q & A



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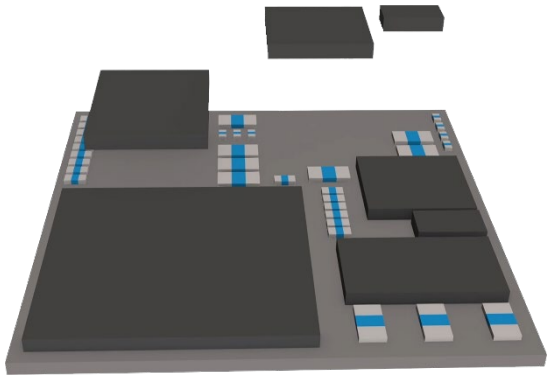
01. INTRODUCTION



The semiconductor industry is driving to enable high volume integration of disparate die types via Heterogeneous Integration. These die can come from a range of wafer sizes fabricated in different technology nodes. This emerging package type creates new challenges regarding assembly efficiency and yield. Traditionally, flip-chip assembly process flows have utilized a single placement tool for the placement of the single die type onto the target substrate. For applications with multiple die types, a series of placement tools have been configured in a production line, with each tool dedicated to the placement of a specific die type.

This paper and presentation explore the implications of this type of solution in the era of Heterogeneous Integration. Impacts on product yield, throughput, manufacturing efficiency, and overall cost of assembly will be explored for a broad range of Heterogeneous Integration die configurations. Based on a sensitivity analysis for the range of die types expected in these applications, a novel approach to optimization of overall assembly economics will be proposed. Appropriateness of this novel approach will be explored for a range of packaging solutions, including Flip Chip, 2.5D, 3D, and Fan-Out.

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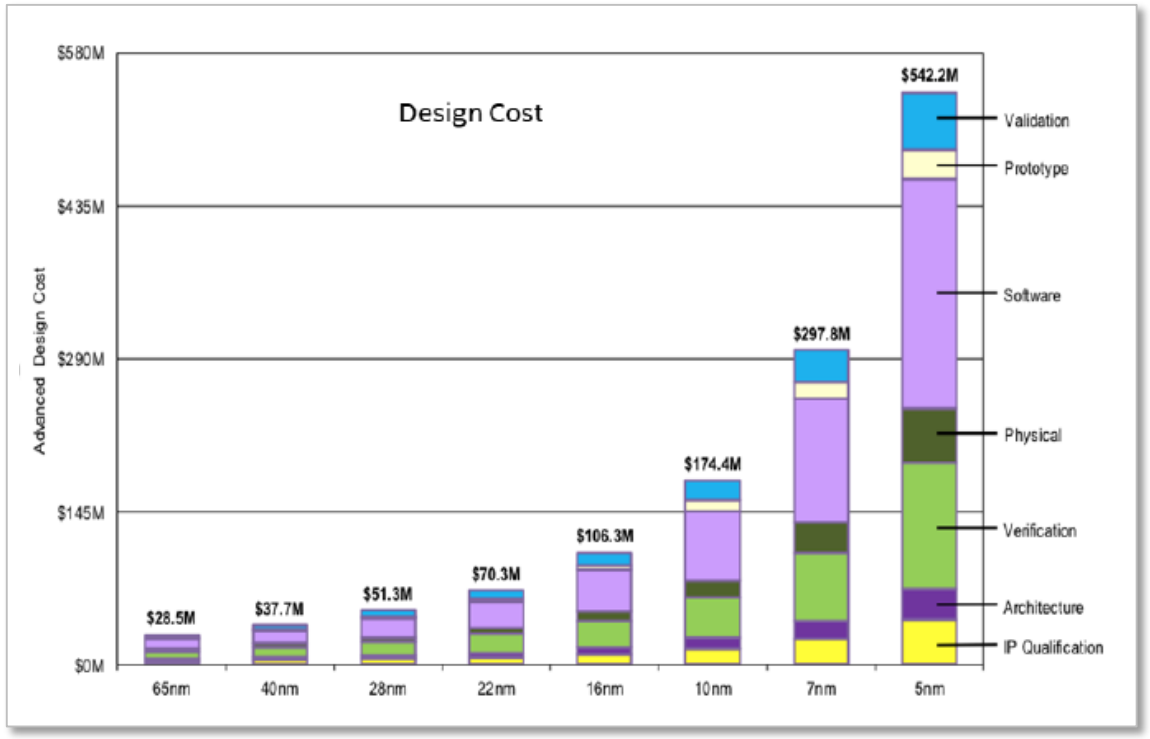
DIMINISHING RETURNS OF MOORE'S LAW

- While transistor scaling continues, the derived economic improvements have been diminishing

  Over the past decade at nodes below 22nm, the associated costs to design and introduce new products has increased by a factor of 7.75

- Heterogeneous Integration promises to lower cost by enabling integration of multiple proven silicon designs in a single package



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VALUE PROPOSITION OF "SINGLE CELL" ASSEMBLY SYSTEM

- Highest Yield
  - 4x lower cost of quality due to higher multi-die yield
- Efficient Heterogeneous Package Assembly
  - 35 - 85% higher throughput for multi-die applications due to efficient Cell utilization
- Lower Other Cost of Goods
  - 75% lower operator costs vs line of dedicated single die-type placement systems
  - 75% lower floor space vs line of dedicated single die-type placement systems
- Higher Factory Utilization
  - >20% utilization improvement vs dedicated lines for combo of unique die part numbers per package

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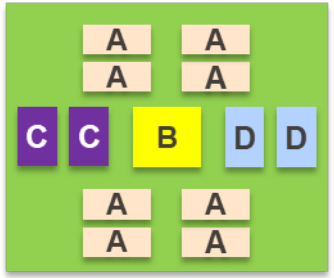
"SINGLE CELL" MULTI-DIE VS SINGLE DIE SYSTEM CONSIDERATIONS

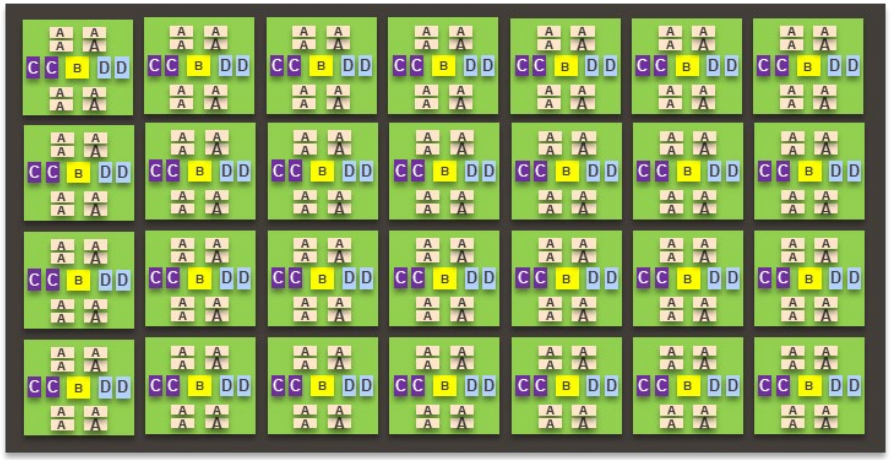
- Typical "HI" device has 3-4 die types
- Quantity per die type of 1 to 8
- Multi-die system enables single cell assembly
  - Flexible set up for any heterogeneous integrated package
  - Fewer operators, less floor space
- Single-die system requires custom line setup
  - Reduced yield due to compounded placement inaccuracy
  - Poor efficiency due to unbalanced line
  - Reduced OEE, increased facility costs

Typical "HI" device



4 unique part numbers
Quantity per p/n from 1 to 8

Typical "HI" device in JEDEC Tray



Note: Next-gen JEDEC tray is 2x width, 2x capacity

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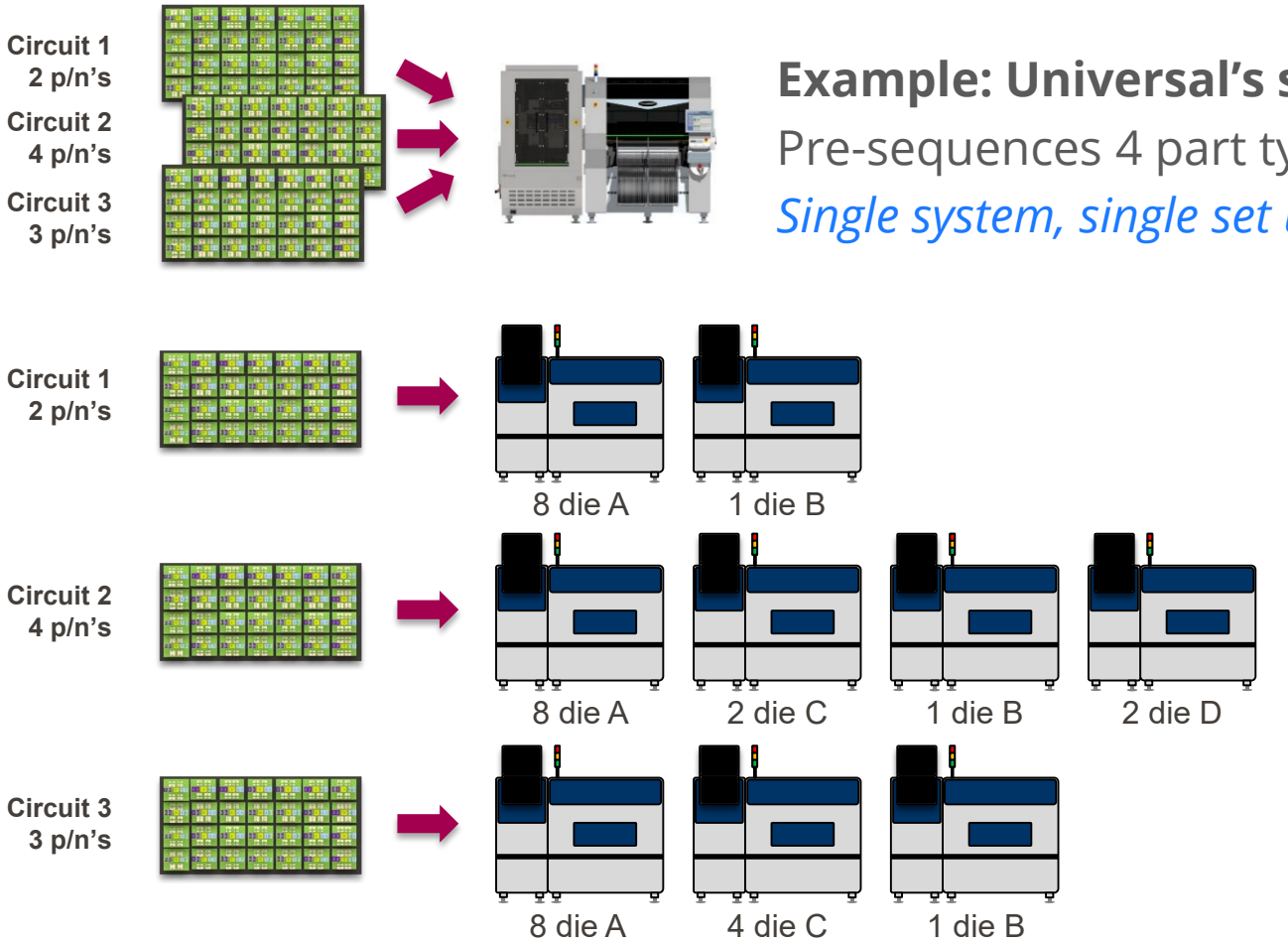
MULTI-DIE VS SINGLE DIE SYSTEM LINE IMPLICATIONS



Example: Universal's single Cell Solution – FuzionSC + HSWF

Pre-sequences 4 part types, with future capability to 8

Single system, single set up for any Heterogeneous Integration Device

Single Die Solution

One machine for each die

Multiple systems, multiple line configurations

- *Multi die solution places all 4 die types in a single cell, no line reconfiguration*
- *Single die solution requires varying line machine count to match varying p/n count*

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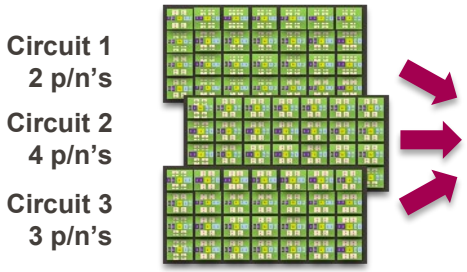
MULTI-DIE VS SINGLE DIE SYSTEM SYSTEM ECONOMICS



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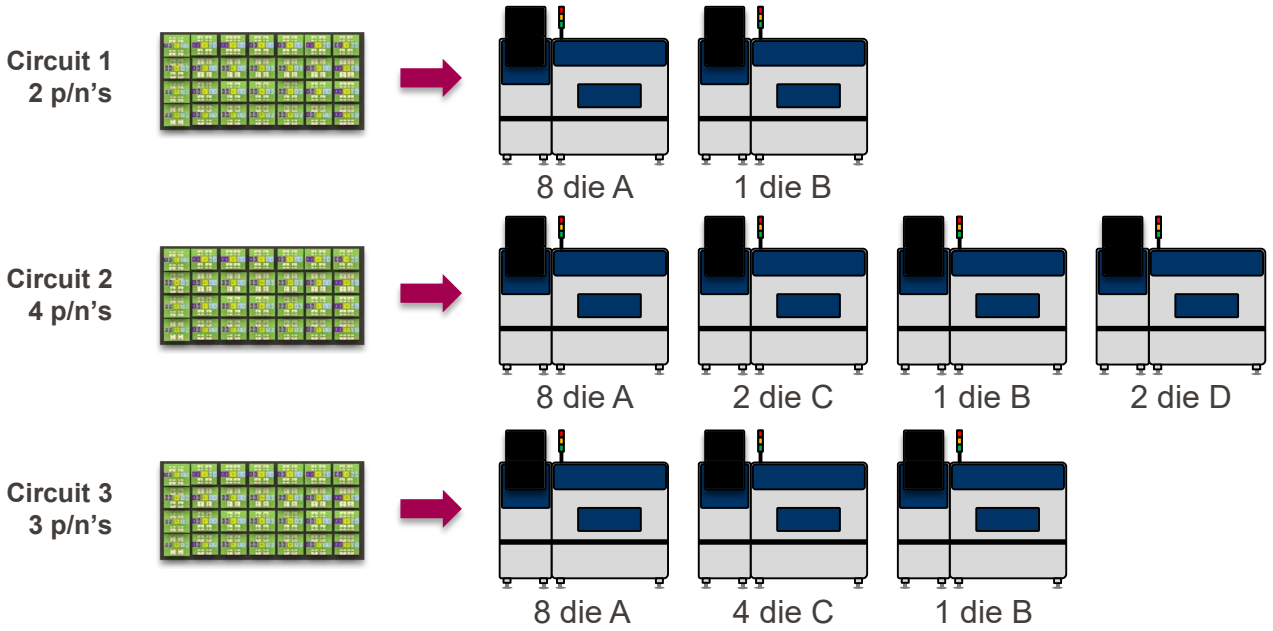

Economic Detractors

Low yield: Increased part handling & vision finds

Low throughput: Unbalanced line causes idle cells

High Operating Cost: More operators & floor space

Low OEE: Idle capacity from Line-Device mismatch

- *Multi die solution places all 4 die types in a single cell, no line reconfiguration*
- *Single die solution requires varying line machine count to match varying p/n count*

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THE IMPACT OF CARRIER SIZE

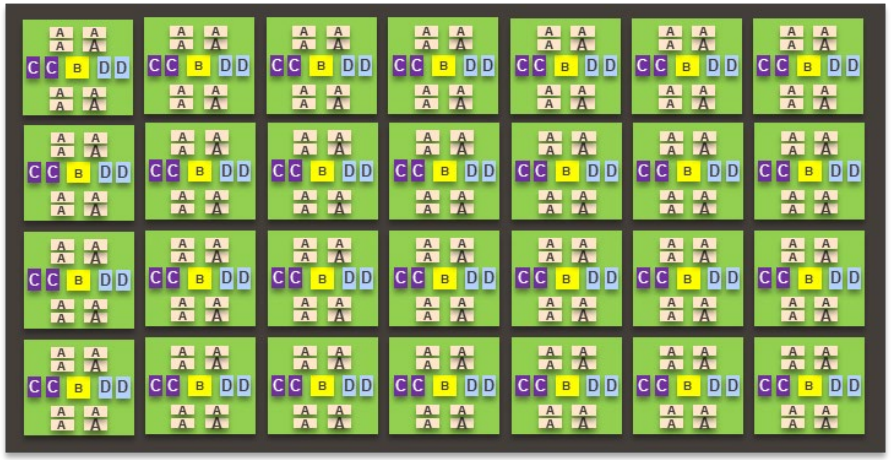
- Singulated organic substrates are typically presented to the “pick and place” assembly tool via a JEDEC standard tray (or Gen2 JEDEC tray in the future)
- At substrate dimensions up to 31 x 44mm, up to 28 circuit substrates can be loaded in one JEDEC tray
- Future Gen2 JEDEC trays can hold up 56 of these
- A substrate-less Wafer level fan-out carrier offers an assembly area for approximately 38 these
- A JEDEC standard panel fan-out carrier (600mm x 600mm) supports up to 247 of these

The number of circuits per carrier has a significant impact on the throughput of a single cell placement solution

31mm x 44mm circuit capacity by carrier type

Carrier Type	Circuits per Carrier
JEDEC Tray	28
Wafer Level Fan-Out Carrier	38
Gen2 JEDEC Tray (future)	56
Semi-Standard Panel	247

JEDEC Tray with 28 Substrates



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PLACEMENT YIELD IMPROVEMENT WITH SINGLE CELL SOLUTION

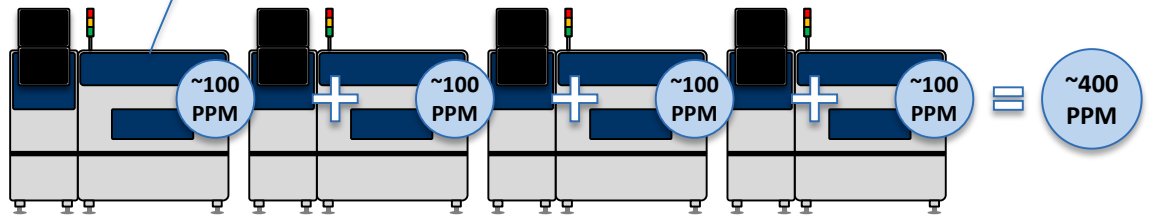
- 100ppm per place performance in a single cell
  - No substrate curvature or movement until all placements completed
  - Common vision find for all placements
  - Common spindle and gantry for all placements
- 400ppm per place performance across multiple cells
  - Substrate curvature & move after each die type placed: die movement on substrate
  - No common vision find reference: greater fid location variation
  - 4x increase in spindles and gantries: greater place variation
- For 4 die types with 17 total placements single cell delivers .51% higher yield

Multi-cell cost of quality is $338k / year for 3 shift operation @ $50 device cost

Single-Platform Solution
No PPM sacrificed for multi-die products

~100 PPM

ERROR SOURCES AT EACH PLATFORM (EACH ADDITIONAL DIE)
- Machine beams & spindles
- Vision/cameras
- Substrate bowing/flattening
- Substrate (lateral) movement



Multi-Platform Production
Error sources at each new die/platform degrades PPM

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THROUGHPUT IMPROVEMENT WITH SINGLE CELL SOLUTION

- "Multi die" Single Cell Benefits
  - Cell is fully utilized for placement at all times
  - Cartridge exchange time minimized as carrier size & number of placements per die type increases
- "Single die" Multiple Cells Detractors
  - Only one system is fully utilized and gates throughput
  - Multiple carrier transfers and vision finds

For 4 die types,13 placements on 32 substrates, single cell throughput is >60% higher

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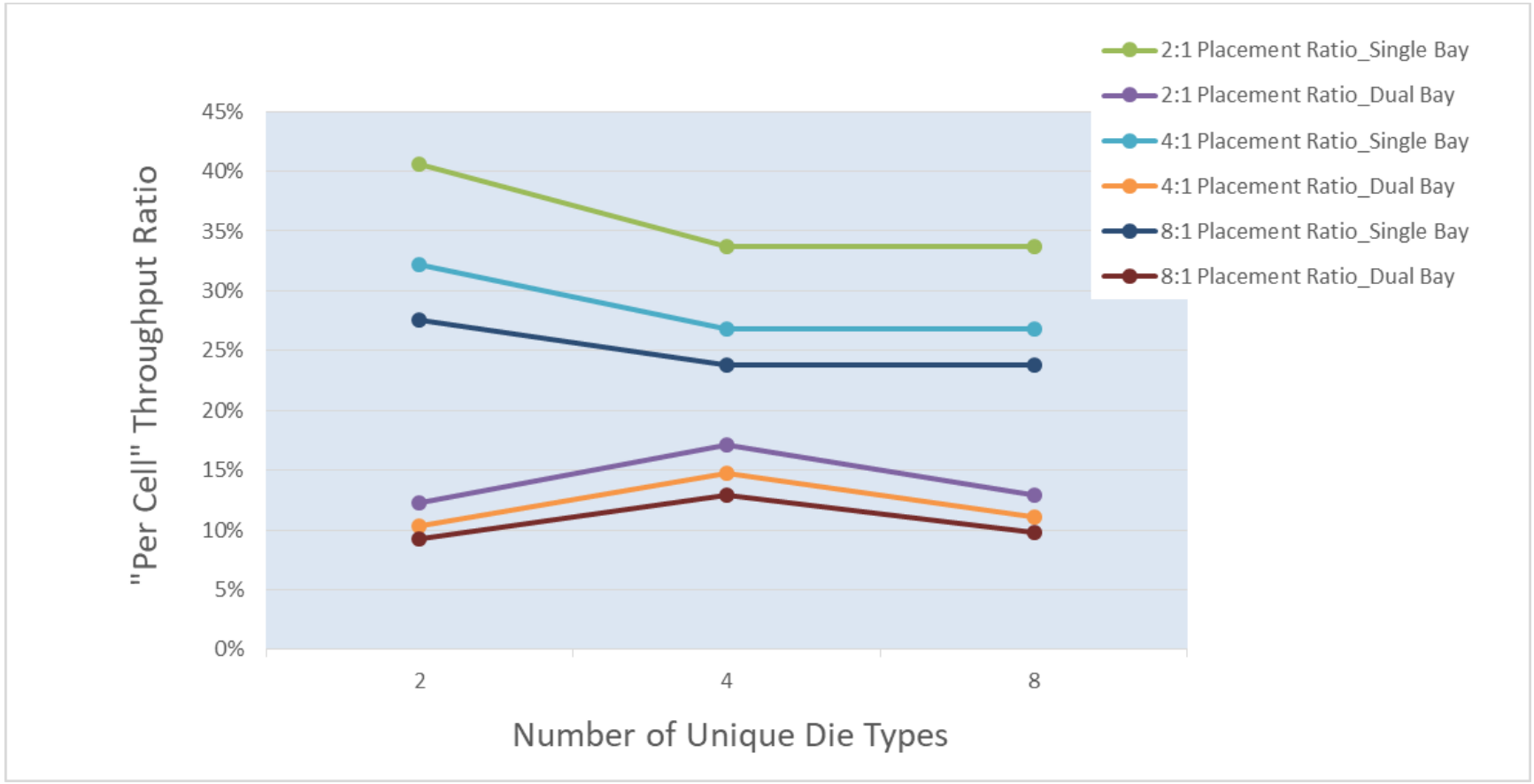
DEPRECIATION COST PER CIRCUIT



- *Multi-Cell platform price must be < 25% of a Single Wafer Table Single Cell Solution*
- *Multi-Cell platform price must be <10% of a Dual Wafer Table Single Cell Solution*

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THROUGHPUT IMPACT ON DEPRECIATION COST AT TYPICAL CAPEX

		Wafer Exchange Time, Single Wafer Table System (sec)									
		15	20	25	30	35	40	45	50	55	60
Circuits per Carrier	4	31%	37%	43%	49%	56%	61%	68%	74%	81%	88%
	8	22%	25%	28%	31%	35%	38%	41%	44%	47%	51%
	16	17%	19%	21%	22%	24%	25%	27%	29%	30%	32%
	32	15%	16%	17%	17%	18%	19%	20%	21%	22%	22%
	64	14%	15%	15%	15%	15%	16%	16%	17%	17%	17%
	128	14%	14%	14%	14%	14%	15%	15%	15%	15%	15%
	256	14%	14%	14%	14%	14%	14%	14%	14%	14%	14%
	512	13%	13%	14%	14%	14%	14%	14%	14%	14%	14%
	1024	13%	13%	13%	13%	13%	13%	13%	14%	14%	14%

Relative Throughput per Circuit: Single System Solution compared to System per Die Type Solution

		Wafer Exchange Time, Dual Wafer Table System (sec)									
		15	20	25	30	35	40	45	50	55	60
Circuits per Carrier	4	16%	19%	22%	25%	28%	31%	34%	37%	41%	43%
	8	11%	13%	15%	16%	18%	19%	21%	22%	24%	26%
	16	9%	10%	11%	11%	12%	13%	14%	15%	16%	16%
	32	8%	8%	9%	9%	10%	10%	10%	11%	11%	12%
	64	8%	8%	8%	8%	8%	8%	9%	9%	9%	9%
	128	8%	8%	8%	8%	8%	8%	8%	8%	8%	8%
	256	7%	8%	8%	8%	8%	8%	8%	8%	8%	8%
	512	7%	7%	7%	7%	7%	7%	8%	8%	8%	8%
	1024	7%	7%	7%	7%	7%	7%	7%	7%	7%	7%

Relative throughput per Circuit: Single System Solution compared to System per Die Type Solution

8 or more circuits per substrate or carrier enables 29-87% depreciation cost reduction

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OCOGS IMPROVEMENT WITH SINGLE CELL SOLUTION

- Single Cell Benefits
  - 1 operator can run complete Cell
  - 75% less floor space
- Multiple Cells Detractors
  - 4x operator count for a four die line, 8x operator count for an 8 die line
  - 4x factory overhead due to 4x floor space requirement

$760k lower Other COGS per year per line assuming $38/hr fully burdened factory rate

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OCOGS IMPROVEMENT WITH SINGLE CELL SOLUTION

- Single Cell Benefits
  - Cell is fully utilized independent of Heterogeneous Integration die configuration
- Multiple Cells Detractors
  - Need fixed lines for each possible combination of unique die part numbers per package
  - Monte Carlo factory simulation indicates up to 30% utilization drop per line across 4 lines

$90k lower OEE cost per year per line

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ECONOMIC MODEL SUMMARY (4 UNIQUE DIE SCENARIO)

	Single Cell Single Bay	Multi Cell Alternative	Comment
"Per Cell" Throughput efficiency	100%	24%	Throughput efficiency of single cell vs multi-cell
Circuits per Year	1273799	1214458	Input number of Assemblies / year
Solution Price	$1,000,000	$2,000,000	Input solution price to meet Assemblies/ year need
Depreciation Years	5	5	Input # of years to depreciate asset Note: a more flexible tool may justify longer depreciation cycle)
Base Depreciation per Unit	$0.157	$0.329	Calculation based on depreciation time interval
COGS of each Assembly	$50.00	$50.00	Input total COGS of all devices being picked and placed + substrate
Throw Rate %	0.13%	0.13%	Input expected device scrap (throw) rate due to mispick
Circuit Yield Loss	0.17%	0.68%	Input expected assembly yield due to misplacements
Total Scrap Cost per Unit produced	$0.150	$0.405	Calculated based on COGS and scrap %
Utilization	85%	60%	Input expected Solution Utilization
Utilization Cost per unit produced	$0.0236	$0.1334	Calculated based on increased depreciation per actual Unit assembled
Operators Required per Shift	1	4	Input # of Operators (1 per system)
Fully Burdened Cost/Oper	$30.00	$30.00	Input Operator Hourly Rate (Fully Burdened)
Operator Cost per Assembly	$0.1413	$0.5929	Calculated based on total operator cost
Floor Space Required	5	20	Input floor area (m2)
Annual Floor Space Cost (incl power, insurance, etc)	$10,000	$10,000	Input total cost per area
Factory Cost per Assembly	$0.0393	$0.1647	Calculated based on total floor space cost
Total Cost per Unit	$0.511	$1.625	
Total Cost if Alternative Solution is free	$0.511	$1.296	

Even if alternate solution is free, Single Cell solution is 60% lower cost per device

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Questions?

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Thank You!

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