Using M-Series with Adaptive Patterning to shrink PCB systems into System-In-Packages

Justin Locke (Siemens EDA)
Robin Davis (Deca Technologies)

SIEMENS

Presenter

Justin Locke
Senior Application Engineer
Siemens EDA - Advanced Packaging Team

Agenda

System in Package

- Definition & History
- Benefits

Adaptive Patterning

- Overview
- Benefits
- Implementation

M-Series

- Overview and benefits

SIEMENS

System in Package

Definition, history, benefits

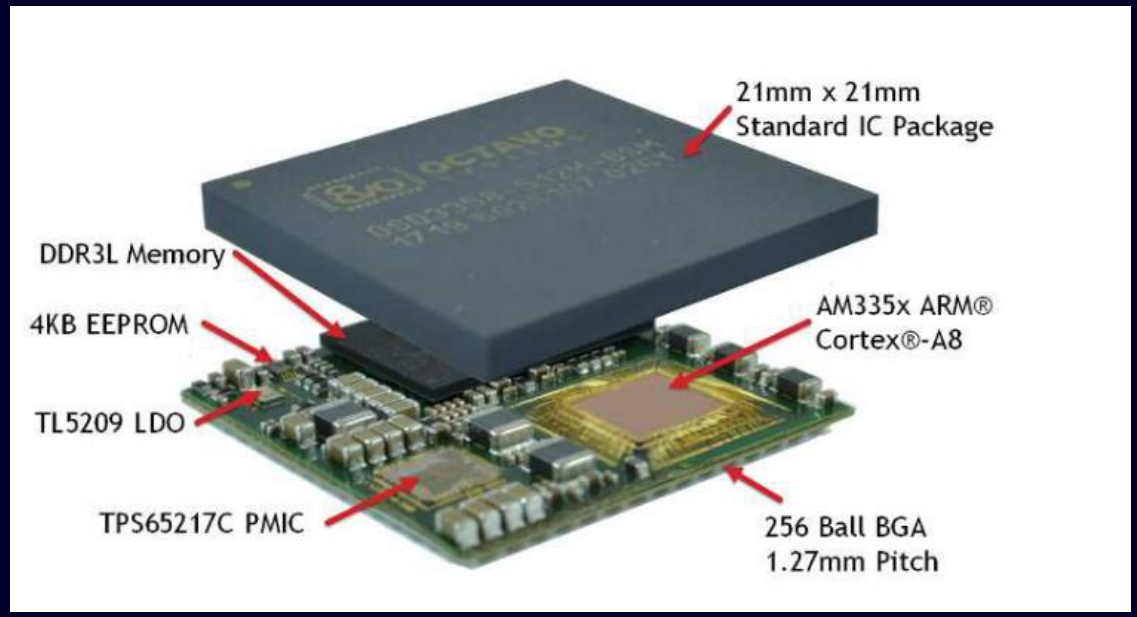
SIEMENS

System in Package – Definition and History

A System in Package (SiP) is a way of bundling multiple integrated circuits into a single package.

Supporting passives are included to create a complete system within a single package

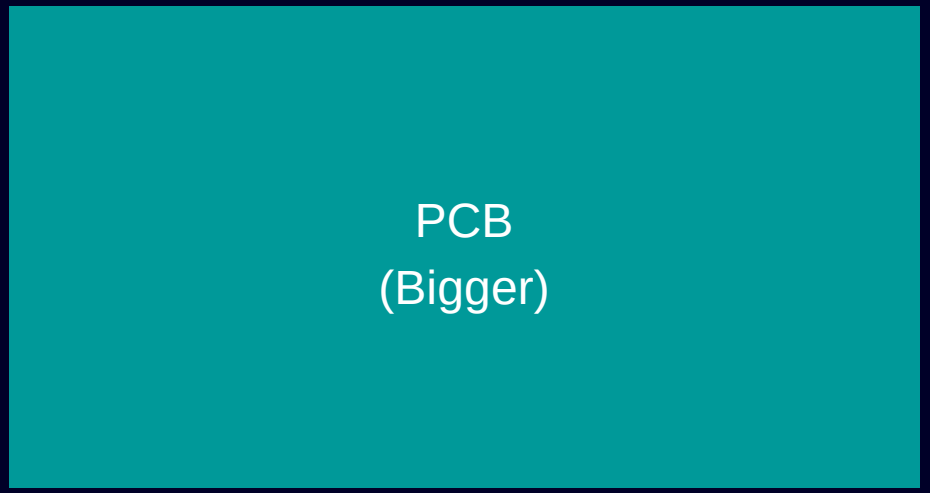
SiP's have been around since the 1980's in the form of Multi-Chip Modules, but the term SiP was first used in publications in 2000 [1]



SiP Benefits - Reduced Form Factor

SiP designs provide the opportunity to reduce the total design form factor

With improved die integration and reduced component spacings, SiP footprints can be reduced when compared to traditional printed circuit board system designs



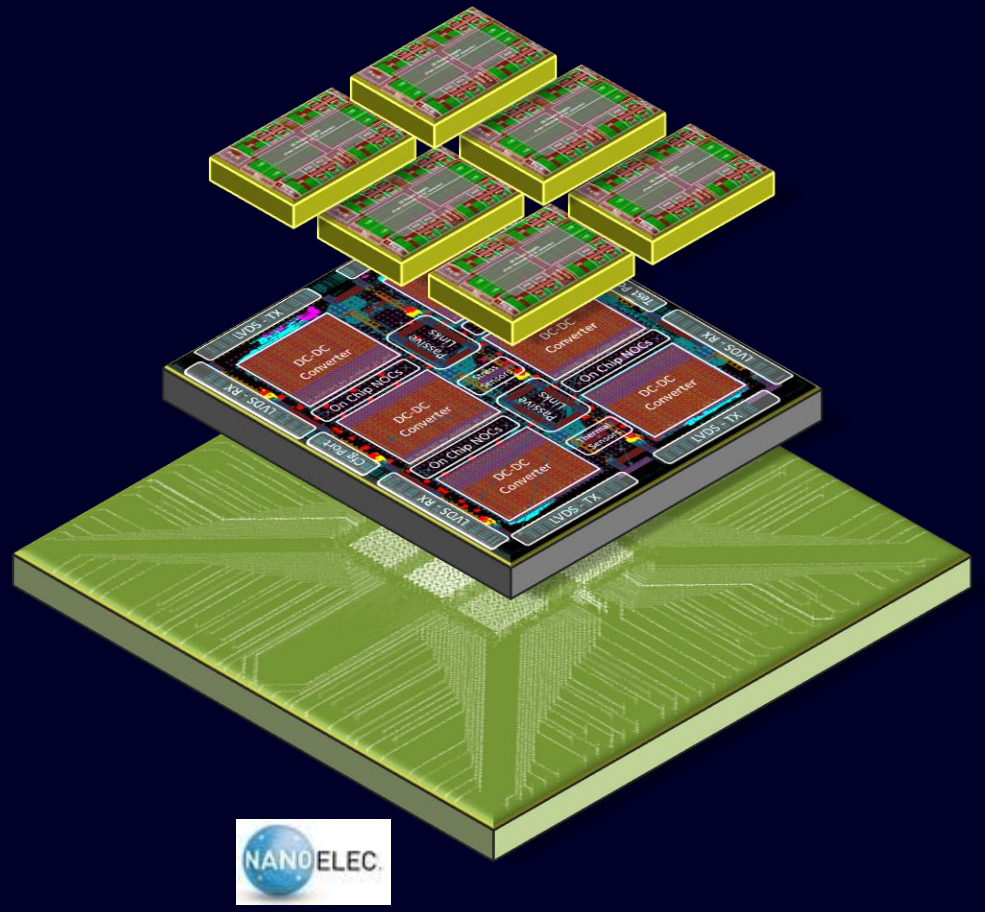
SIEMENS

SiP Benefits - Design Flexibility

One major benefit of SiP's over SoC's is the ability to use chips designed at different nodes

Analog IP, for example, may not be as easy to move to the next design node

Rather than design the entire SoC at a given node, each chip can be designed at the ideal node based on cost and density factors

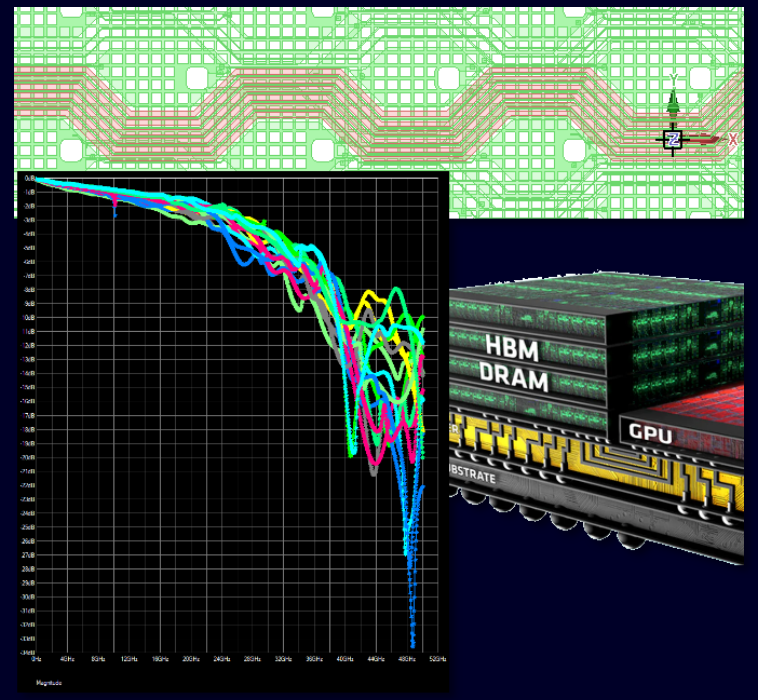


SIEMENS

SiP Benefits - Improved Signal & Power Integrity

By co-packaging chips in a SiP, the distance signals need to travel is reduced as compared to PCB interconnects

These shorter signal lengths result in greater signal speeds, while also reducing the power consumption requirements needed to drive the signals



SiP Interconnect (Shorter)

PCB Interconnect (Longer)

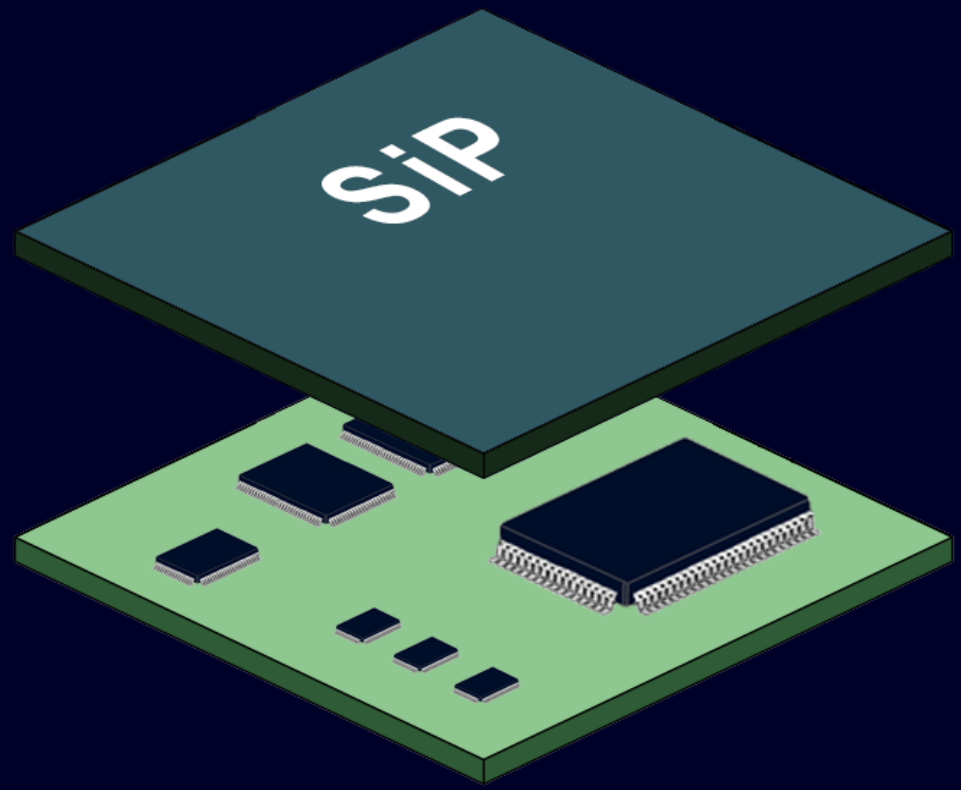
SiP Benefits - Reduced Customer Design Requirements

System in Package designs provide semiconductor companies with the opportunity to reduced the design requirements of their end-customers

Semiconductor companies will often provide a reference PCB design showing best practices for implementation of their given IC

However, the design rules and guidance of this reference PCB may not be properly implemented by the customer, resulting in less-than-ideal performance with the system-level PCB design

By integrating their chips into a SiP, semiconductor companies can ensure the system is properly designed, ensuring ideal performance of the entire system

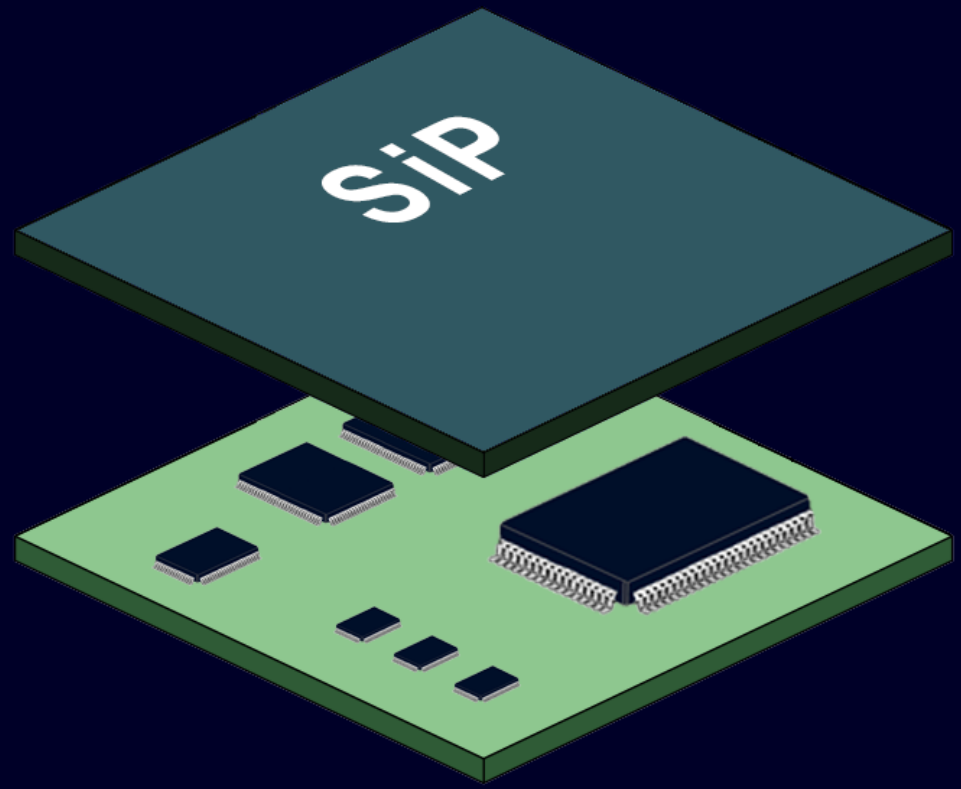


SIEMENS

Limitations to SiP Designs

Of course, there are drawbacks and limitations to SiP designs.

By leveraging Adaptive Patterning from Deca Technologies, many of these concerns can be mitigated.



SIEMENS

Adaptive Patterning®

Overview, benefits, implementation

SIEMENS

Adaptive Patterning Overview

Adaptive Patterning from Deca Technologies effortlessly accounts for die-shift in fan-out wafer-level (FOWLP) or panel-level (PLP) processes.

Adaptive Patterning is a methodology which adapts design artwork to align with measured die orientation misalignment in X, Y, and Theta directions

By combining a high-speed and accurate optical position inspection with a scalable computing cluster, **Adaptive Patterning generates a custom-made layout for each individual device that compensates for measured positional error**

Adaptive Patterning Overview

Deca's built-in real-time design rule checking (DRC) guarantees a successful result. After each pattern is generated, it is swiftly converted into digital exposure data for implementation with maskless photolithography equipment.

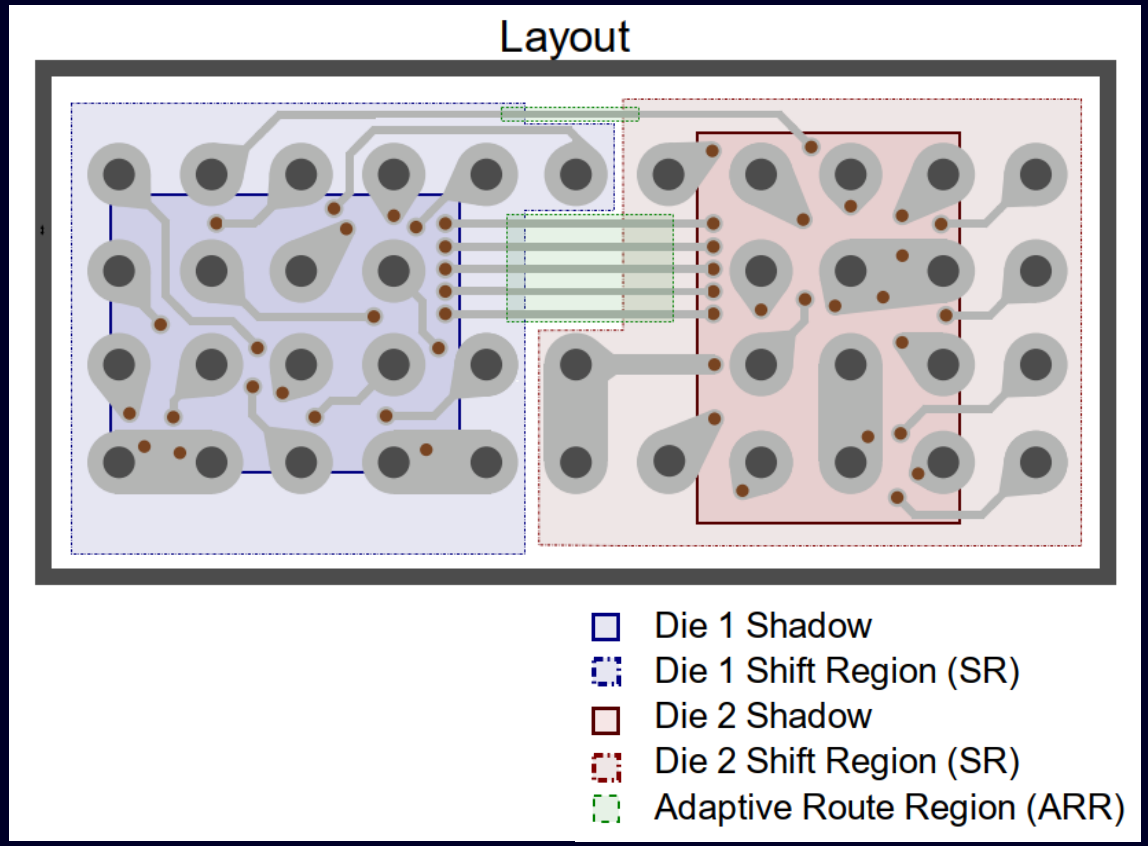
As a product moves through the manufacturing process, Adaptive Patterning customizes each lithographic layer on a device-by-device basis to ensure the highest possible yield

Adaptive Patterning Implementation

There are two primary features designers must include in their physical package definition.

Shift Region (SR): A polygon surrounding the design-features on one or more consecutive layers that shift together.

Adaptive Routing Region (ARR): A region in the design that will utilize Adaptive Routing. These areas bridge the connection between PRDL features within a shift region and other PRDL features that can either be in a fixed position or shifted with a different die in the design. These regions are defined by the designer.



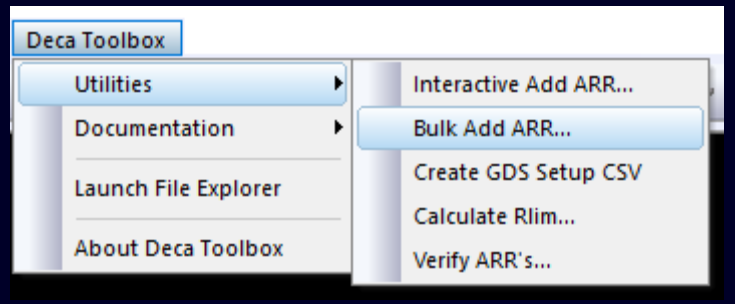
Adaptive Route Region Implementation

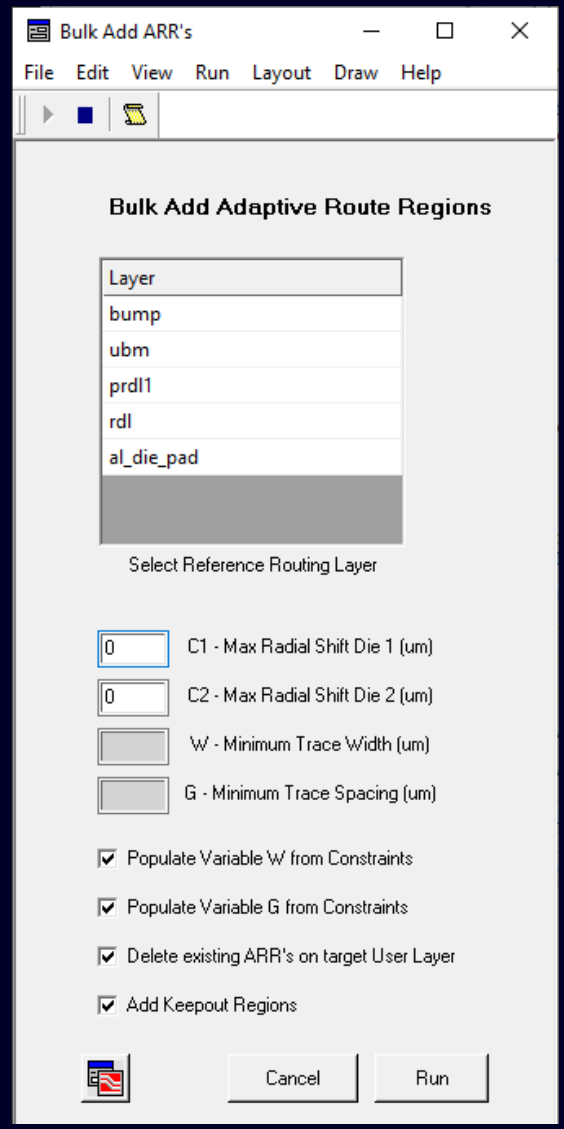
Number of routes in ARR	Max radial shift of DIE1, µm	Max radial shift of DIE2, µm	Min Trace width, µm	Min space between adaptively routed traces µm	Adaptive Route Region Length, µm	Adaptive Route Region Width, µm	Trace Group Width, µm
n	C1	C2	W	G	L	X	Y

ARR Widths and Lengths are a function of the equations below:

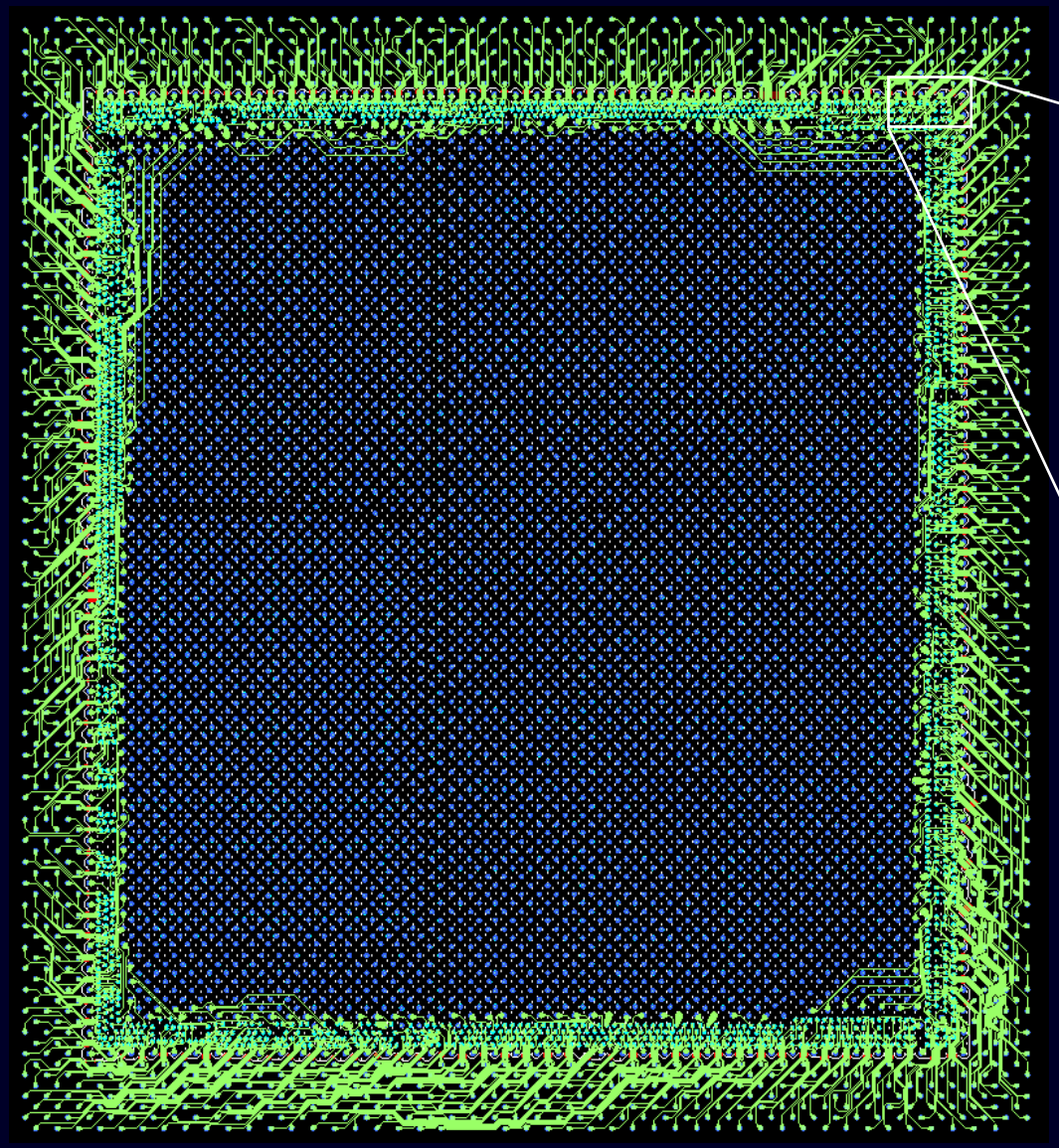
$$Length\ (L)\ \geq\ \sqrt{2(C1\ +\ C2)}+\ (n(W\ +\ G)-\ G)\ *\ \tan(22.5°)$$

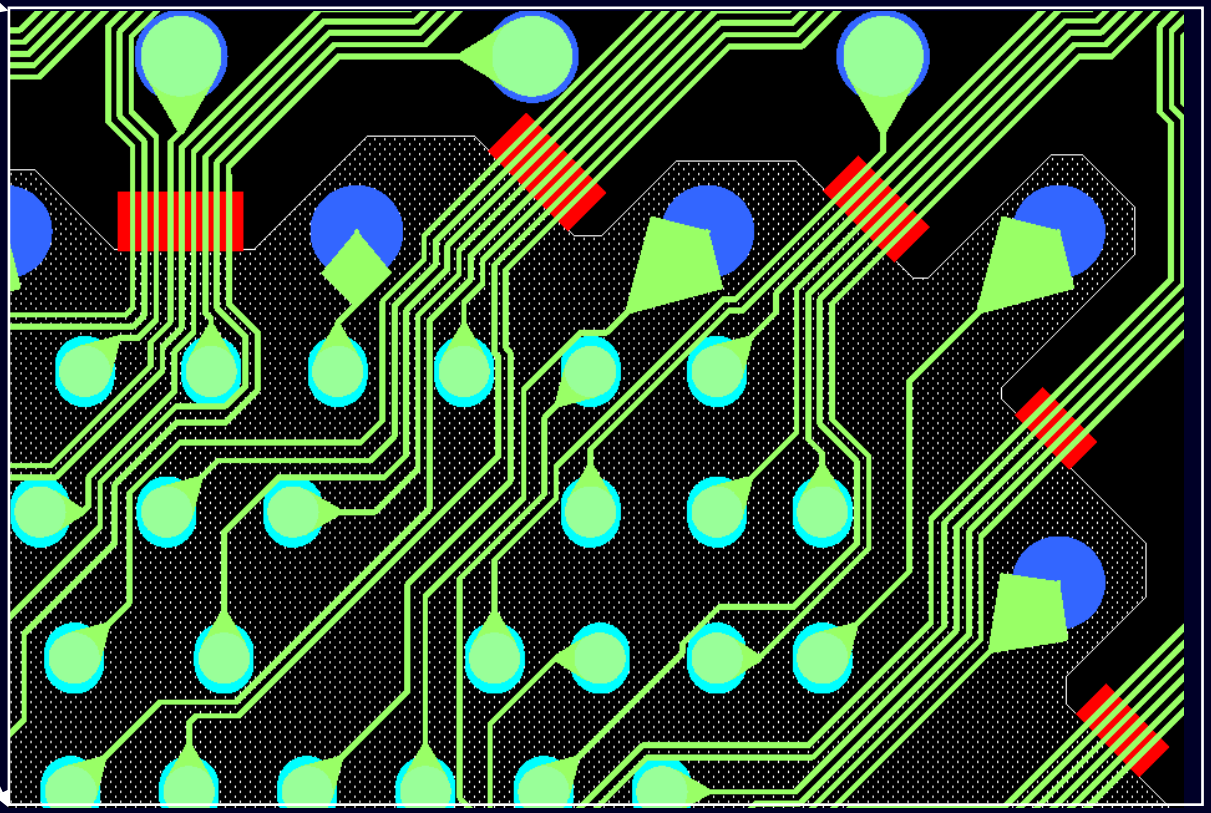
$$Width\ (X)\ \geq\ n\ \cdot\ (W\ +\ G)\ +\ 3G$$



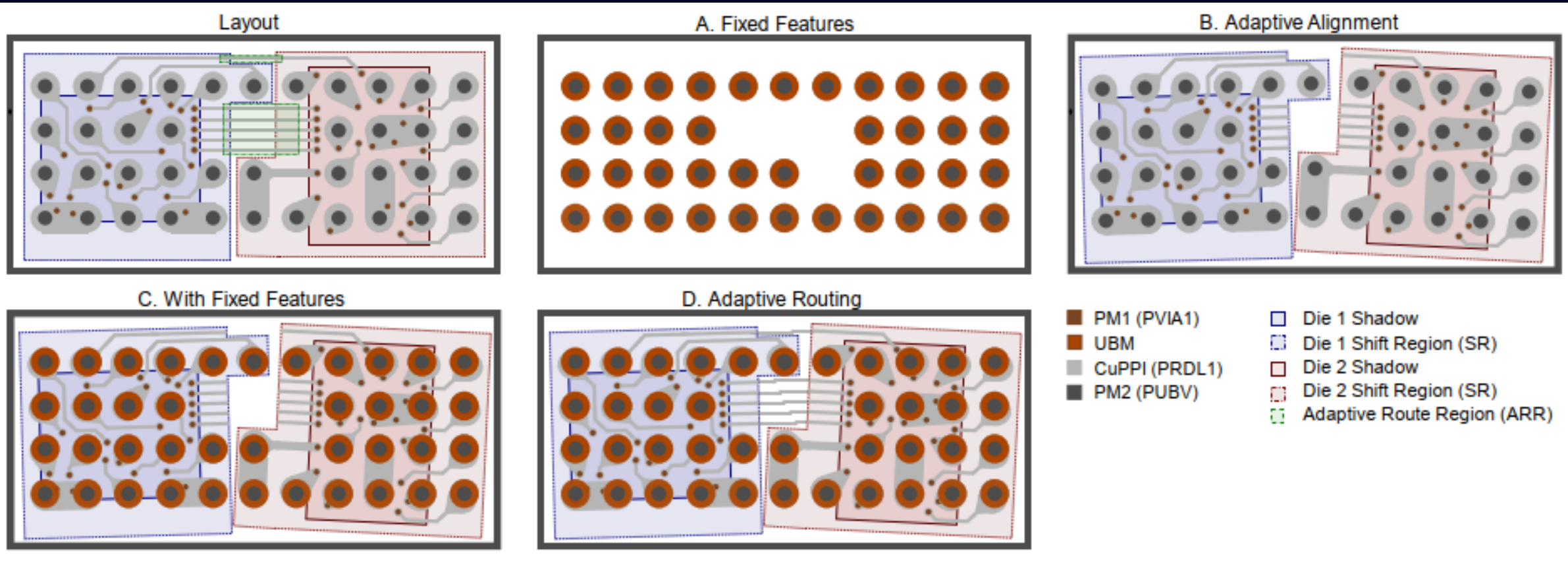


Adaptive Patterning Implementation





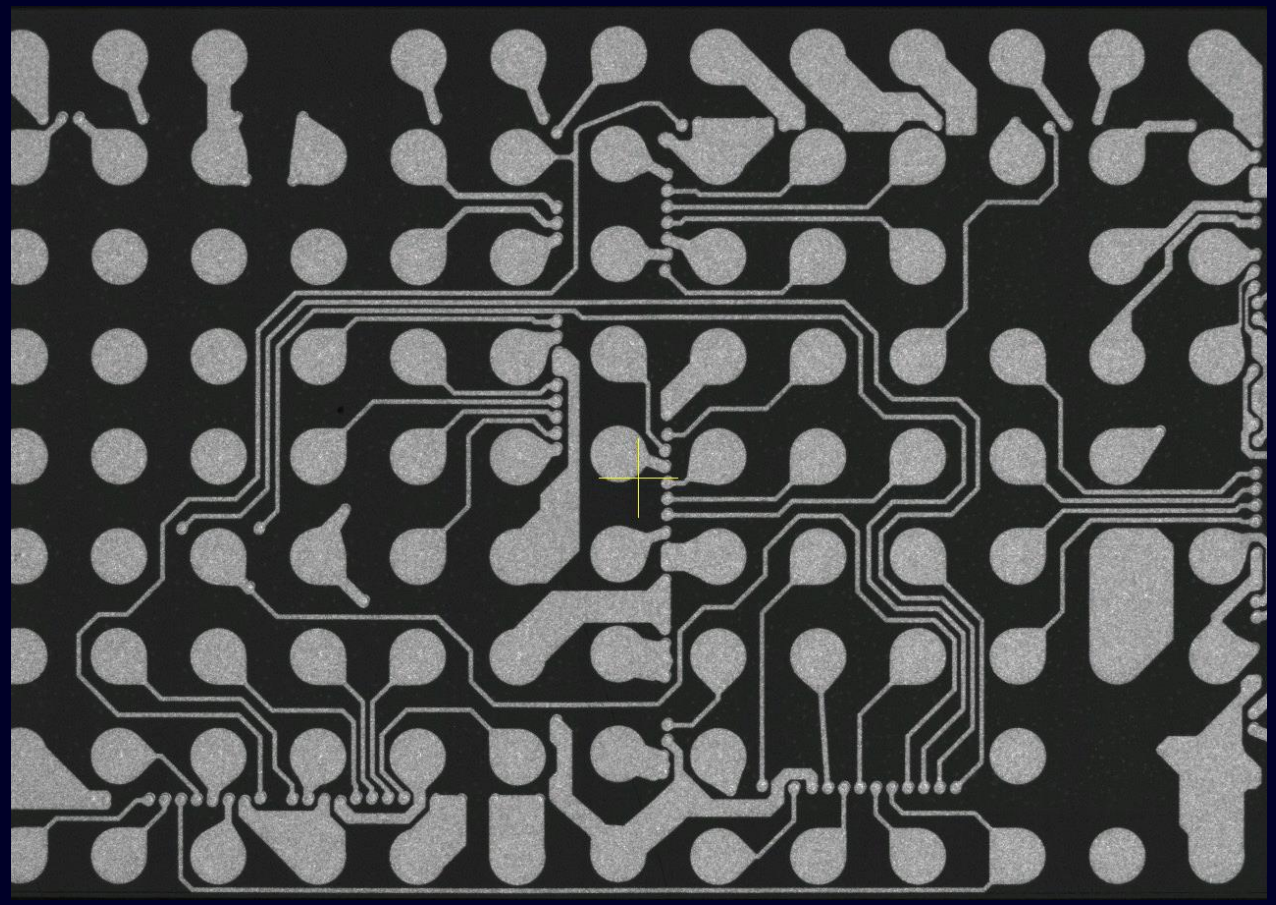
Adaptive Patterning Two-Die Example



Adaptive Patterning Benefits to Assembly Yield

Assembly yield is always a concern in package design. This is particularly true for FOWL-SiP designs where many die are used

The Adaptive Routing system combines perfect alignment with real-time dynamic auto-routing to meet the challenges of combining up to nine die in a SiP with tens of thousands of high-frequency connections



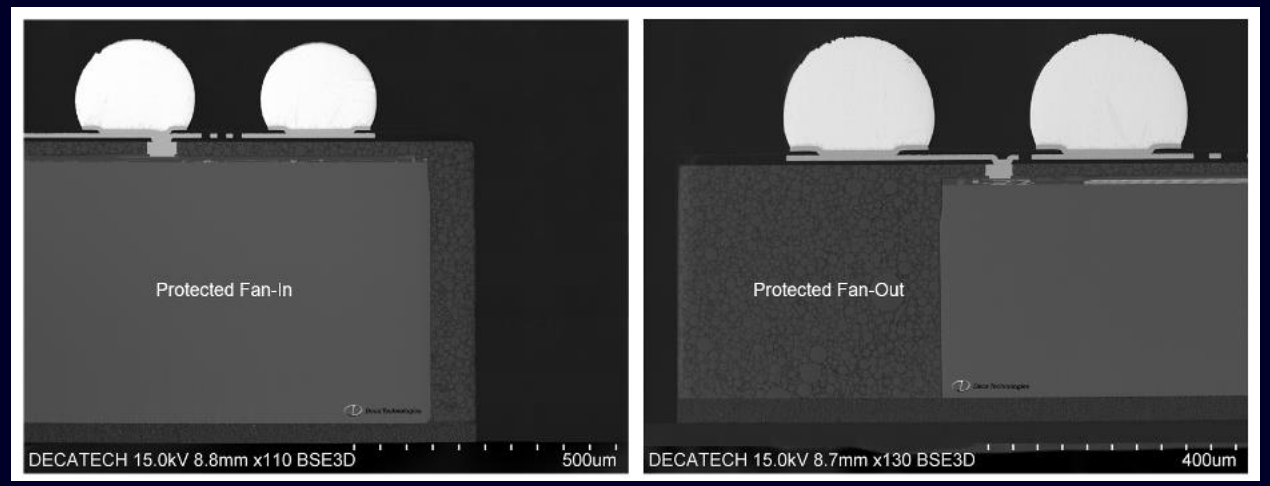
M-Series™

Overview and benefits

SIEMENS

Deca's M-Series

A fan-out or fan-in wafer level package wherein the chips are encapsulated within a mold compound surrounding five (5) sides of each chip including the active surface and having Cu bumps that extend from the active surface through the mold compound to enable electrical connection between the active surface of the chip and a fan-out redistribution structure.



SIEMENS

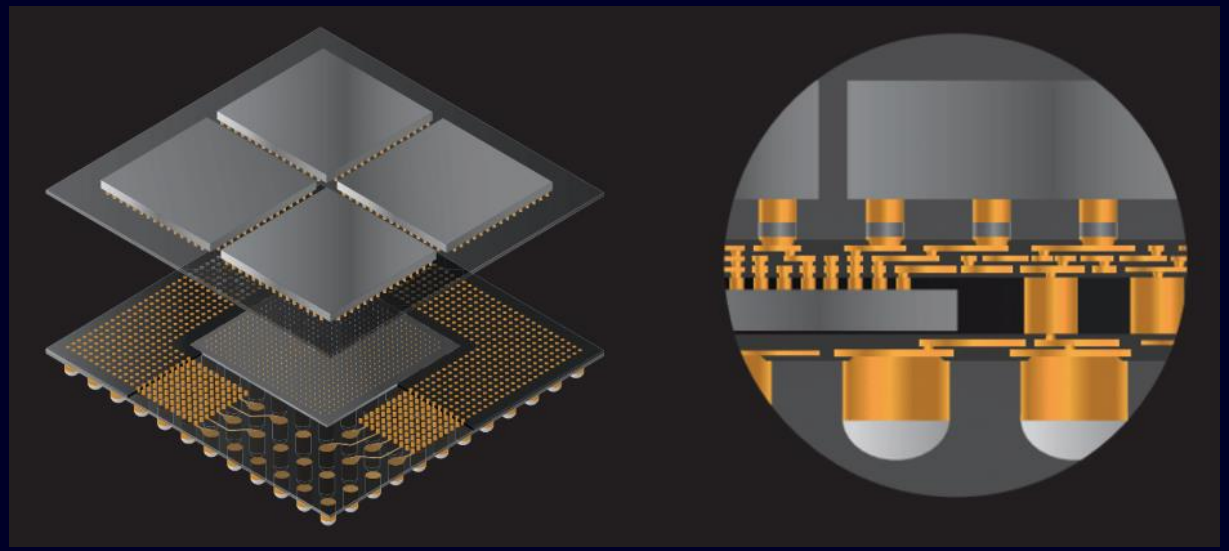
Benefits to M-Series with Adaptive Patterning

Improved yield

Minimize signal lengths

Reduce crosstalk

Minimize joules-per-bit in high-speed designs



2.5 billion units
powering leading smartphones

100% improvement
in board reliability

99.9% yield
in high volume production

Summary

Migrating PCB System to System-in-Package designs offers numerous benefits. Using M-Series with Adaptive Patterning amplifies the benefits of this design migration.

- Reduced form factor
- Closer proximity of die
- Improved signal and power integrity
- Increased design density
- Reduced customer-design requirements
- Improved assembly yield

Contact

Published by Siemens EDA

Justin Locke
Senior Application Engineer
IC Packaging
8005 Boeckman Road
Wilsonville, OR 97223

Phone +1 503 367 4638

E-mail justin.locke@siemens.com

[1] W. W. -M. Dai, "Historical Perspective of System in Package (SiP)," in IEEE Circuits and Systems Magazine, vol. 16, no. 2, pp. 50-61, Secondquarter 2016, doi: 10.1109/MCAS.2016.2549949.

Disclaimer

OPTIONAL

Subject to changes and errors. The information given in this document only contains general descriptions and/or performance features which may not always specifically reflect those described, or which may undergo modification in the course of further development of the products. The requested performance features are binding only when they are expressly agreed upon in the concluded contract.

All product designations may be trademarks or other rights of Siemens AG, its affiliated companies or other companies whose use by third parties for their own purposes could violate the rights of the respective owner.

SIEMENS