American Semiconductor®
Reliably Thin Electronics

Thin and Ultra-thin sidewall protected P-WLCSP

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Advanced Packaging

- Defining “Advanced Packaging” (AP)
  - Advanced packaging is the aggregation and interconnection of components before traditional integrated circuit packaging – Wikipedia
  - Advanced packaging is a general grouping of a variety of distinct techniques, including 2.5D, 3D-IC, fan-out wafer-level packaging and system-in-package – Semiengineering
  - These definitions fail in defining “advanced packaging” as it relates to package manufacturing

- FEOL Example: Next Generation multi-core SOC vs Next Advanced Process Node
  - Scaling from 28nm to 5nm is an example of advanced manufacturing
  - Designing improved multi-core ICs is not, but may be realized in an advanced manufacturing process
  - Advanced manufacturing is not limited by new designs and can provide improvements independent of product designs

- Advanced Packaging is correctly defined as: The leading edge of packaging technology
  - AP can be applied to benefit old and new technology nodes, designs, chiplets, passives, etc.
  - AP is not limited to advanced technology nodes, multi-chip assemblies, AI, 6G, etc.

Advanced Packaging

Advanced Packaging is fundamental to reestablishing U.S. semiconductor manufacturing

- Applying advanced packaging capability to WLCSP for FI is one example
- Die sidewall protection has become important for high IO die reliability
- Advanced Packaging in the form of non-WL CSP FO processes such as M-Series and eWLB have been applied to provide side protection (6S) for FI
- Non-WL CSP includes die reconstitution, expensive tapes, molding operations, and resolves the reliability issues for FI, but the added cost and process complexity was and is far from optimal
- Advance Packaging for P-WLCSP can resolve the issues associated with using FO processing to achieve FI reliability AND enable commercial on-shore packaging by providing cost advantages

6-side protection: P-WLCSP

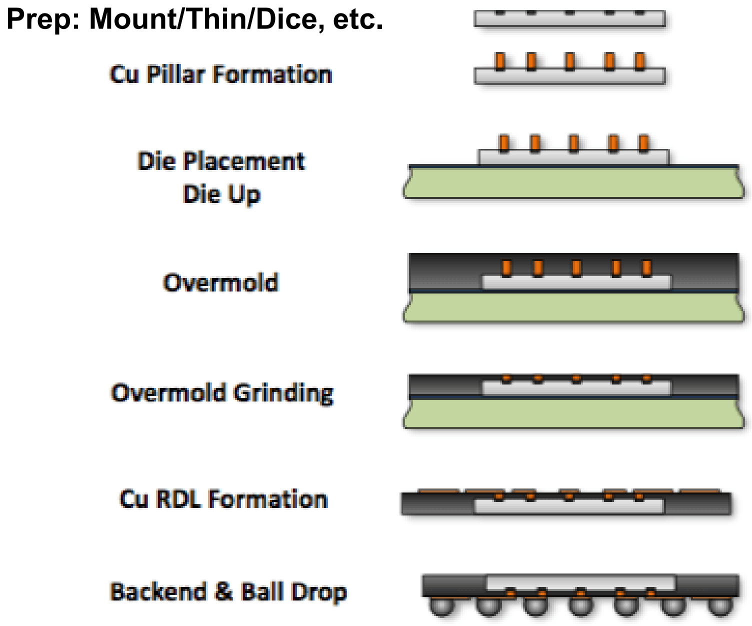
- “Protected WLCSP” (P-WLCSP) resolves Cost and Complexity of non-WL for FI
  - 6-side protection without the cost and complexity on non-WL FO type processes
  - P-WLCSP does not require pre-package die thinning, dicing or reconstitution
  - P-WLCSP Substantially reduce the equipment and process steps required for processing
  - Material reductions with the elimination of dicing tape and molding materials
- Example: SoP-TM™ 6-side protected P-WLCSP introduced at IMAPS 2021
  - Full protection, without the cost/complexity of non-WL FO processes used for protected CSP FI
  - 300mm process utilizes polyimide for encasement
  - The process includes maskless processing and high temperature temporary bonding
  - Adaptive processing expands the selection of PIs available for stress balancing
  - Final singulation (dicing) speed enhancement due to P-WLCSP PI scribe streets
- Enabling ultra-thin devices
  - Reduced die thickness improves capability for through silicon via (TSV) size and pitch
  - Enables high-temperature backside RDL (B-RDL) and heat sinks
  - CMOS silicon thicknesses is typically 10-15um, but can be adjusted as needed

SoP-TM vs non-WL CSP

another example

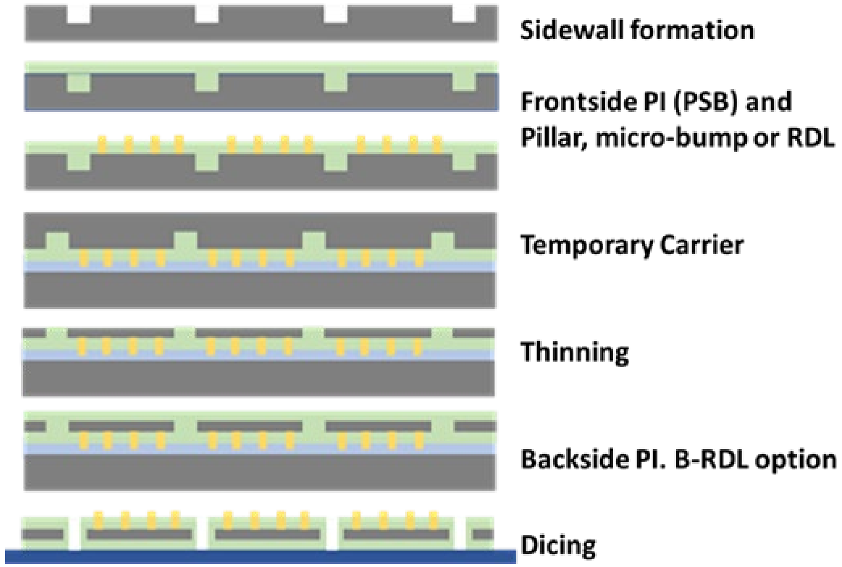
- Non-WL CSP vs P-WLCSP SoP illustrates advanced packaging benefits for FI

Die Up - M-Series



M-Series CSP FO Process. Source: SemicondcutorEngineering Feb. 2018

P-WLCSP – SoP-TM



FleX-TM Protected WLCSP, U.S. Patent 9,082,881

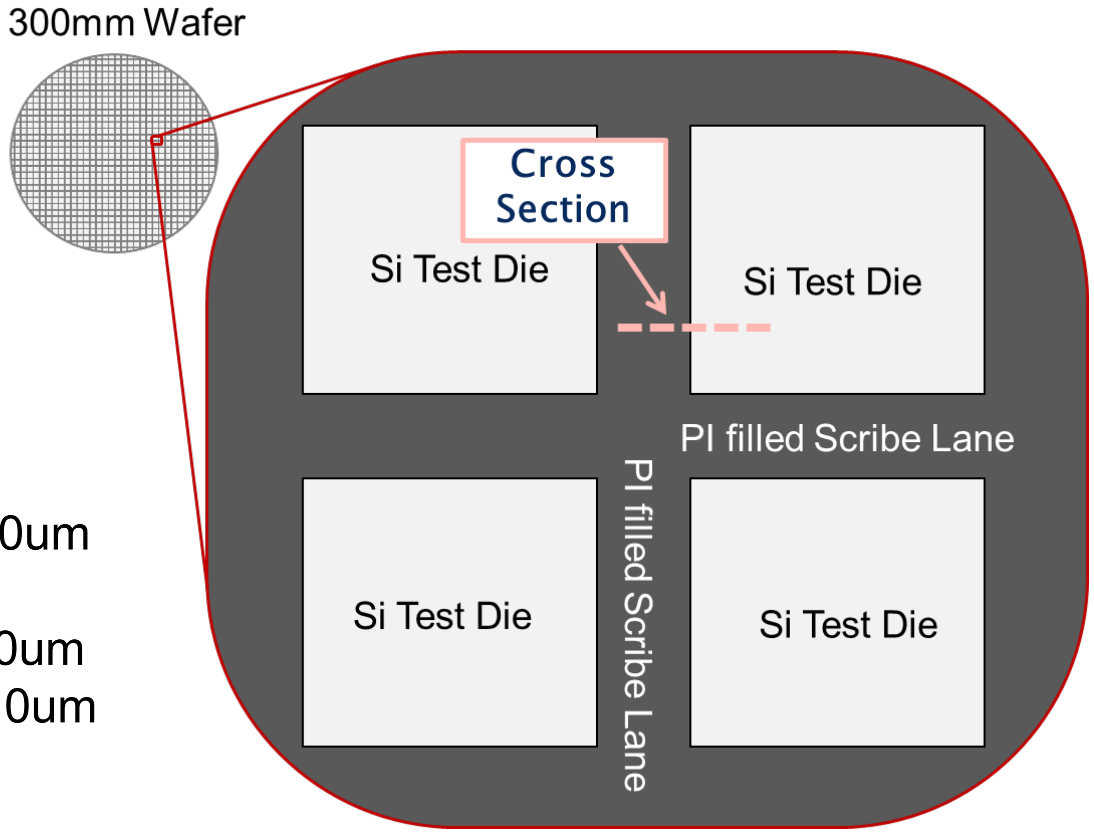
- P-WLCSP provides cost reduction and performance improvement in CSP FI applications
- **50% fewer steps –> 50% less capital, or 2X capacity increased for existing facilities**
- **50% Less labor cost –> Cycletime 50% less, improves cash flow**
- **30-50% Less material cost**

SoP-TM – Enables On-Shore Manufacturing

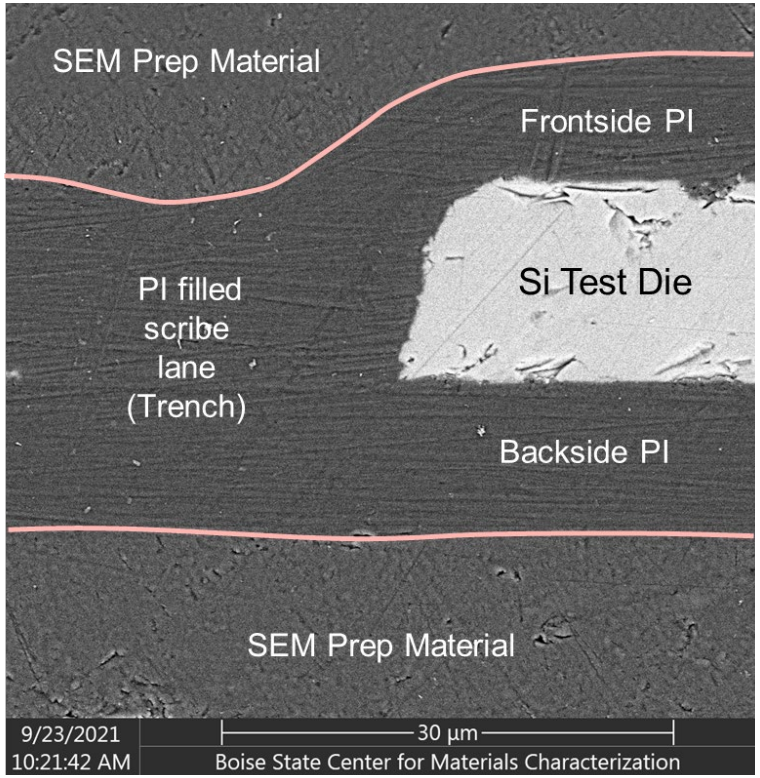
2021 SoP-TM 6-side P-WLCSP Initial Work

IMAPS 2021 - 1st Silicon Results announced

SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection utilizes polyimide for encasement. The process includes maskless processing, high temperature temporary bonding, final singulation with extremely fast laser dicing



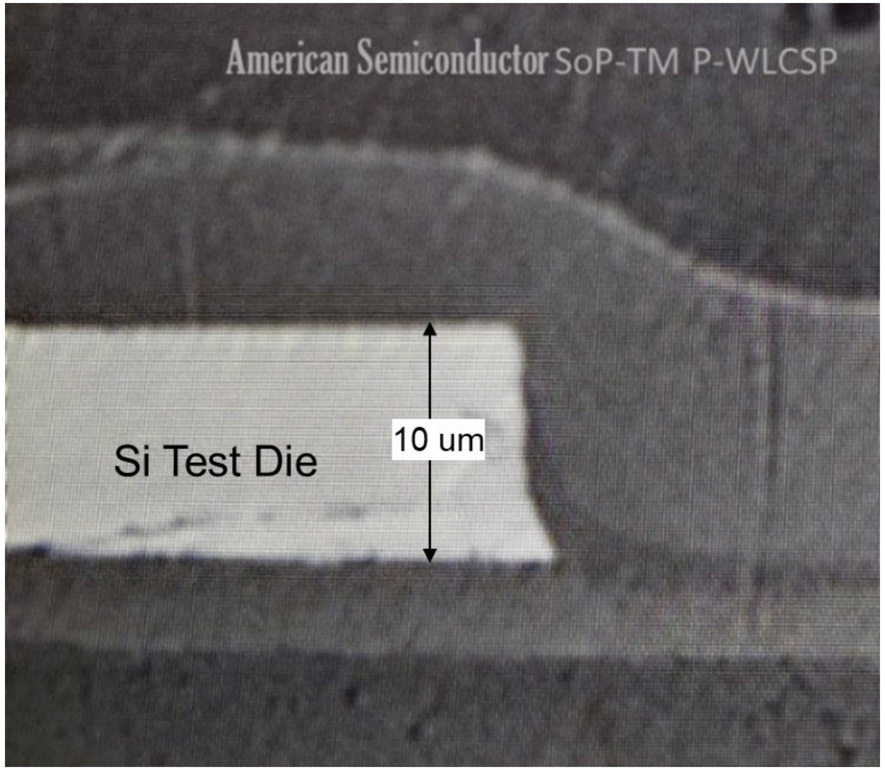
Trench 45um
Frontside PI 10um
Silicon 11um
Backside PI 10um
Sidewall PI ~10um

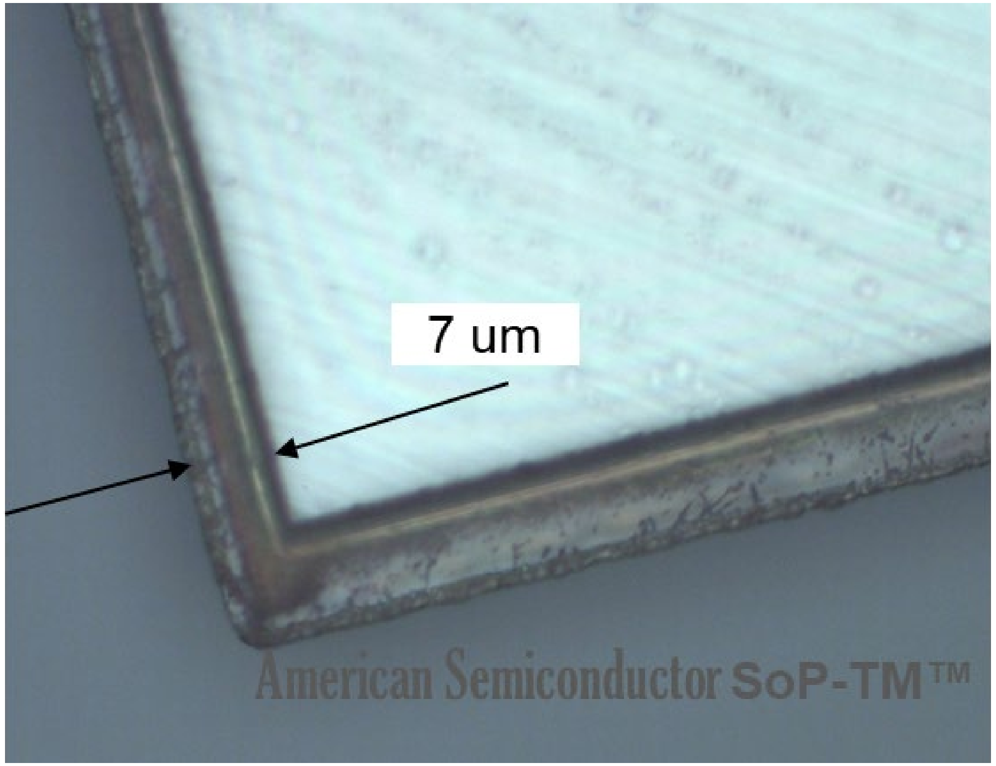


2022 SoP-TM Sidewall Demonstration

DPC2022 - SoP-TM development update

Current progress for SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection
Improved sidewall formation and demonstration of laser singulation





Trench 45um
Top PI (PSB) 10um
Silicon 10um
Bottom PI (PSB) 4um
Sidewall PI (PSB) ~7um

2022 SoP-TM Laser Patterning and Dicing

Adaptive Processing

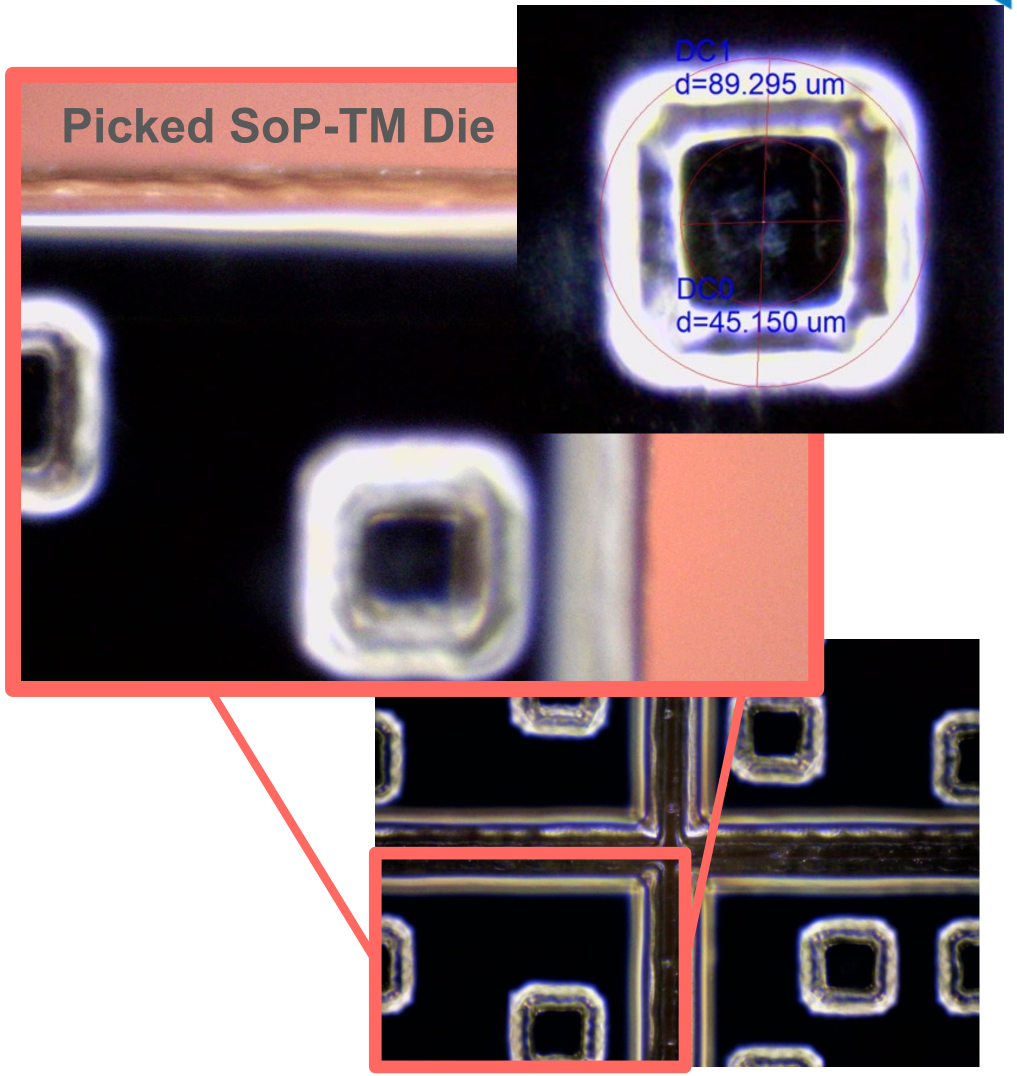
- Adaptive processing with direct write
- Maskless processing during RDL steps such as for via.

High Speed SoP Dicing

- Multi-pass recipe proves 200 mm/s effective cut speed
- Low power of 1.25 Watts.
- SoP polyimide encasement cuts cleanly without scorching
- Smooth cut line without need of protective coatings/cleans

Throughput (pre-production tool)

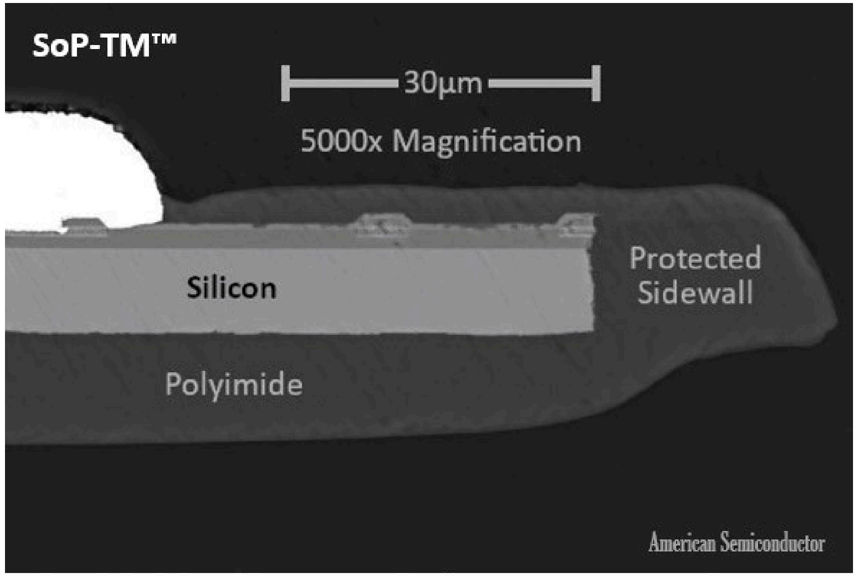
- Demonstrated at 4-5 WPH for 2 mm die on a 200 mm wafer.



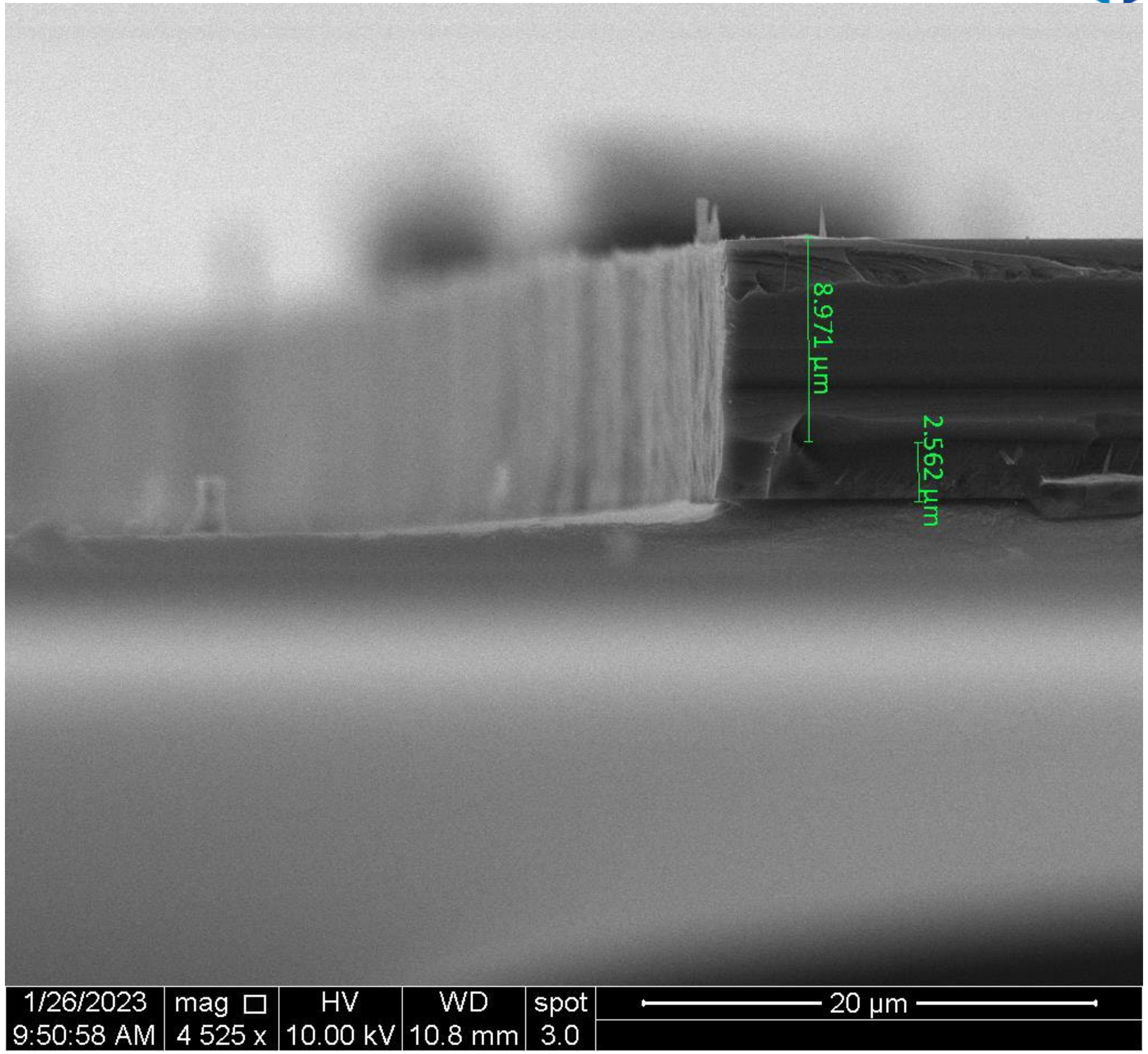
2023 SoP-TM Sidewalls

SoP-TM Sidewall

- 10-100um Silicon process
- 10um Standard Si Thickness
- Sidewall surface optimized for die strength
- Plasma etch (similar to plasma dicing)
- Die Strength Optimization



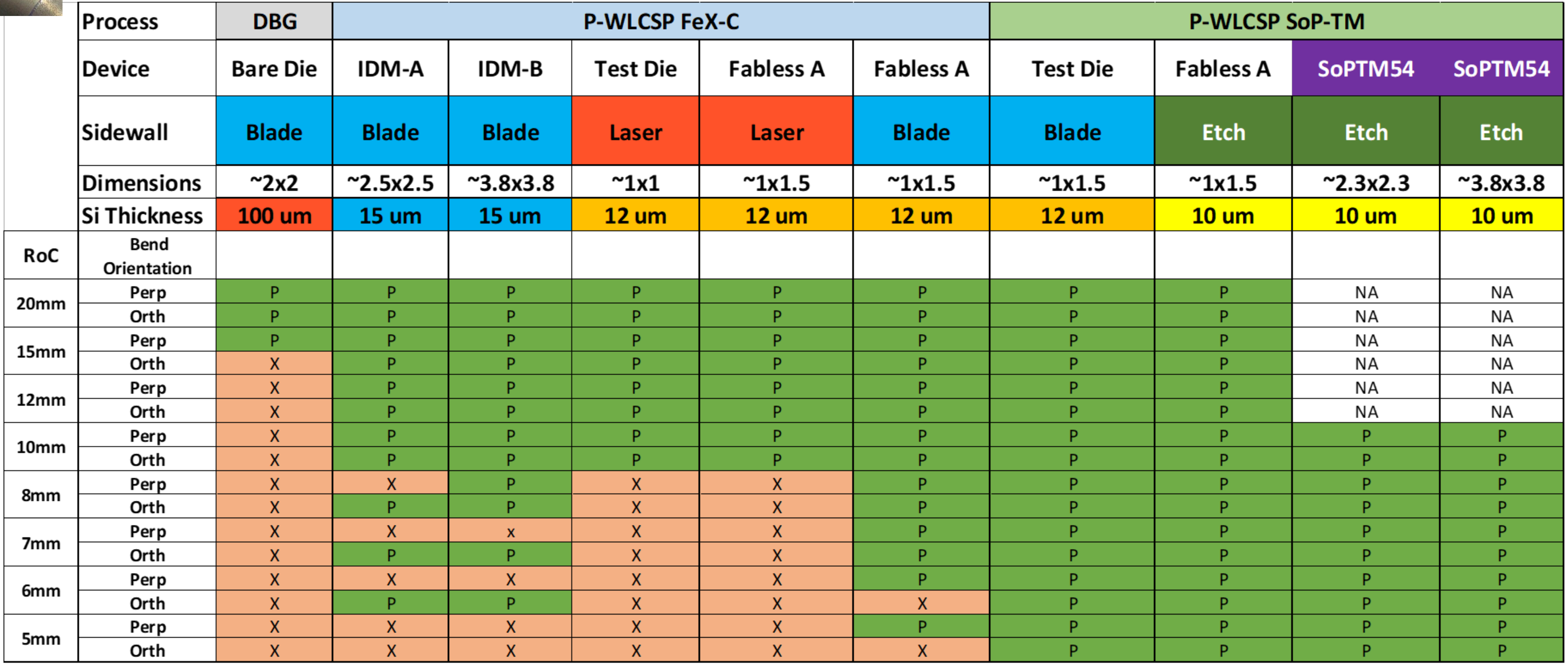
A cross-section view of a SoP-TM™ test die



Die Strength Comparison

Static RoC Testing (TEST003)

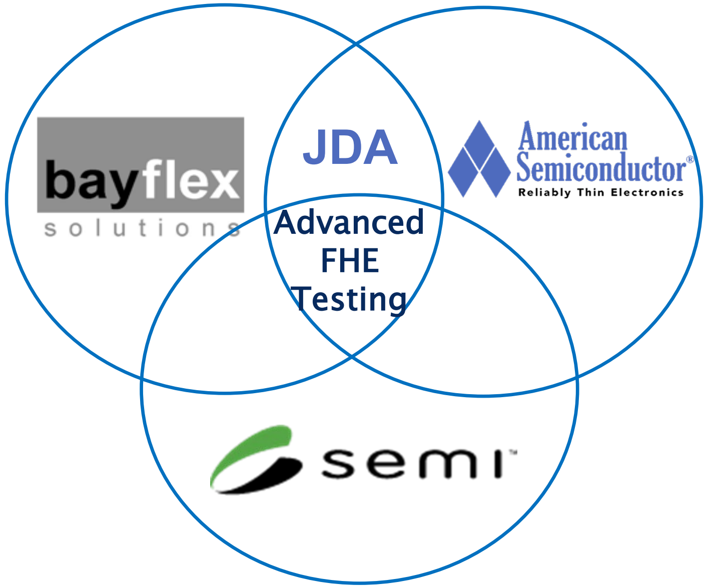
- Manual conformance to RoC mandrel

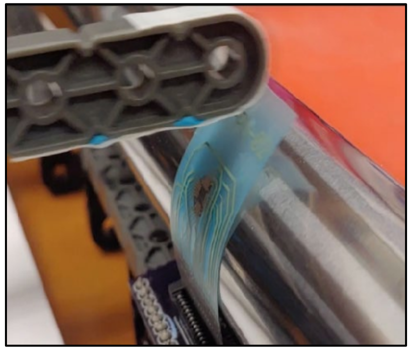


	Process	DBG	P-WLCSP FeX-C					P-WLCSP SoP-TM			
	Device	Bare Die	IDM-A	IDM-B	Test Die	Fabless A	Fabless A	Test Die	Fabless A	SoPTM54	SoPTM54
	Sidewall	Blade	Blade	Blade	Laser	Laser	Blade	Blade	Etch	Etch	Etch
	Dimensions	~2x2	~2.5x2.5	~3.8x3.8	~1x1	~1x1.5	~1x1.5	~1x1.5	~1x1.5	~2.3x2.3	~3.8x3.8
	Si Thickness	100 um	15 um	15 um	12 um	12 um	12 um	12 um	10 um	10 um	10 um
RoC	Bend Orientation										
20mm	Perp	P	P	P	P	P	P	P	P	NA	NA
	Orth	P	P	P	P	P	P	P	P	NA	NA
15mm	Perp	P	P	P	P	P	P	P	P	NA	NA
	Orth	X	P	P	P	P	P	P	P	NA	NA
12mm	Perp	X	P	P	P	P	P	P	P	NA	NA
	Orth	X	P	P	P	P	P	P	P	NA	NA
10mm	Perp	X	P	P	P	P	P	P	P	P	P
	Orth	X	P	P	P	P	P	P	P	P	P
8mm	Perp	X	X	P	X	X	P	P	P	P	P
	Orth	X	P	P	X	X	P	P	P	P	P
7mm	Perp	X	X	x	X	X	P	P	P	P	P
	Orth	X	P	P	X	X	P	P	P	P	P
6mm	Perp	X	X	X	X	X	P	P	P	P	P
	Orth	X	P	P	X	X	X	P	P	P	P
5mm	Perp	X	X	X	X	X	P	P	P	P	P
	Orth	X	X	X	X	X	X	P	P	P	P

ASI & Bayflex/Yuasa (JDA) & SEMI collaboration

- Dynamic Bend Test (Die Strength)
- ASI TEST005 derived from ASTM D522-93a
  - Chips mounted on flex coupons of PET or PI
  - Robotic cycling at specific (RoC) for bend, concave and convex
- Developing test equipment and methods
- Equipment development
  - Universal sample mounting
  - Method for electrical connection (in-situ bias device operation)
  - Mechanical design to isolate targeted axis of motion
  - Compatible mini-environments for temp, humidity, etc.
- Method development
  - Flexure direction and amplitude
  - Test coupon design
  - Targeted cycle counts
  - Acceptable cycle rates
- ASI/Bayflex collaboration with SEMI to create NIST standards





Current ROC Endurance Test

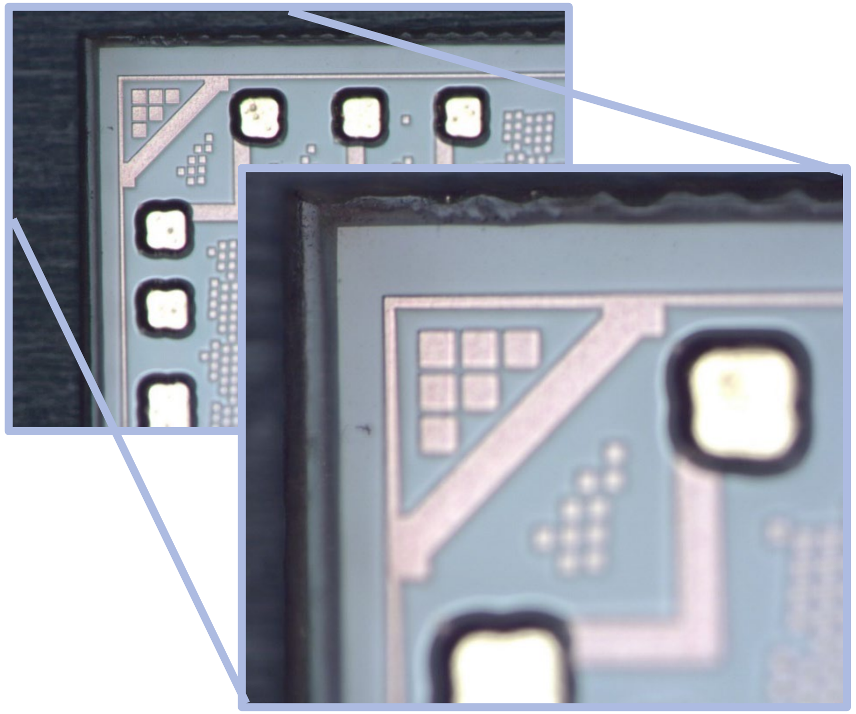
Bayflex/ASI ROC Endurance Test

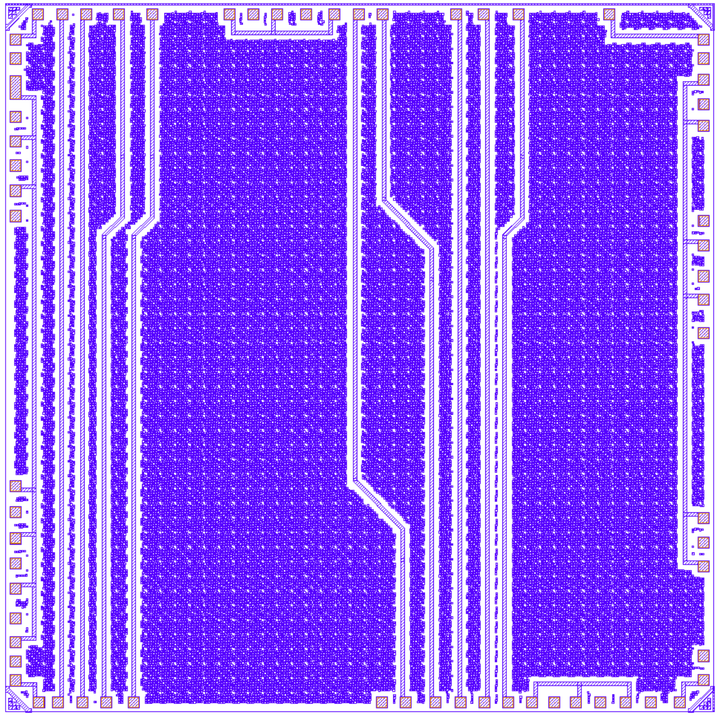
2023 SoP-TM initial process release

DPC2023 – Process Release and Test Chips

SoP-TM has been released for early industry adoption. The high-efficiency P-WLCSP process for protected FI includes ultra-thin package capability and is supported with Test Chips for assembly verification and development.

SoP-TM™ Test Die Samples in case





AS_SoPTM54AP_A.fxd Test Chip

Early Adopter ***SoP-TM – First SoP-TM IC qualification is in-progress by top tier tech company***

Summary and Next Steps

Summary:

- SoP-TM is the “industry 1st”:
  - Wafer level sidewall protected CSP process
  - Fully dry via opening process with no wet develop or wet pad clean, Adaptive Processing
  - CSP process with imaged patterns not limited to photo-definable materials
  - High reliability ENIG bump structure (bump over PI)

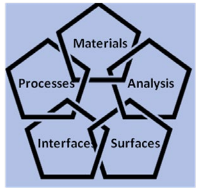
Next Steps

- Accelerated Stress Testing (HAST)
- Dynamic Chip-on-flex Testing (TEST005)
- Capacity Expansion

American Semiconductor - Boise, ID

Member:

Packaging, Assembly, Test and Related Services



MASIP LLC- Phoenix, AZ

MASIP LLC holistic approaches to products/markets

- Market and materials/process trends (IC pkg focus)
- Manufacturing optimization (FA and rel assessments)
- Material and process development & implementation
- Specific application materials and process assessment

Wide experience:

- Electronics-FAB, packaging and assembly
  - early publications and patents for FI & FO (RCP)
- **Material and development**
  - Implemented 1st 2 PSPSI materials at Motorola
  - IP on materials/processes for WSS/flux/AM
- **Material/interface experience and Rel modeling**
  - Solving failure mechanisms (surface/interfaces)
  - Appling material principles to key areas
    - Reliability modeling, Processing, Materials
- **Optimization of plastic package for high reliability**
  - Materials, processes, interfaces

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Thank You

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