Thin and Ultra-thin sidewall protected P-WLCSP

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• Defining “Advanced Packaging” (AP)
  ‣ Advanced packaging is the aggregation and interconnection of components before traditional integrated circuit packaging – Wikipedia
  ‣ Advanced packaging is a general grouping of a variety of distinct techniques, including 2.5D, 3D-IC, fan-out wafer-level packaging and system-in-package – Semiengineering
  ‣ These definitions fail in defining “advanced packaging” as it relates to package manufacturing

• FEOL Example: Next Generation multi-core SOC vs Next Advanced Process Node
  ‣ Scaling from 28nm to 5nm is an example of advanced manufacturing
  ‣ Designing improved multi-core ICs is not, but may be realized in an advanced manufacturing process
  ‣ Advanced manufacturing is not limited by new designs and can provide improvements independent of product designs

• Advanced Packaging is correctly defined as: The leading edge of packaging technology
  ‣ AP can be applied to benefit old and new technology nodes, designs, chiplets, passives, etc.
  ‣ AP is not limited to advanced technology nodes, multi-chip assemblies, AI, 6G, etc.
Advanced Packaging is fundamental to reestablishing U.S. semiconductor manufacturing

• Applying advanced packaging capability to WLCSP for FI is one example
• Die sidewall protection has become important for high IO die reliability
• Advanced Packaging in the form of non-WL CSP FO processes such as M-Series and eWLB have been applied to provide side protection (6S) for FI
• Non-WL CSP includes die reconstitution, expensive tapes, molding operations, and resolves the reliability issues for FI, but the added cost and process complexity was and is far from optimal
• Advance Packaging for P-WLCSP can resolve the issues associated with using FO processing to achieve FI reliability AND enable commercial on-shore packaging by providing cost advantages
6-side protection: P-WLCSP

- “Protected WLCSP” (P-WLCSP) resolves Cost and Complexity of non-WL for FI
  - 6-side protection without the cost and complexity on non-WL FO type processes
  - P-WLCSP does not require pre-package die thinning, dicing or reconstitution
  - P-WLCSP Substantially reduce the equipment and process steps required for processing
  - Material reductions with the elimination of dicing tape and molding materials

- Example: SoP-TM™ 6-side protected P-WLCSP introduced at IMAPS 2021
  - Full protection, without the cost/complexity of non-WL FO processes used for protected CSP FI
  - 300mm process utilizes polyimide for encasement
  - The process includes maskless processing and high temperature temporary bonding
  - Adaptive processing expands the selection of PIs available for stress balancing
  - Final singulation (dicing) speed enhancement due to P-WLCSP PI scribe streets

- Enabling ultra-thin devices
  - Reduced die thickness improves capability for through silicon via (TSV) size and pitch
  - Enables high-temperature backside RDL (B-RDL) and heat sinks
  - CMOS silicon thicknesses is typically 10-15um, but can be adjusted as needed
• Non-WL CSP vs P-WLCSP SoP illustrates advanced packaging benefits for FI

- P-WLCSP provides cost reduction and performance improvement in CSP FI applications
- 50% fewer steps → 50% less capital, or 2X capacity increased for existing facilities
- 50% Less labor cost → Cycle time 50% less, improves cash flow
- 30-50% Less material cost

SoP-TM – Enables On-Shore Manufacturing
IMAPS 2021 - 1st Silicon Results announced

SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection utilizes polyimide for encasement. The process includes maskless processing, high temperature temporary bonding, final singulation with extremely fast laser dicing.
DPC2022 - SoP-TM development update
Current progress for SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection
Improved sidewall formation and demonstration of laser singulation

Trench 45um
Top PI (PSB) 10um
Silicon 10um
Bottom PI (PSB) 4um
Sidewall PI (PSB) ~7um
Adaptive Processing
• Adaptive processing with direct write
• Maskless processing during RDL steps such as for via.

High Speed SoP Dicing
• Multi-pass recipe proves 200 mm/s effective cut speed
• Low power of 1.25 Watts.
• SoP polyimide encasement cuts cleanly without scorching
• Smooth cut line without need of protective coatings/cleans

Throughput (pre-production tool)
• Demonstrated at 4-5 WPH for 2 mm die on a 200 mm wafer.
SoP-TM Sidewall

- 10-100um Silicon process
- 10um Standard Si Thickness
- Sidewall surface optimized for die strength
- Plasma etch (similar to plasma dicing)
- Die Strength Optimization
**Static RoC Testing (TEST003)**

- Manual conformance to RoC mandrel

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<thead>
<tr>
<th>Process</th>
<th>DBG</th>
<th>P-WL CSP FeX-C</th>
<th>P-WLCSP SoP-TM</th>
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<tbody>
<tr>
<td>Device</td>
<td>Bare Die</td>
<td>IDM-A</td>
<td>IDM-B</td>
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<td>Sidewall</td>
<td>Blade</td>
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<td>Dimensions</td>
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• Dynamic Bend Test (Die Strength)
• ASI TEST005 derived from ASTM D522-93a
  ‣ Chips mounted on flex coupons of PET or PI
  ‣ Robotic cycling at specific (RoC) for bend, concave and convex
• Developing test equipment and methods
• Equipment development
  ‣ Universal sample mounting
  ‣ Method for electrical connection (in-situ bias device operation)
  ‣ Mechanical design to isolate targeted axis of motion
  ‣ Compatible mini-environments for temp, humidity, etc.
• Method development
  ‣ Flexure direction and amplitude
  ‣ Test coupon design
  ‣ Targeted cycle counts
  ‣ Acceptable cycle rates
• ASI/Bayflex collaboration with SEMI to create NIST standards
DPC2023 – Process Release and Test Chips
SoP-TM has been released for early industry adoption. The high-efficiency P-WLCSP process for protected FI includes ultra-thin package capability and is supported with Test Chips for assembly verification and development.
Summary:
• SoP-TM is the “industry 1st”:
  ‣ Wafer level sidewall protected CSP process
  ‣ Fully dry via opening process with no wet develop or wet pad clean, Adaptive Processing
  ‣ CSP process with imaged patterns not limited to photo-definable materials
  ‣ High reliability ENIG bump structure (bump over PI)

Next Steps
• Accelerated Stress Testing (HAST)
• Dynamic Chip-on-flex Testing (TEST005)
• Capacity Expansion
American Semiconductor - Boise, ID

**Flexible Hybrid Lab**

Class 100 Cleanroom

**Packaging, Assembly, Test and Related Services**

MASIP LLC- Phoenix, AZ

**MASIP LLC holistic approaches to products/markets**
- Market and materials/process trends (IC pkg focus)
- Manufacturing optimization (FA and rel assessments)
- Material and process development & implementation
- Specific application materials and process assessment

**Wide experience:**
- Electronics-FAB, packaging and assembly
  - early publications and patents for FI & FO (RCP)
- Material and development
  - Implemented 1st 2 PSPSI materials at Motorola
  - IP on materials/processes for WSS/flux/AM
- Material/interface experience and Rel modeling
  - Solving failure mechanisms (surface/interfaces)
  - Applying material principles to key areas
    - Reliability modeling, Processing, Materials
- Optimization of plastic package for high reliability
  - Materials, processes, interfaces
Thank You

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