Cost Analysis of Fan-out Processes for Chiplet Packaging

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Agenda

- Introduction
- Process Flows
- Cost Comparison
  - Fan-out on Substrate vs. Flip Chip
  - Fan-out with Embedded Silicon vs. Flip ChIp
- Summary

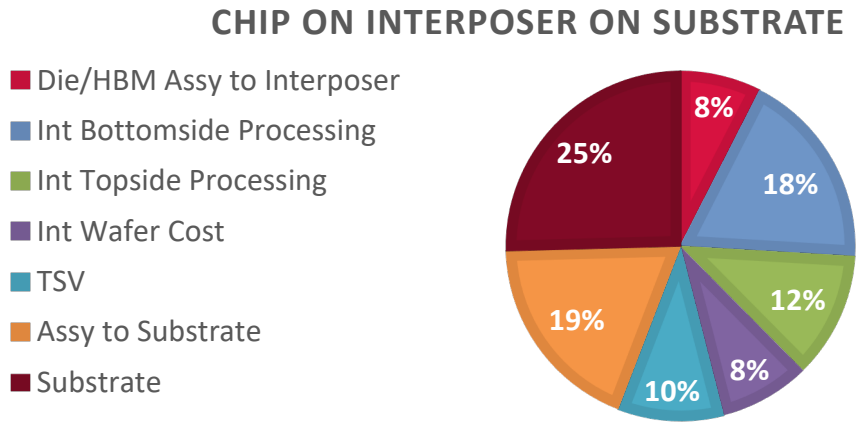
Introduction

- When building a design around chiplets, there are many factors to consider, including:
  - Industry standards (or lack thereof)
  - Availability of chiplets within the supply chain
  - Size requirements
  - Cost
- Even if all design requirements can be met by the current supply chain, the chiplet design will not be produced if the cost is too high
- Basic tradeoff between a monolithic SoC die and a series of chiplets is a reduction in die costs countered by an increase in packaging costs
  - Reduction in die costs comes from using advanced (expensive) nodes ONLY where required
  - Instead of a large monolithic die, the entirety of which must be at the node required for its most advanced function, chiplets provide the opportunity to mix and match mature and advanced nodes
  - A 10x10mm die at 10nm can be about twice as much as a 10x10mm die at 28nm

Activity Based Cost Modeling

- Bottom-up approach to cost that accounts for every cost component for every activity
  - The time required to complete the activity
  - The amount of labor dedicated to the activity
  - The cost of material required to perform that activity – both consumable and permanent material
  - Any tooling cost
  - The depreciation cost of the equipment required to perform the activity
  - The yield loss associated with the activity
- Detailed output enables results to be seen in detail or rolled up in categories

Step Name	Labor Cost/Wafer	Capital Cost/Wafer	Tooling Cost/Wafer	Material Cost/Wafer	Yield Cost
RDL Spin coat	$ 0.08	$ 3.63	$ -	$ 7.38	$ 0.062
RDL Mask Cost	$ -	$ -	$ -	$ 0.21	$ 0.001
RDL Expose	$ 0.02	$ 2.07	$ -	$ -	$ 0.014
RDL Develop	$ 0.03	$ 1.54	$ -	$ 0.55	$ 0.014
RDL Cure	$ 0.08	$ 0.19	$ -	$ -	$ 0.002



Process Flow Overviews

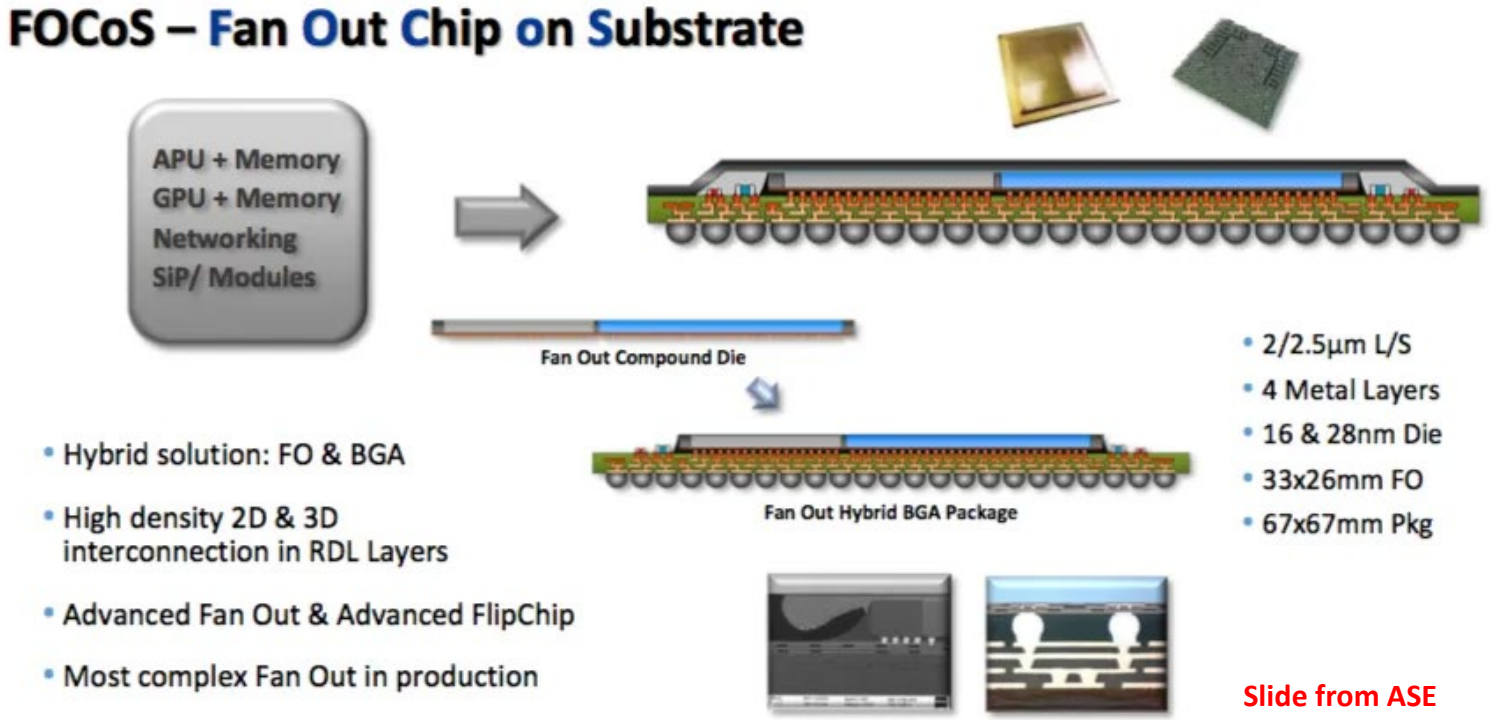
- Upcoming slides introduce two technologies suitable for packaging chiplets
- Scenario 1: Two-chiplet chip-last fan-out on substrate package vs. standard flip chip package
- Scenario 2: Four-chiplet fan-out package that utilizes embedded silicon for additional interconnect vs. standard flip chip package
- Process flows are genericized
  - Sometimes individual activities are listed, sometimes groups of activities
  - Any process flow may have variations
- When deciding between process flows, it's not just about cost
  - Different advanced packaging options will support different sizes, different number of chiplets, etc.

Fan-out on Substrate

TWO CHIPLET DESIGN

Fan-out on Substrate

- One solution to avoid an interposer
  - ASE example shown below; others (Amkor, TSMC, etc.) have similar solutions
  - Main features that differentiate this from standard fan-out → HBM support, finer line/space RDLs



Slide from ASE

Fan-out on Substrate

Standard Chip-last Fan-out

- Start with carrier, build up RDLs
- Bond chips
- Apply underfill
- Mold
- Ball attach
- Singulate
- Ready for PCB assembly

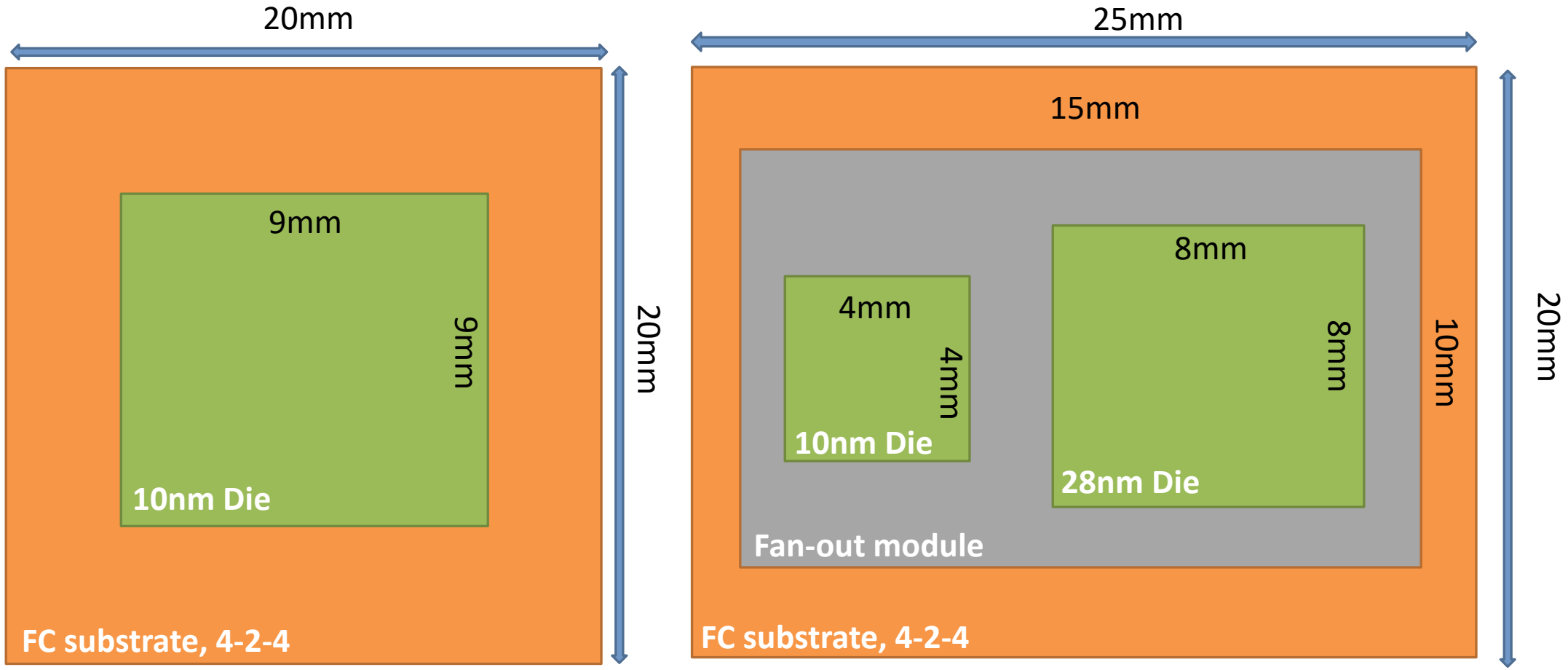
Chip-last Fan-out on Substrate

- Start with carrier, build up RDLs
- Bond chiplets
- Apply underfill
- Mold
- Debond from Carrier
- Add microbumps to bottom of fan-out wafer
- Singulate
- Place diced fan-out package on substrate
- Attach solder balls to substrate
- Ready for PCB assembly

Chiplets have microbumps or copper pillars, so this is a die bonding, not a simple placement

Fan-out on Substrate vs. FC Design

Monolithic die, flip chip connection



Drawing not to scale

Fan-out on Substrate vs. FC Design

- No overhead or profit margin included
- Factory location (impacting labor rate) same for all
- Same substrate structure assumed for all
- RDL count kept low to simplify

	FC Design	Fan-out on Substrate
Die Size (mmxmm)	9x9mm 10nm die	4x4 10nm die, 8x8 28nm die
Fan-out Module Size (mmxmm)		15x10
Substrate Size (mmxmm)	20x20	25x20
BOM Items	1 die	2 die
RDLs		2

Total area of die in both scenarios approx. the same (~80mm^2)

Fan-out on Substrate vs. FC Design

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This is a helpful assumption for understanding direct cost differences between technologies. This is not helpful when you must think about *price*. More on this later.

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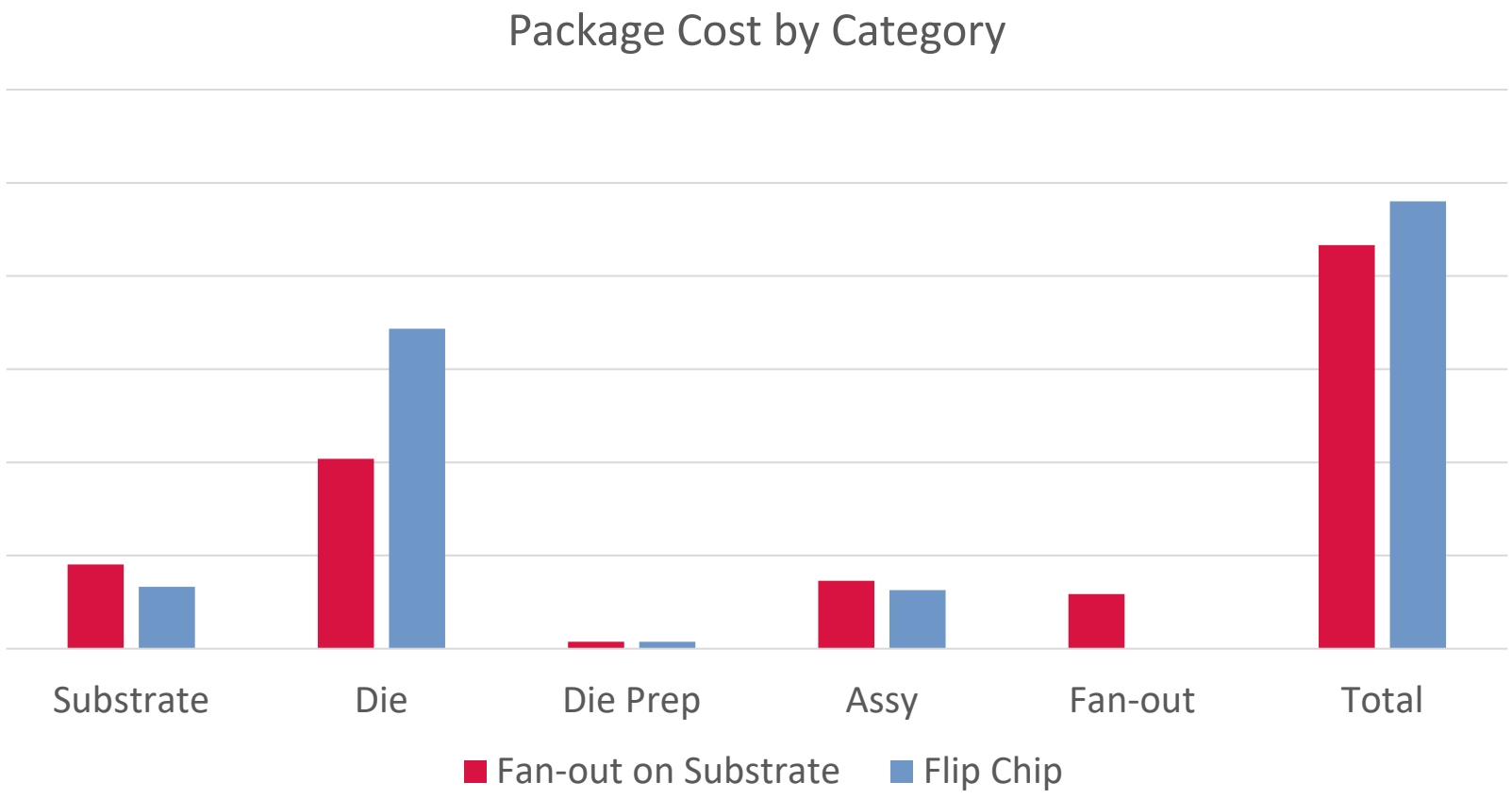

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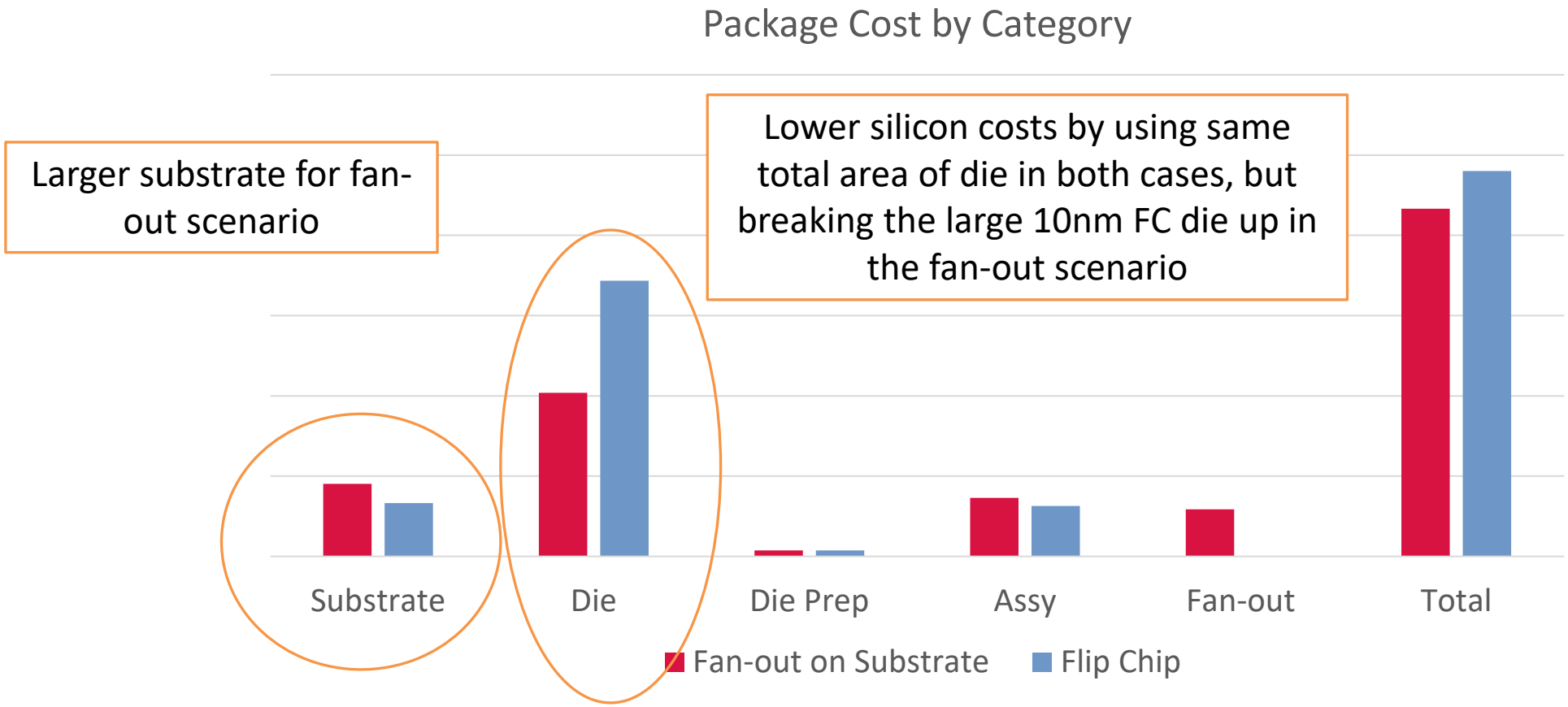
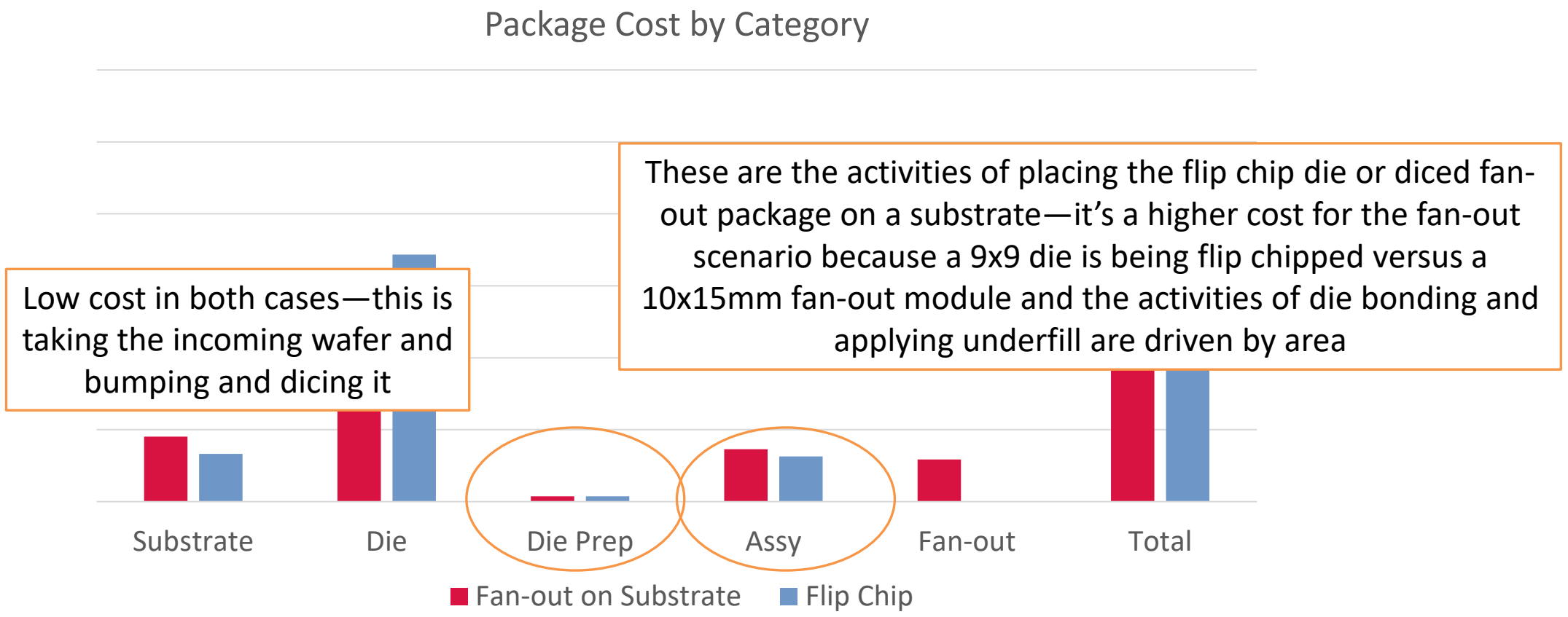


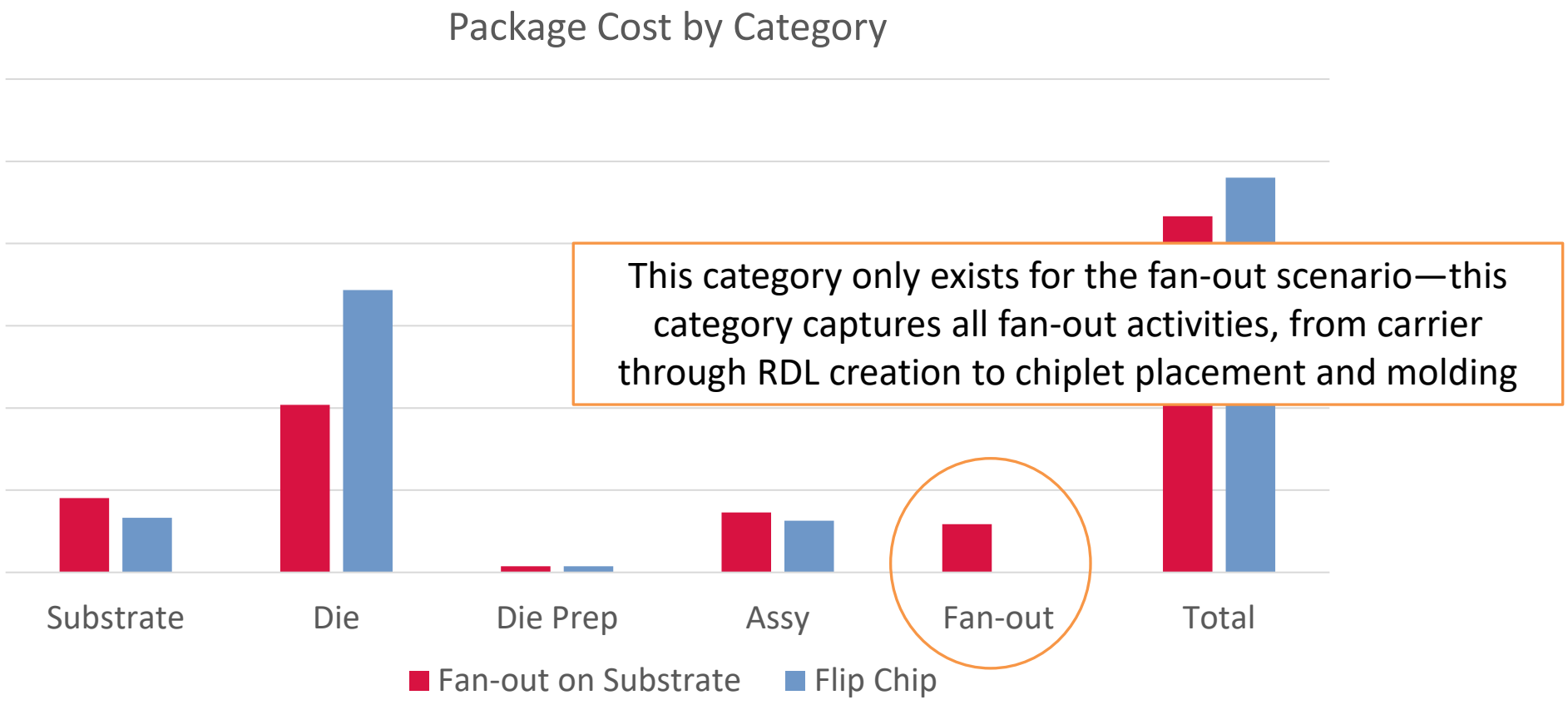
Fan-out on Substrate vs. FC Design



Low cost in both cases—this is taking the incoming wafer and bumping and dicing it

These are the activities of placing the flip chip die or diced fan-out package on a substrate—it's a higher cost for the fan-out scenario because a 9x9 die is being flip chipped versus a 10x15mm fan-out module and the activities of die bonding and applying underfill are driven by area

Fan-out on Substrate vs. FC Design



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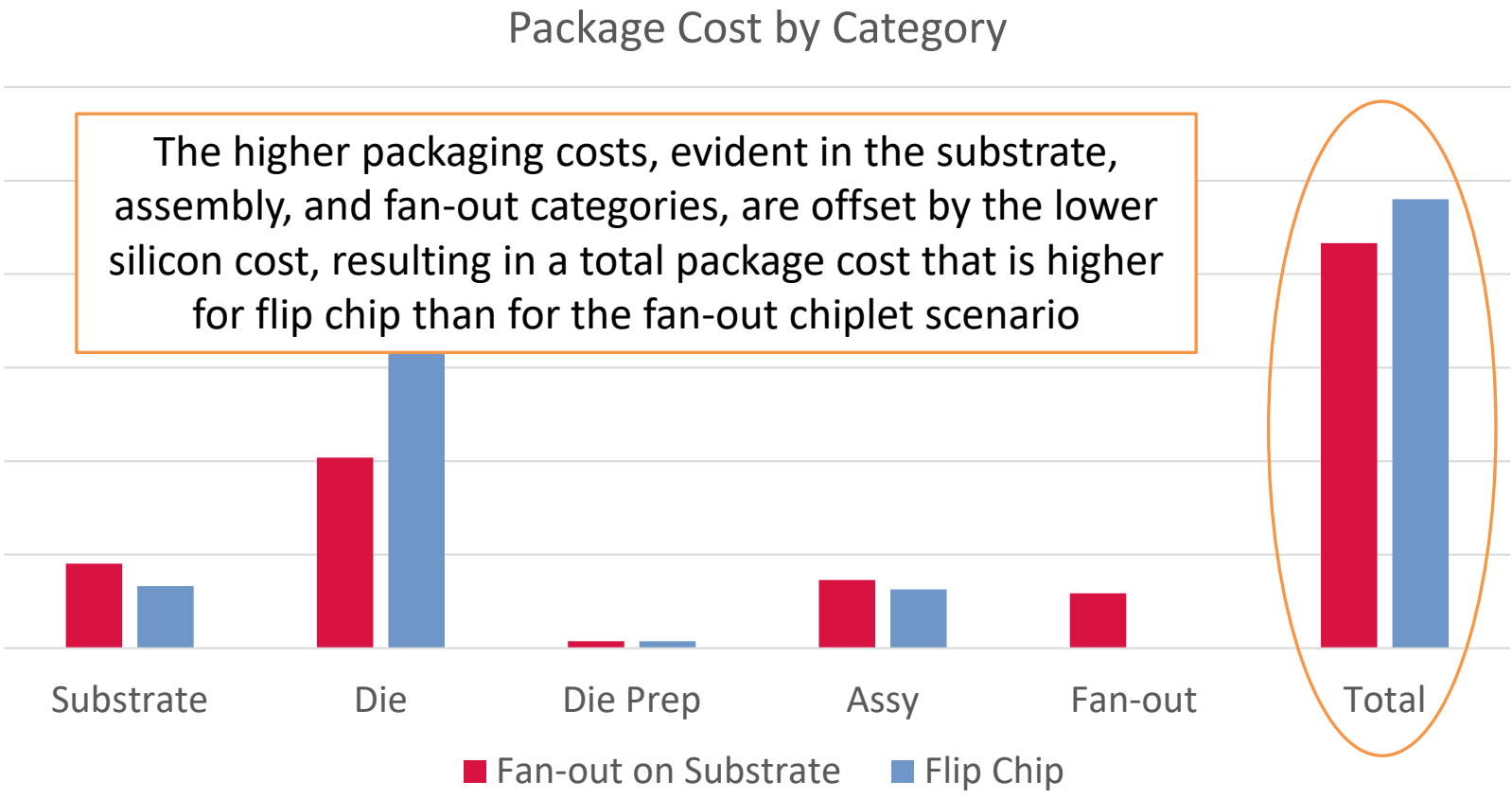


Takeaway

- Does this mean fan-out on substrate is always more cost effective for packaging chiplets than a flip chip package? → No
- Results are heavily dependent on fan-out module size, die size and which node is necessary for each die, how much larger the substrate must be, how many RDLs are needed, among other factors
- Previous example shows the fan-out scenario to be 10% less expensive than flip chip
- Table below shows how the relative cost changes with one variable change

Scenario	Fan-out Cost relative to FC
Baseline Scenario	-10%
Fan-out module extended by 1mm in each direction	-7%
3 RDLs	-7%
1% yield drop for fan-out	-9%
16nm instead of 10nm	12%

Fan-out with Embedded Silicon

FOUR CHIPLET DESIGN

Fan-out with Embedded Silicon Bridges

- Another solution to avoid an interposer
- Embed a piece of silicon in a fan-out module to provide interconnect paths between die
  - Requires less silicon than a full silicon interposer
  - SPIL has FOEB (Fan-out Embedded Bridge), Intel has EMIB (Embedded Multi-die Interconnect Bridge), etc.

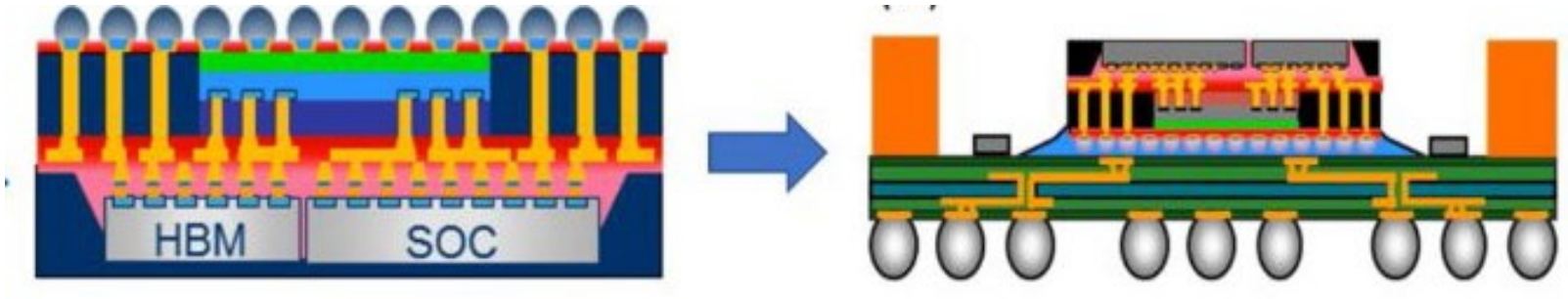
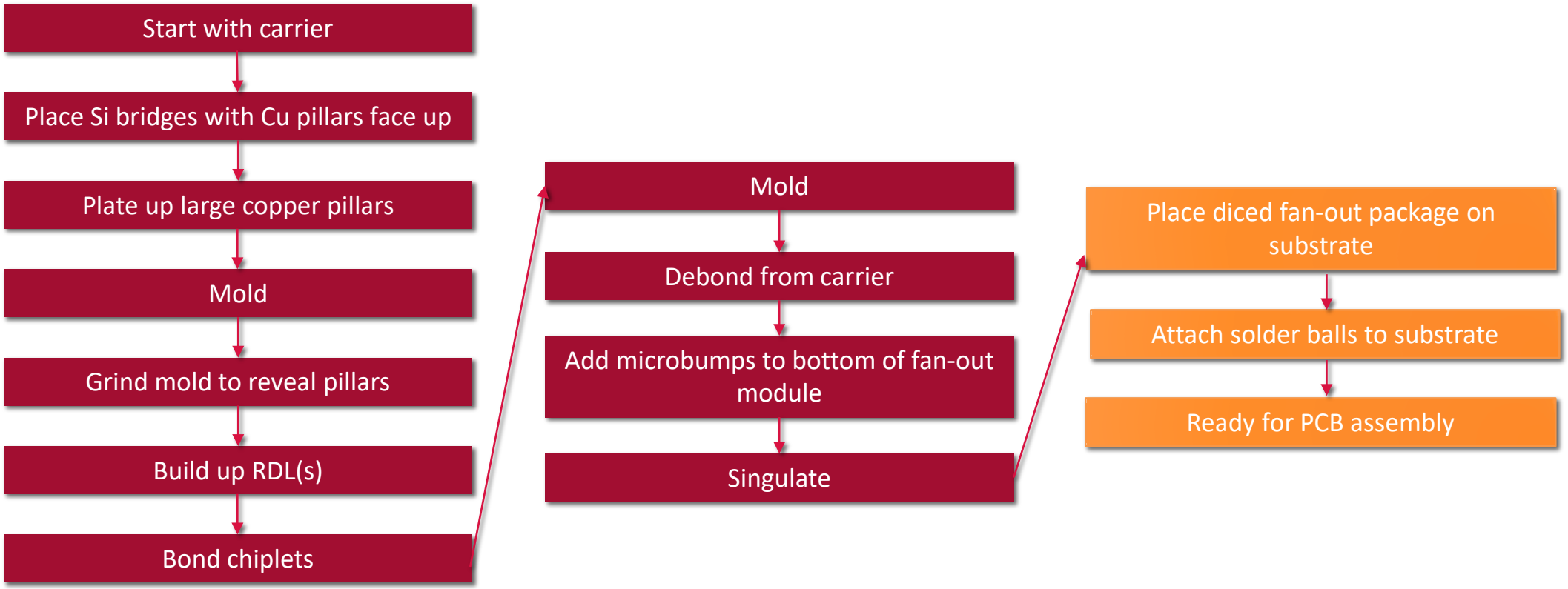


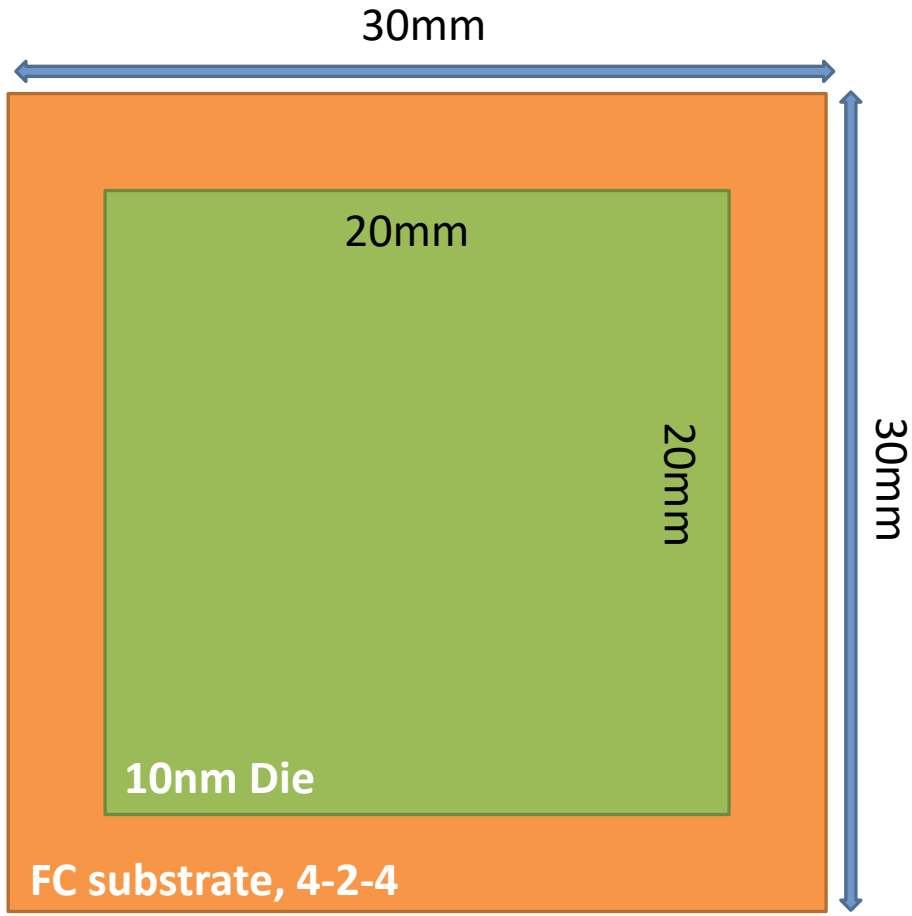
Image from SPIL

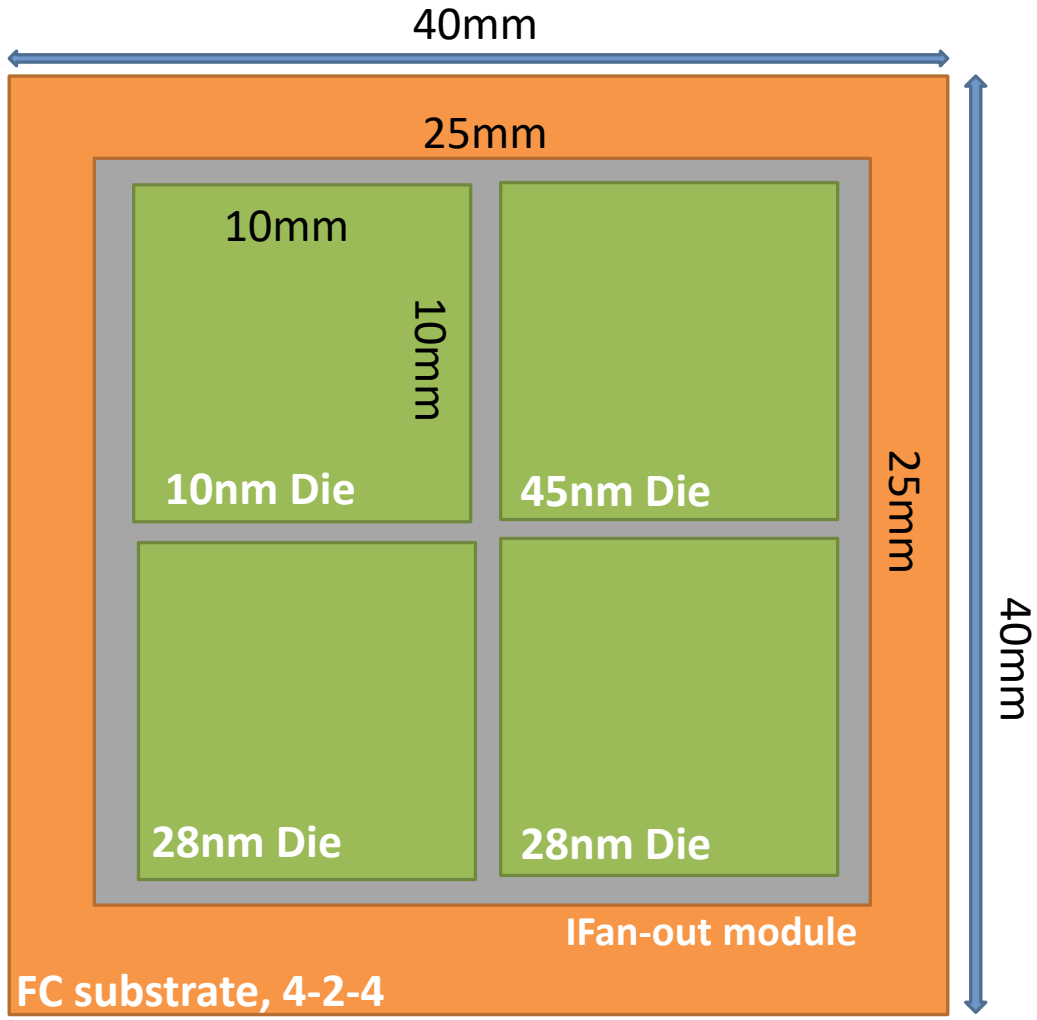
Fan-out with Embedded Silicon Bridges



Fan-out on w/Embedded Si vs. FC Design

Monolithic die, flip chip connection





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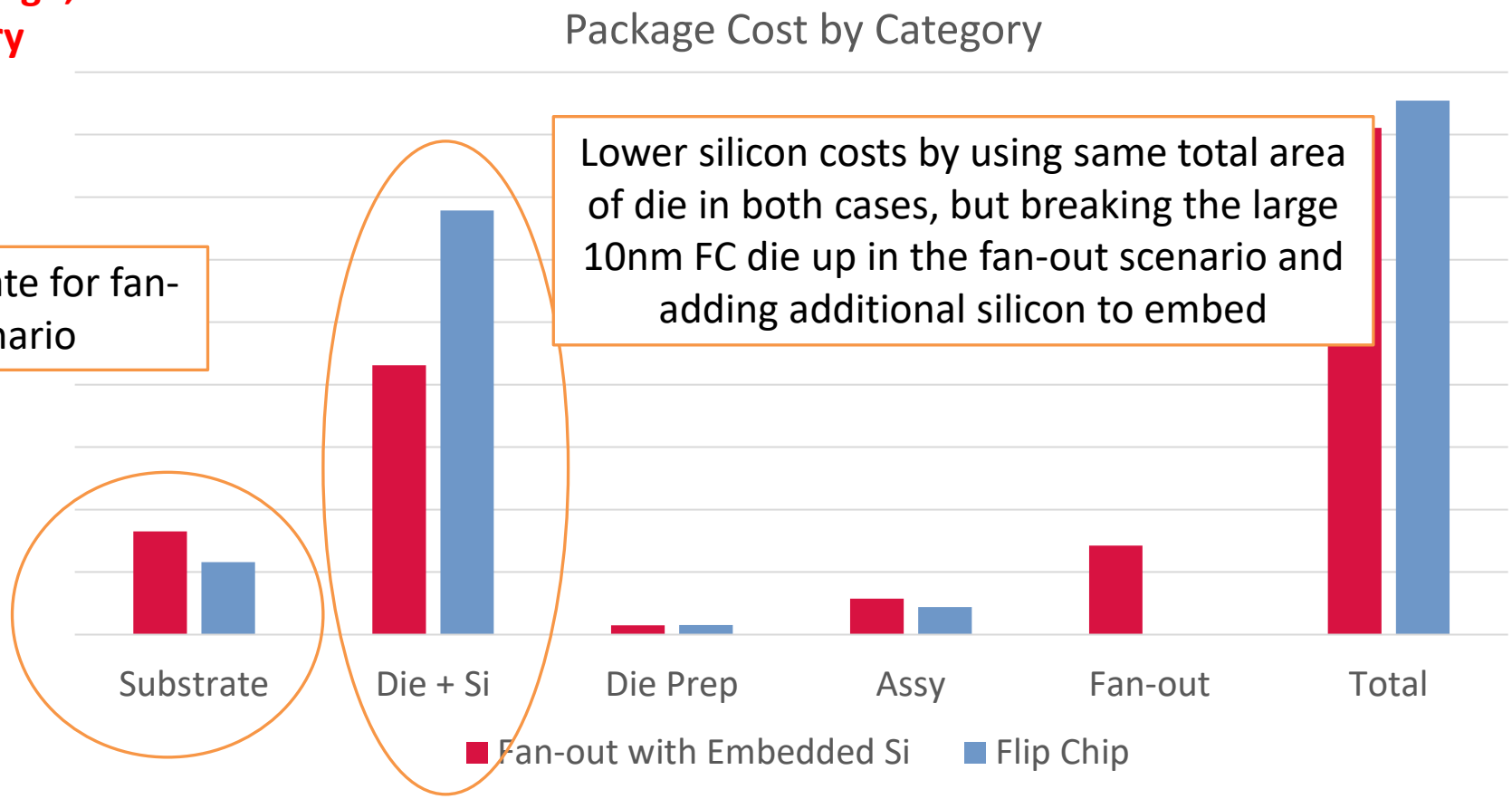
Fan-out on w/Embedded Si vs. FC Design

- No overhead or profit margin included
- Factory location (impacting labor rate) same for all
- Same substrate structure assumed for all
- RDL count kept low to simplify

	FC Design	Fan-out w/Emb Si
Die Size (mmxmm)	20x20mm 10nm die	All die 10x10mm Two 28nm, One 45nm One 10nm
Fan-out Module Size (mmxmm)		25x25
Substrate Size (mmxmm)	30x30	40x40
BOM Items	1 die	4 die, 2 silicon bridges to embed, 50 cents each
RDLs		1 topside, 1 bottom side, both fine l/s

Fan-out on w/Embedded Si vs. FC Design

Different design, same story

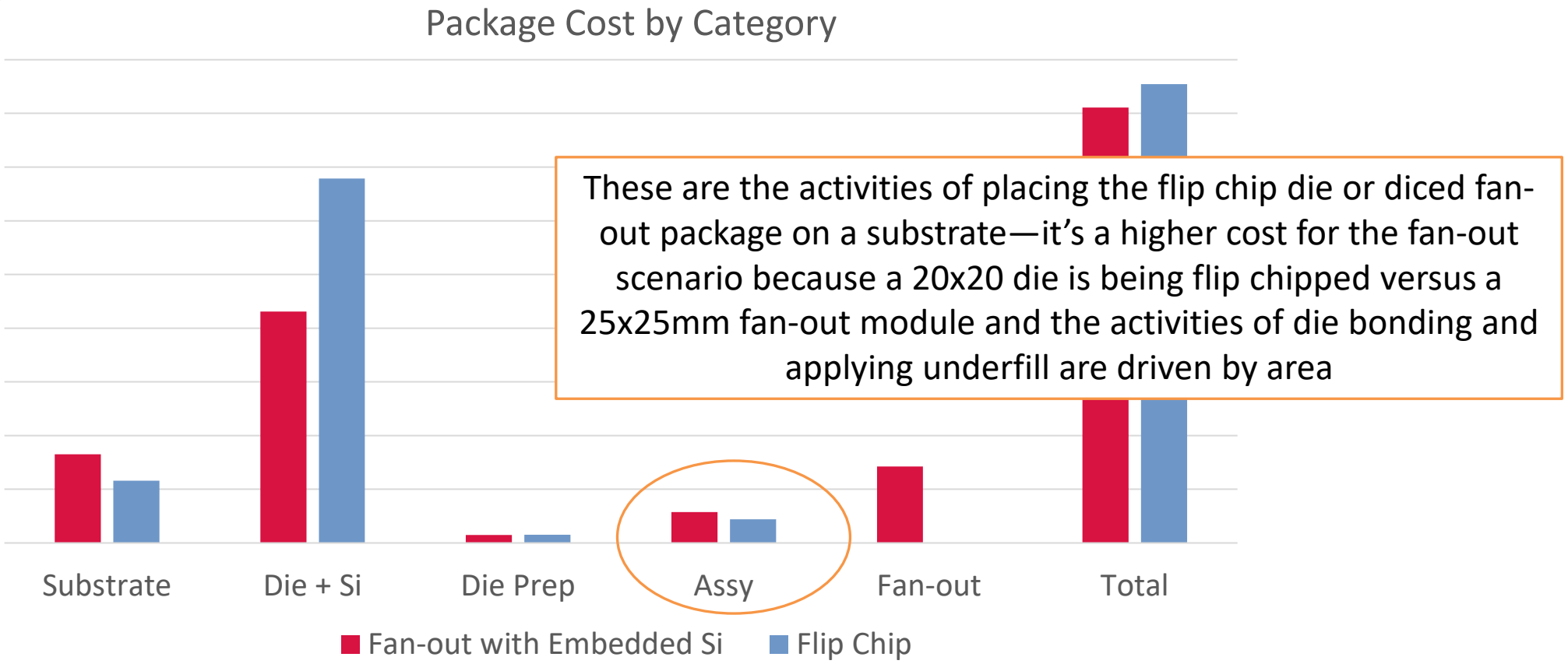


Larger substrate for fan-out scenario

Lower silicon costs by using same total area of die in both cases, but breaking the large 10nm FC die up in the fan-out scenario and adding additional silicon to embed

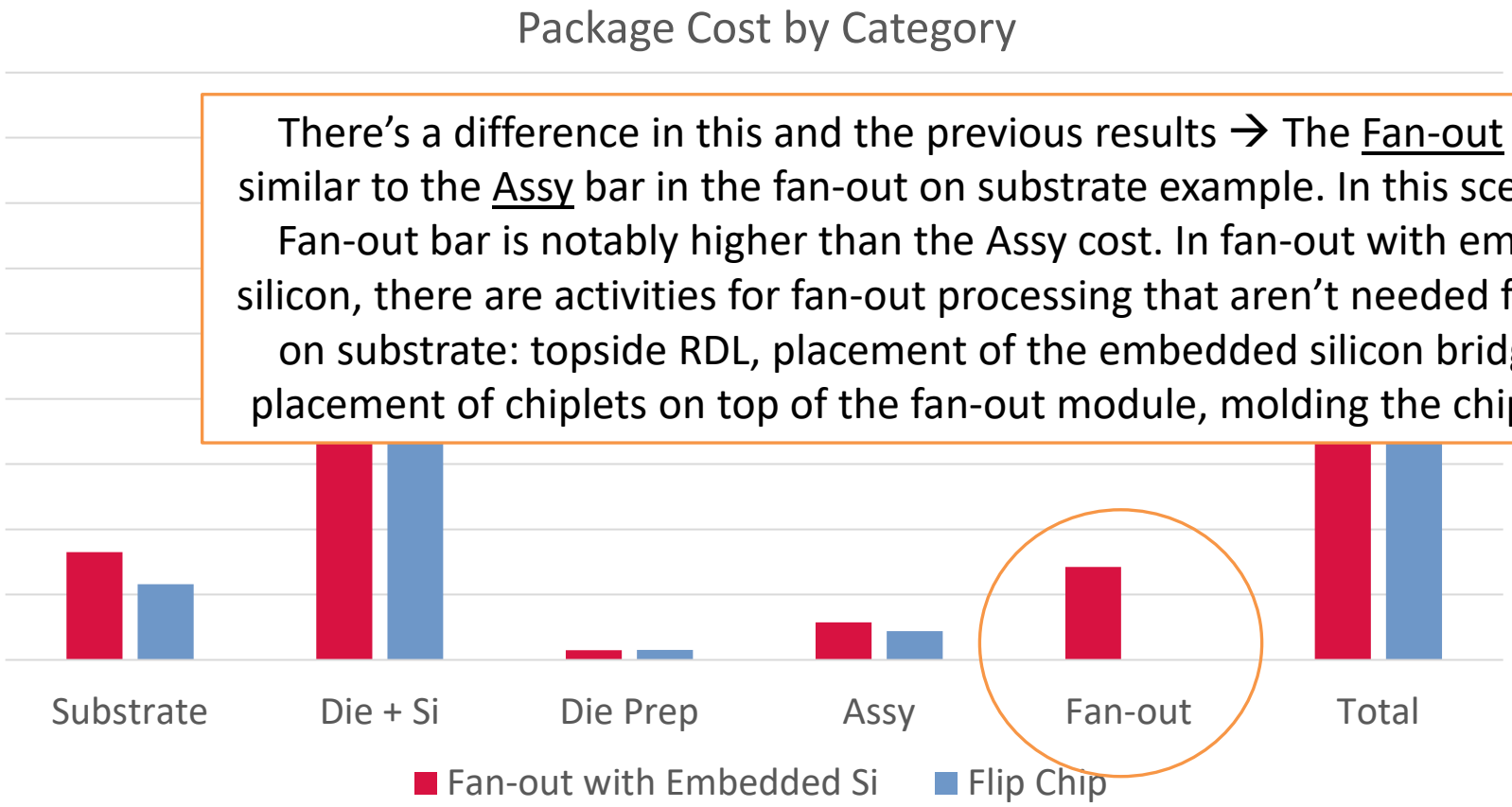
Fan-out on w/Embedded Si vs. FC Design

Different design, same story



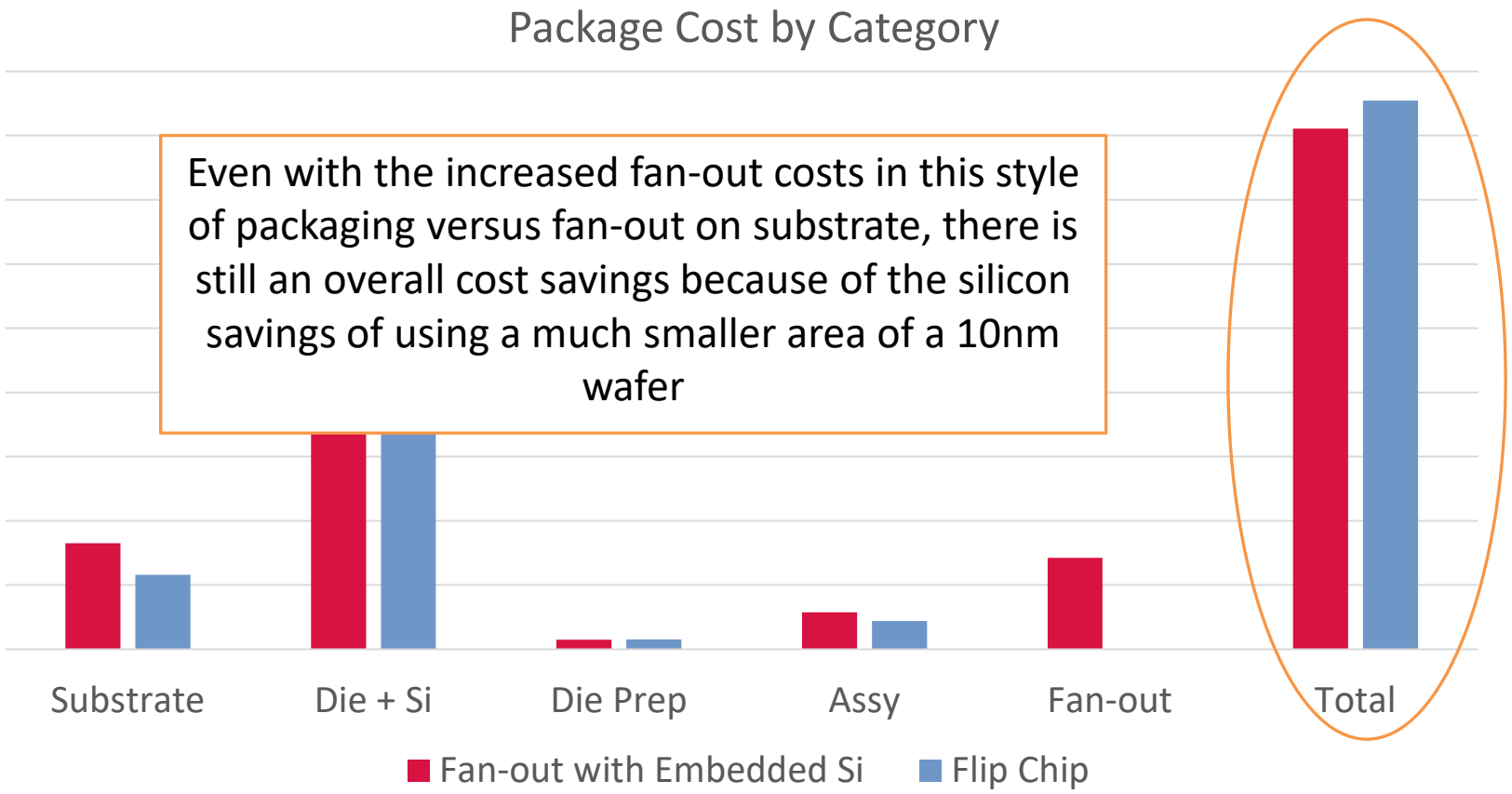
These are the activities of placing the flip chip die or diced fan-out package on a substrate—it's a higher cost for the fan-out scenario because a 20x20 die is being flip chipped versus a 25x25mm fan-out module and the activities of die bonding and applying underfill are driven by area

Fan-out on w/Embedded Si vs. FC Design



There's a difference in this and the previous results → The Fan-out bar was similar to the Assy bar in the fan-out on substrate example. In this scenario, the Fan-out bar is notably higher than the Assy cost. In fan-out with embedded silicon, there are activities for fan-out processing that aren't needed for fan-out on substrate: topside RDL, placement of the embedded silicon bridges plus placement of chiplets on top of the fan-out module, molding the chiplets, etc.

Fan-out on w/Embedded Si vs. FC Design



Takeaway

- Does this mean fan-out on with embedded silicon is always more cost effective than a flip chip package? → No
- As before, many design factors impact whether a chiplet design will be cost-effective with fan-out technology
  - Package size, substrate size, number of RDLs, yield considerations, etc.

Scenario	How much more expensive is FC, per package?
Baseline Scenario	$2.17
2% yield drop for fan-out	$1.82
Fan-out module extended by 1mm in each direction	$1.79
One 20nm die instead of a 28nm die	$1.21
2 topside RDLs, 2 bottom RDLs	$0.28

Cost vs. Price

- The focus of this technology comparison is direct cost → A valuable way to understand the cost drivers of disparate technologies
- In the real world, a designer or user would want to think about price
- Price is complicated and impacted by many factors not represented in this analysis
  - Factory utilization and the volume of the package being built impact price
  - Indirect costs must also be considered; these are factory costs not directly associated with a specific activity like support, quality, manufacturing engineering, utilities, and clean room
  - There are overhead costs, which are generally company costs that need to be covered, like marketing and engineering
  - Profit margin must be factored in
- This analysis is a great starting point to understand how newer technologies like fan-out may compete with a mature process like flip chip, but real world pricing may ultimately drive very different results at this point in time

Summary

- Basic tradeoff between a monolithic die and a series of chiplets is a **reduction** in die costs countered by an **increase** in packaging costs
- Various advanced packaging technologies are emerging to support chiplets
  - Fan-out on substrate shown for a two-chiplet design
  - Fan-out with embedded silicon shown for a four-chiplet design
- For both designs, some categories of direct cost were more expensive with fan-out—substrate costs, assembly costs, fan-out processing costs—but the silicon savings were enough to make the fan-out package more cost-effective than the flip chip package
- Fan-out packaging of chiplets will not always be more cost-effective
  - Chiplet size, chiplet nodes, required package size, required substrate size, and number of RDLs are some of the design attributes that will determine whether chiplets are cost-effective
- Chiplet packaging is complex → Every scenario should be evaluated before committing to a packaging method

Thank you!

Contact amyl@savansys.com with any questions or comments