Cost Analysis of Fan-out Processes for Chiplet Packaging

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Agenda

- Introduction
- Process Flows
- Cost Comparison
  - Fan-out on Substrate vs. Flip Chip
  - Fan-out with Embedded Silicon vs. Flip Chip
- Summary
Introduction

- When building a design around chiplets, there are many factors to consider, including:
  - Industry standards (or lack thereof)
  - Availability of chiplets within the supply chain
  - Size requirements
  - Cost

- Even if all design requirements can be met by the current supply chain, the chiplet design will not be produced if the cost is too high

- Basic tradeoff between a monolithic SoC die and a series of chiplets is a reduction in die costs countered by an increase in packaging costs
  - Reduction in die costs comes from using advanced (expensive) nodes ONLY where required
  - Instead of a large monolithic die, the entirety of which must be at the node required for its most advanced function, chiplets provide the opportunity to mix and match mature and advanced nodes
  - A 10x10mm die at 10nm can be about twice as much as a 10x10mm die at 28nm
Activity Based Cost Modeling

- Bottom-up approach to cost that accounts for every cost component for every activity
  - The time required to complete the activity
  - The amount of labor dedicated to the activity
  - The cost of material required to perform that activity – both consumable and permanent material
  - Any tooling cost
  - The depreciation cost of the equipment required to perform the activity
  - The yield loss associated with the activity

- Detailed output enables results to be seen in detail or rolled up in categories
Process Flow Overviews

- Upcoming slides introduce two technologies suitable for packaging chiplets
- Scenario 1: Two-chiplet chip-last fan-out on substrate package vs. standard flip chip package
- Scenario 2: Four-chiplet fan-out package that utilizes embedded silicon for additional interconnect vs. standard flip chip package

- Process flows are genericized
  - Sometimes individual activities are listed, sometimes groups of activities
  - Any process flow may have variations

- When deciding between process flows, it’s not just about cost
  - Different advanced packaging options will support different sizes, different number of chiplets, etc.
Fan-out on Substrate

TWO CHIPLET DESIGN
Fan-out on Substrate

- One solution to avoid an interposer
  - ASE example shown below; others (Amkor, TSMC, etc.) have similar solutions
  - Main features that differentiate this from standard fan-out → HBM support, finer line/space RDLs

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**FOCoS – Fan Out Chip on Substrate**

- APU + Memory
- GPU + Memory
- Networking
- SIP/ Modules

- Hybrid solution: FO & BGA
- High density 2D & 3D Interconnection in RDL Layers
- Advanced Fan Out & Advanced FlipChip
- Most complex Fan Out in production

- 2/2.5μm L/S
- 4 Metal Layers
- 16 & 28nm Die
- 33x26mm Die
- 67x67mm Pkg

Slide from ASE
Fan-out on Substrate

Standard Chip-last Fan-out
- Start with carrier, build up RDLs
- Bond chips
- Apply underfill
- Mold
- Ball attach
- Singulate
- Ready for PCB assembly

Chip-last Fan-out on Substrate
- Start with carrier, build up RDLs
- Bond chiplets
- Apply underfill
- Mold
- Debond from Carrier
- Add microbumps to bottom of fan-out wafer
- Singulate
- Place diced fan-out package on substrate
- Attach solder balls to substrate
- Ready for PCB assembly

Chiplets have microbumps or copper pillars, so this is a die bonding, not a simple placement
Fan-out on Substrate vs. FC Design

Monolithic die, flip chip connection

**Drawing not to scale**
Fan-out on Substrate vs. FC Design

- No overhead or profit margin included
- Factory location (impacting labor rate) same for all
- Same substrate structure assumed for all
- RDL count kept low to simplify

<table>
<thead>
<tr>
<th></th>
<th>FC Design</th>
<th>Fan-out on Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die Size (mmxmm)</strong></td>
<td>9x9mm 10nm die</td>
<td>4x4 10nm die, 8x8 28nm die</td>
</tr>
<tr>
<td><strong>Fan-out Module Size (mmxmm)</strong></td>
<td></td>
<td>15x10</td>
</tr>
<tr>
<td><strong>Substrate Size (mmxmm)</strong></td>
<td></td>
<td>20x20 25x20</td>
</tr>
<tr>
<td><strong>BOM Items</strong></td>
<td>1 die</td>
<td>2 die</td>
</tr>
<tr>
<td><strong>RDLs</strong></td>
<td></td>
<td>2</td>
</tr>
</tbody>
</table>

Total area of die in both scenarios approx. the same (~80mm²)
Fan-out on Substrate vs. FC Design

- No overhead or profit margin included
- Factory location (impacting labor rate) same for all
- Same substrate structure assumed for all
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This is a helpful assumption for understanding direct cost differences between technologies. This is not helpful when you must think about *price*. More on this later.

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<table>
<thead>
<tr>
<th>Category</th>
<th>Fan-out on Substrate</th>
<th>Flip Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die Prep</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assy</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fan-out</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Fan-out on Substrate vs. FC Design**

Package Cost by Category
Fan-out on Substrate vs. FC Design

Package Cost by Category

Larger substrate for fan-out scenario

Lower silicon costs by using same total area of die in both cases, but breaking the large 10nm FC die up in the fan-out scenario
Fan-out on Substrate vs. FC Design

Package Cost by Category

Low cost in both cases—this is taking the incoming wafer and bumping and dicing it.

These are the activities of placing the flip chip die or diced fan-out package on a substrate—it’s a higher cost for the fan-out scenario because a 9x9 die is being flip chipped versus a 10x15mm fan-out module and the activities of die bonding and applying underfill are driven by area.
Fan-out on Substrate vs. FC Design

Package Cost by Category

This category only exists for the fan-out scenario—this category captures all fan-out activities, from carrier through RDL creation to chiplet placement and molding.
The higher packaging costs, evident in the substrate, assembly, and fan-out categories, are offset by the lower silicon cost, resulting in a total package cost that is higher for flip chip than for the fan-out chiplet scenario.
Takeaway

- Does this mean fan-out on substrate is always more cost effective for packaging chiplets than a flip chip package? → No

- Results are heavily dependent on fan-out module size, die size and which node is necessary for each die, how much larger the substrate must be, how many RDLs are needed, among other factors

- Previous example shows the fan-out scenario to be 10% less expensive than flip chip

- Table below shows how the relative cost changes with one variable change

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Fan-out Cost relative to FC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline Scenario</td>
<td>-10%</td>
</tr>
<tr>
<td>Fan-out module extended by 1mm in each direction</td>
<td>-7%</td>
</tr>
<tr>
<td>3 RDLs</td>
<td>-7%</td>
</tr>
<tr>
<td>1% yield drop for fan-out</td>
<td>-9%</td>
</tr>
<tr>
<td>16nm instead of 10nm</td>
<td>12%</td>
</tr>
</tbody>
</table>
Fan-out with Embedded Silicon

FOUR CHIPLET DESIGN
Fan-out with Embedded Silicon Bridges

- Another solution to avoid an interposer

- Embed a piece of silicon in a fan-out module to provide interconnect paths between die
  - Requires less silicon than a full silicon interposer
  - SPIL has FOEB (Fan-out Embedded Bridge), Intel has EMIB (Embedded Multi-die Interconnect Bridge), etc.
Fan-out with Embedded Silicon Bridges

1. Start with carrier
2. Place Si bridges with Cu pillars face up
3. Plate up large copper pillars
4. Mold
5. Grind mold to reveal pillars
6. Build up RDL(s)
7. Bond chiplets
8. Mold
9. Debond from carrier
10. Add microbumps to bottom of fan-out module
11. Singulate
12. Place diced fan-out package on substrate
13. Attach solder balls to substrate
14. Ready for PCB assembly

Ready for PCB assembly
Fan-out on w/Embedded Si vs. FC Design

Monolithic die, flip chip connection

**Drawing not to scale**
Fan-out on w/Embedded Si vs. FC Design

- No overhead or profit margin included
- Factory location (impacting labor rate) same for all
- Same substrate structure assumed for all
- RDL count kept low to simplify

<table>
<thead>
<tr>
<th></th>
<th>FC Design</th>
<th>Fan-out w/Emb Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size (mmxmm)</td>
<td>20x20mm 10nm die</td>
<td>All die 10x10mm Two 28nm, One 45nm One 10nm</td>
</tr>
<tr>
<td>Fan-out Module Size (mmxmm)</td>
<td></td>
<td>25x25</td>
</tr>
<tr>
<td>Substrate Size (mmxmm)</td>
<td>30x30</td>
<td>40x40</td>
</tr>
<tr>
<td>BOM Items</td>
<td>1 die</td>
<td>4 die, 2 silicon bridges to embed, 50 cents each</td>
</tr>
<tr>
<td>RDLs</td>
<td>1 topside, 1 bottom side, both fine l/s</td>
<td></td>
</tr>
</tbody>
</table>
**Fan-out on w/Embedded Si vs. FC Design**

Different design, same story

- Larger substrate for fan-out scenario
- Lower silicon costs by using same total area of die in both cases, but breaking the large 10nm FC die up in the fan-out scenario and adding additional silicon to embed

Package Cost by Category

- Substrate
- Die + Si
- Die Prep
- Assy
- Fan-out
- Total

- Fan-out with Embedded Si
- Flip Chip
Different design, same story

These are the activities of placing the flip chip die or diced fan-out package on a substrate—it’s a higher cost for the fan-out scenario because a 20x20 die is being flip chipped versus a 25x25mm fan-out module and the activities of die bonding and applying underfill are driven by area.
There’s a difference in this and the previous results. The **Fan-out** bar was similar to the **Assy** bar in the fan-out on substrate example. In this scenario, the **Fan-out** bar is notably higher than the **Assy** cost. In fan-out with embedded silicon, there are activities for fan-out processing that aren’t needed for fan-out on substrate: topside RDL, placement of the embedded silicon bridges plus placement of chiplets on top of the fan-out module, molding the chiplets, etc.
Even with the increased fan-out costs in this style of packaging versus fan-out on substrate, there is still an overall cost savings because of the silicon savings of using a much smaller area of a 10nm wafer.
Takeaway

- Does this mean fan-out on with embedded silicon is always more cost effective than a flip chip package? → No

- As before, many design factors impact whether a chiplet design will be cost-effective with fan-out technology
  - Package size, substrate size, number of RDLs, yield considerations, etc.

<table>
<thead>
<tr>
<th>Scenario</th>
<th>How much more expensive is FC, per package?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline Scenario</td>
<td>$2.17</td>
</tr>
<tr>
<td>2% yield drop for fan-out</td>
<td>$1.82</td>
</tr>
<tr>
<td>Fan-out module extended by 1mm in each direction</td>
<td>$1.79</td>
</tr>
<tr>
<td>One 20nm die instead of a 28nm die</td>
<td>$1.21</td>
</tr>
<tr>
<td>2 topside RDLs, 2 bottom RDLs</td>
<td>$0.28</td>
</tr>
</tbody>
</table>
Cost vs. Price

- The focus of this technology comparison is direct cost → A valuable way to understand the cost drivers of disparate technologies

- In the real world, a designer or user would want to think about price

- Price is complicated and impacted by many factors not represented in this analysis
  - Factory utilization and the volume of the package being built impact price
  - Indirect costs must also be considered; these are factory costs not directly associated with a specific activity like support, quality, manufacturing engineering, utilities, and clean room
  - There are overhead costs, which are generally company costs that need to be covered, like marketing and engineering
  - Profit margin must be factored in

- This analysis is a great starting point to understand how newer technologies like fan-out may compete with a mature process like flip chip, but real world pricing may ultimately drive very different results at this point in time
Summary

- Basic tradeoff between a monolithic die and a series of chiplets is a **reduction** in die costs countered by an **increase** in packaging costs.

- Various advanced packaging technologies are emerging to support chiplets
  - Fan-out on substrate shown for a two-chiplet design
  - Fan-out with embedded silicon shown for a four-chiplet design

- For both designs, some categories of direct cost were more expensive with fan-out—substrate costs, assembly costs, fan-out processing costs—but the silicon savings were enough to make the fan-out package more cost-effective than the flip chip package.

- Fan-out packaging of chiplets will not always be more cost-effective
  - Chiplet size, chiplet nodes, required package size, required substrate size, and number of RDLs are some of the design attributes that will determine whether chiplets are cost-effective.

- Chiplet packaging is complex → Every scenario should be evaluated before committing to a packaging method.
Thank you!

Contact amyl@savansys.com with any questions or comments