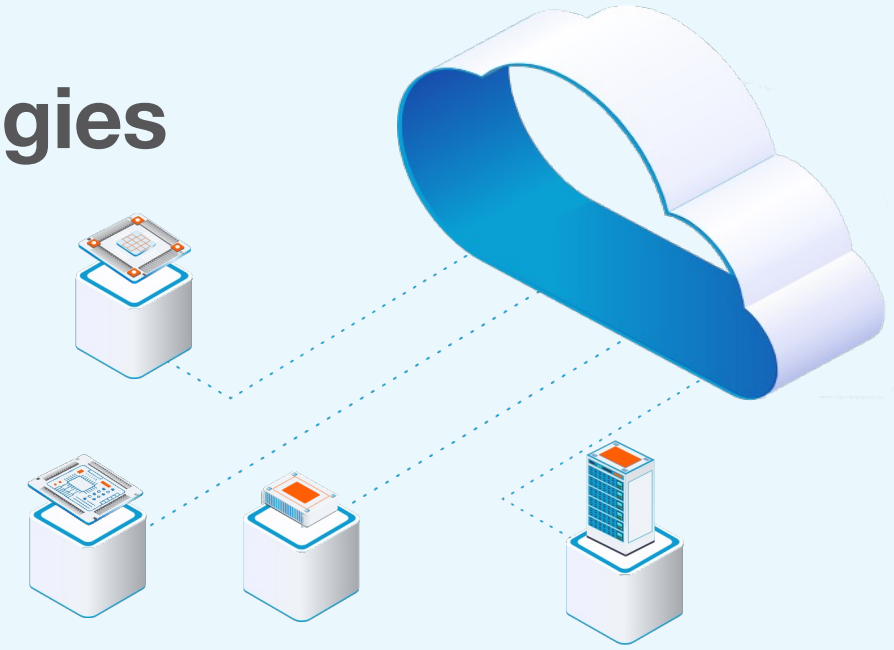
proteanTecs
Electronics visibility. From within

ADVANTEST®

iMAPS

Advanced Test Technologies for Heterogeneous & 2.5D/3D Packaging



March 2023

Marc Hutner, proteanTecs | Ken Butler, Advantest Inc

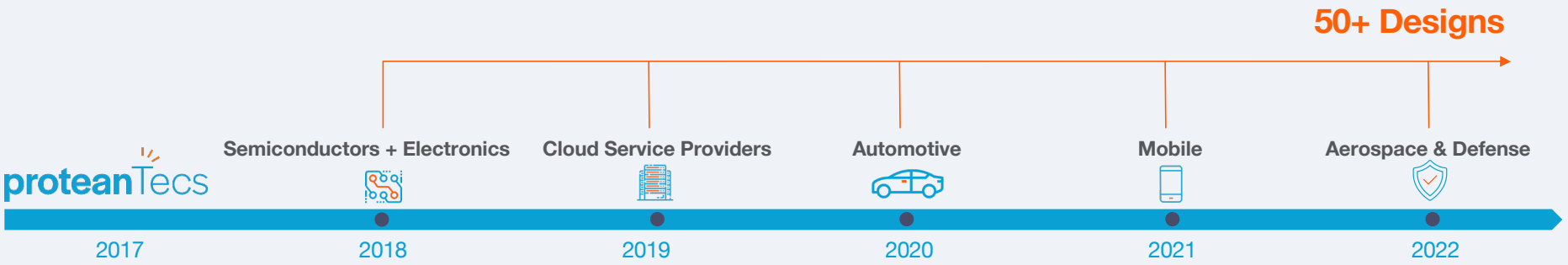
Introduction

- Multi-Chip packaging is enabling the next wave of innovation in electronics
- Driving increased test complexity for wafer and package testing
- Die-to-Die (D2D) interfaces are an enabler SIP with improved power per bit transmission
- We will present a test solution for D2D interfaces that enables
  - Full test solution where we present silicon results and test method at ATE
  - Provides per-lane parametric grading
  - Adaptive tester decision making leveraging trained functions

proteanTecs at a glance

Trusted by industry leaders

Hyperscalers • Fortune 100 corporations • OEMs • Disruptive startups • ASIC and IP vendors



Member of Leading Industry Affiliations:

Foundries

tsmc Open Innovation Platform®

SAMSUNG SAFE™

Standardization

CHIPS ALLIANCE

ISO 26262

UCIe

Affiliations

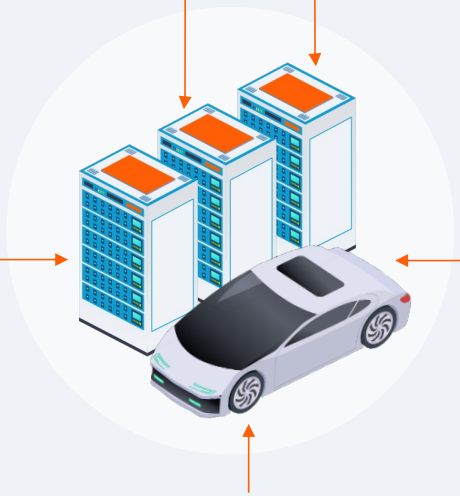
GSA Where Leaders Meet

OPEN COMMUNITY®

Increasing Challenges in Advanced Electronics

Increased thermal density
High performance applications with greater transistor density

Advanced Packaging
Micro-bump cracks and voids, silicon warpage and bridge-shorts on substrate



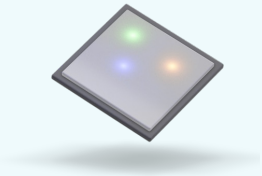
Stronger impact of degradation & failure mechanisms
In-mission manifestation of physics-of-failure becomes common

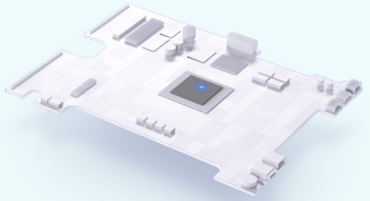
Latent defects
Escapes of marginal or latent defects due to aggressive design architectures and advanced process technologies

SW impact on HW
AI/ML driven applications with dynamic mission profile create ongoing risks

Advanced Analytics Based on Deep Data

- Bring-up
- Qual & Char
- Production
- In-Field





ATE → System → End-Product

pT Cloud Analytics Platform: Data Fusion & Machine Learning Engine

Operational and Application Monitoring

Interconnect Performance Monitoring

Performance and Degradation Monitoring

Classification and Profiling

Realtime Sensors

Design Simulation Data

3rd party Sensors and Test Data

Production System In-Field Data

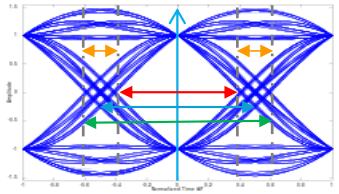
Agents + Simulations + SW Platform = Targeted Analytics & Insights

Targeted Applications per Stage

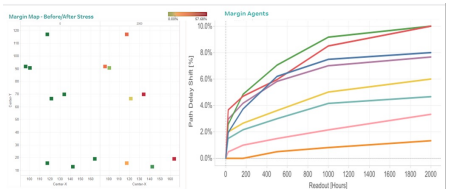
Chip NPI

Post to Pre silicon correlation

Correlation between value chain stages

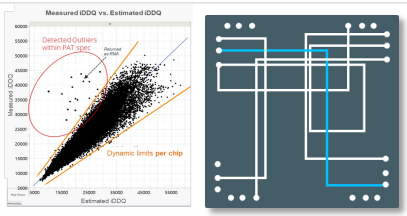


Die-to-die visibility

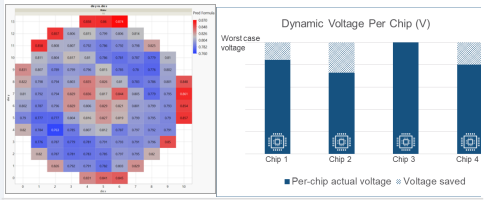


Degradation monitoring in qualification

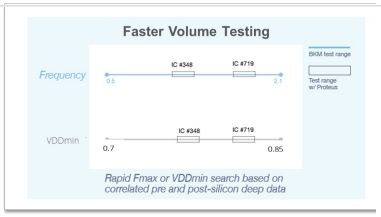
Chip Production



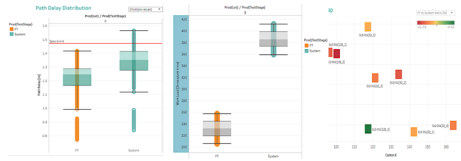
DPPM Reduction (Fine grain latent defects screening)



Power reduction



Test time reduction

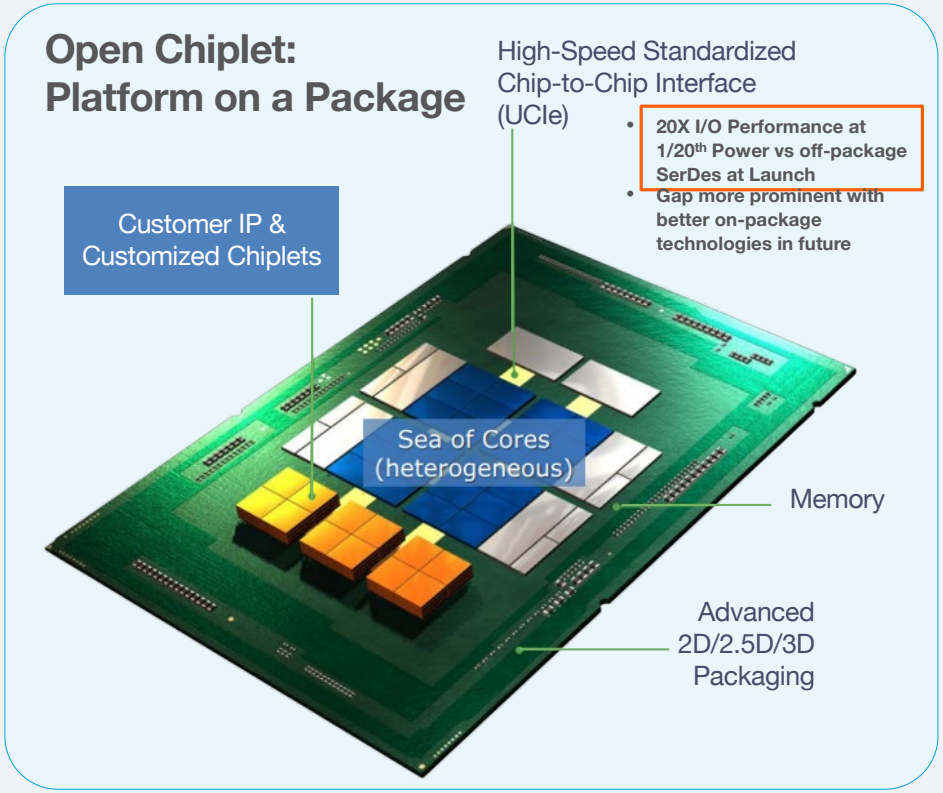


Lower RMAs and Fast Time-to-Resolution

More Than Moore

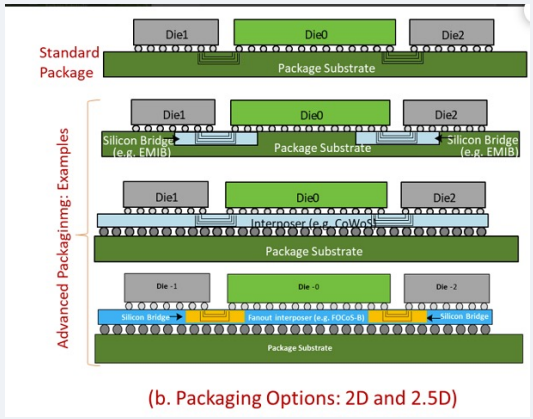
- Allow overcoming reticle size limitations for large devices
- Improve yield: Yield goes down exponentially with size but with tiling, it is linear
- Allow hybrid devices: Each IC in a SiP can be manufactured at a different process:
  - CPU/GPU/NPU/TPU on latest CMOS technology
  - DRAM on DRAM process
  - Wireless/RF on Analog RF process
- Support “economies of scale” with Chiplet
  - Uses the same building block multiplied according to application instead of multiple designs

Efficient interconnect is key for success!



Heterogeneous Integration fueled by an Open Chiplet Ecosystem (Mix-and-match chiplets from different process nodes / fabs / companies / assembly

2.5D/3D Integration Technology Map



(b. Packaging Options: 2D and 2.5D)

	SERDES (112G-XSR)	Parallel (GLink 2.3LL)
Bit Error Rate	1E-7…1E-12	Reliable
Power efficiency	1.5-2.5 pJ/bit	0.27 pJ/bit
Beachfront efficiency	0.6-0.7 Tbps/mm	2.5 Tbps/mm
Area efficiency	0.3-0.5 Tbps/mm^2	2.1 Tbps/mm^2
Total power	150-250 W	27 W
ASIC die beachfront	75-85 mm	20 mm
ASIC die area	100-170 mm^2	24 mm^2

Substrate Technologies

Silicon Interposer

CoWoS®

Organic Substrate

InFO

Serial

XSR/USR SERDES

Optimized for low pin count, long distances
Complex, large area, high power

Optimized for high pin count, short distances
Simple, low area, low power

Parallel

HBM2, HBM2e, HBM3

OpenHBI (-2, -3)

GLink™, AIB (Gen1, Gen2), BoW

UCIe

Industry Test Challenges Have Been Identified

KGD, Quality and Visibility Concerns

SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Waiting For Chiplet Standards

902 Shares

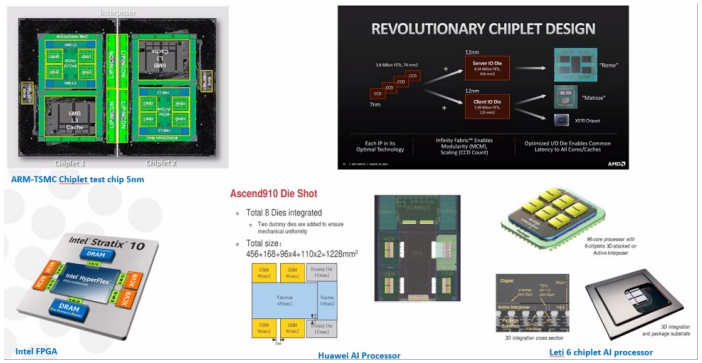
An ecosystem is required to make chiplets a viable strategy for long-term success, and ecosystems are built around standards. Those standards are beginning to emerge today.

MARCH 25TH, 2021 - BY: **BRIAN BAILEY**

The need and desire for chiplets is increasing, but for most companies that shift will happen slowly until proven standards are in place.

Interoperability and compatibility depend on many layers and segments of the supply chain coming to agreement. Unfortunately, fragmented industry requirements may lead to a plethora of solutions.

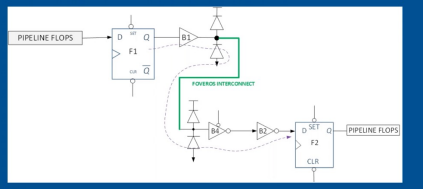
Standards always have enabled increasing specialization. In the early days of the chip industry, a company had to design, implement, and fabricate everything. For most companies, fabrication became separated from design by well-defined interfaces and models, such as PDKs, BSIM models, and libraries.



https://semiengineering.com/waiting-for-chiplet-standards/

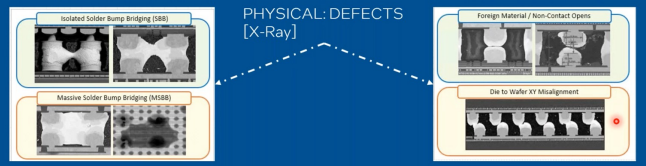
CHIP-LET INTERCONNECT TEST PROBLEM

- Simple Circuit. But ....
- Challenges
  - No touch test
  - Large numbers
  - High density
  - Complicated failure mechanism
  - High failure rate, yield recovery and repair
  - Fault isolation and debug
  - .....



intel
ODSA_OCPJuly2022

WHAT CAUSES INTERCONNECTS TO FAIL?



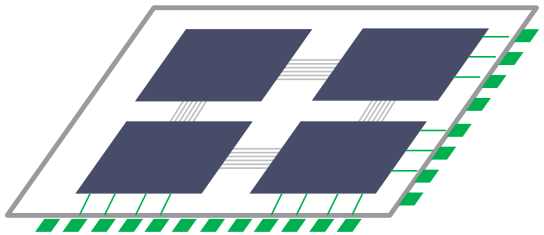
COUPLING
[Spice Simulation]

intel
ODSA_OCPJuly2022

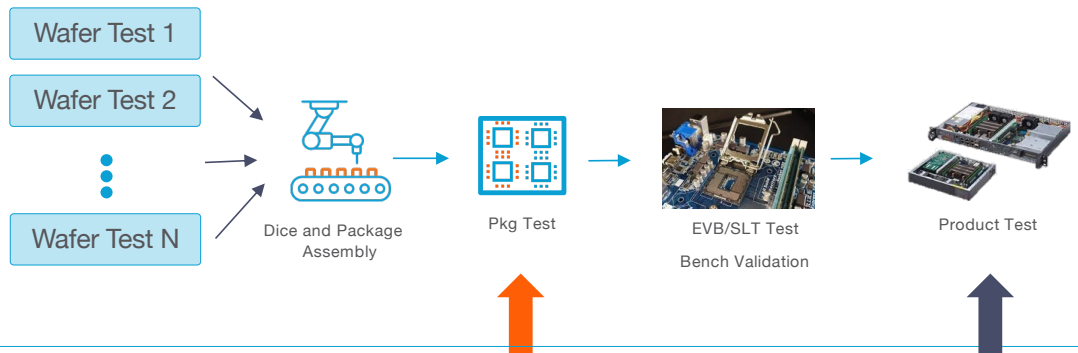
https://www.youtube.com/watch?v=Am0AG6X28FQ

Testing Challenge for Chiplets

System in Package (SiP)



- Interface available at package
- Chiplet



With proteanTecs

Solution deployed at Package testing:

- Provide parametric per-lane assessment
- Enables improved repair with deep data
- Test sequences 100x shorter than conventional approaches at later stage

Value in test coverage improvement:

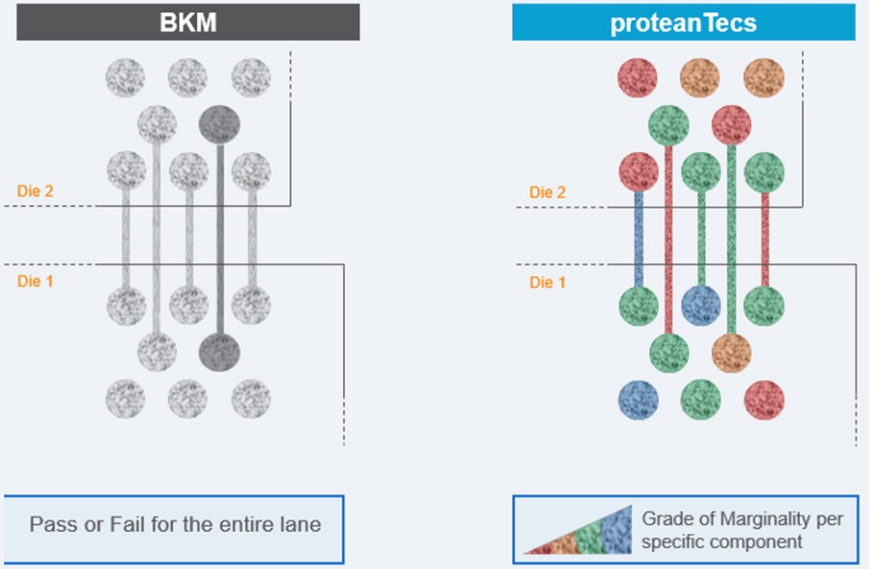
- Shift left with higher resolution testing
- Reduction of RMA by identifying marginal operation and latent defects

Todays Problem:

- 1000's of D2D connections no evaluated until system test
- No test access to D2D interface at SiP
- Existing test method Pass/Fail BIST with long runtime

Enables per-lane parametric visibility

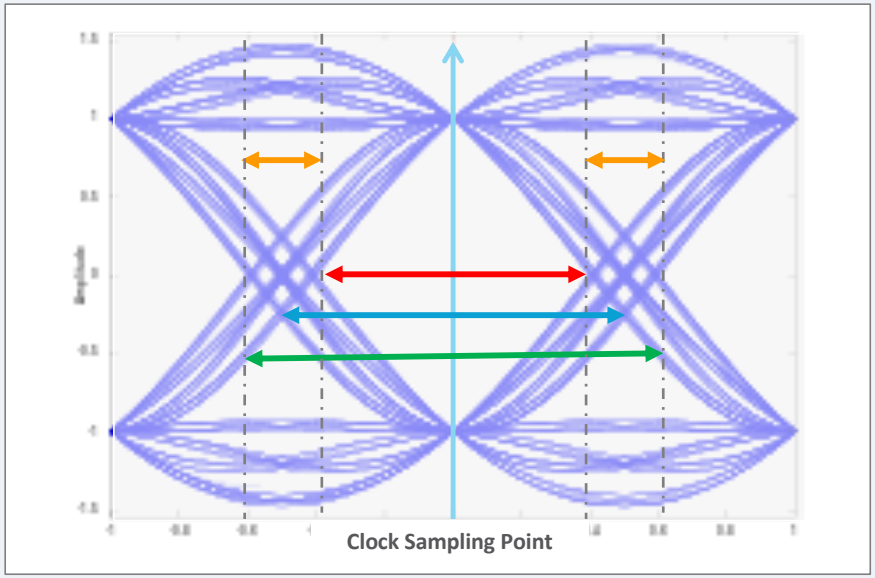
- Comprehensive parametric lane grading
- 100% lane coverage
- Monitors the eye width and jitter
  - During test and **in-mission**
  - While the devices are at **normal operation**
- SW Platform solution with data analytics capabilities
  - Characterization & Qualification
  - HVM @ATE
  - System HVM
  - In mission
- Patent protected



- **Complementary to proteanTecs comprehensive chip performance and health monitoring solutions**

Parametric Lane Grading

- Parameters of lanes are compared across the interface to determine Lane Grading
- TCA performs measurement at a single-lane level
- Measurement dynamic range and step resolution are configurable
- *Combination of measured and calculated parameters*



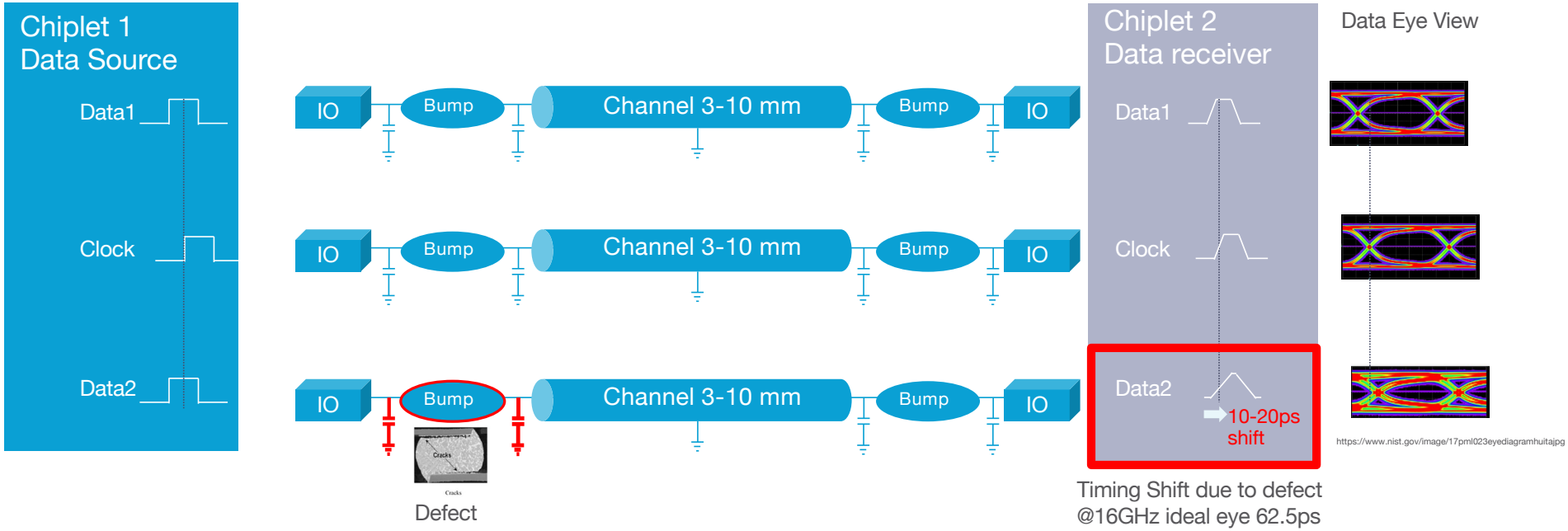
Measured Margin Setup and Hold time

Maximum Minimum Average

Calculated Eye width crossing jitter:

Latent Defect on D2D

Example: 16 Gbps lane operation
Defect will get worse with thermal/electrical stress where eye closes further



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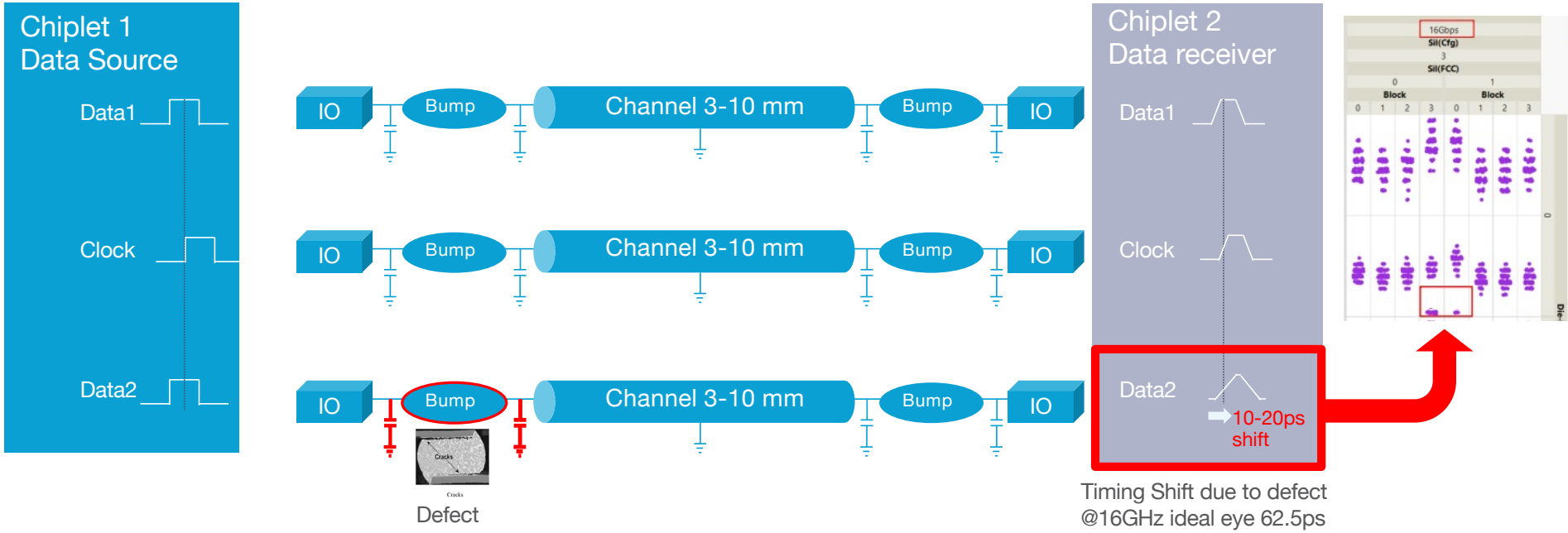
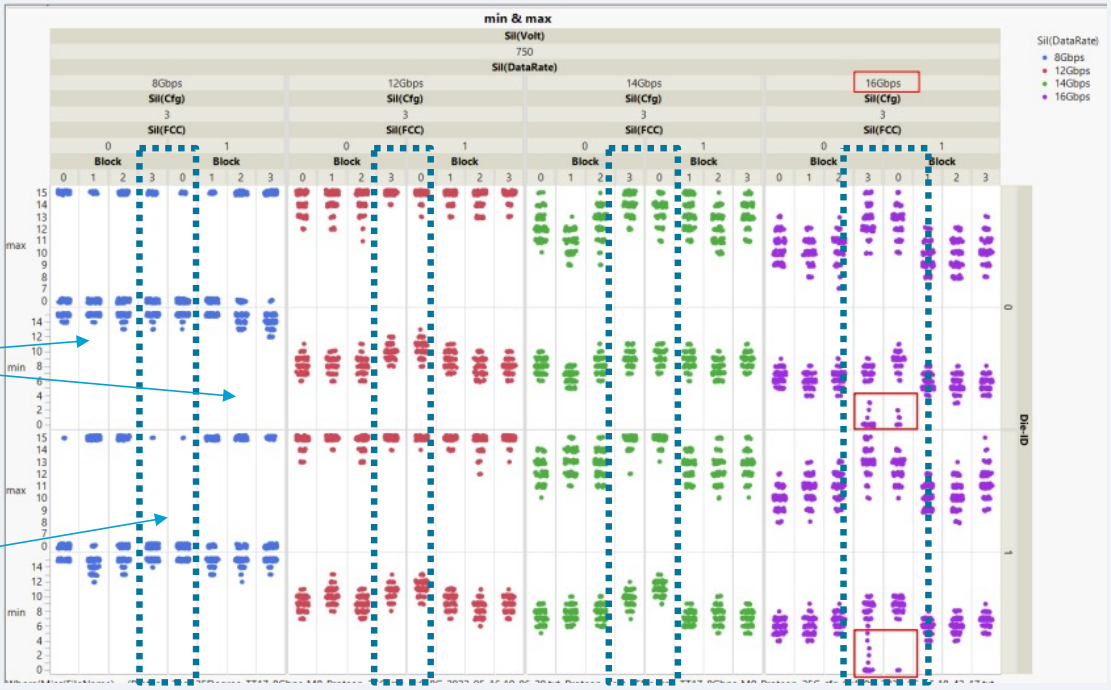


Timing Shift due to defect
@16GHz ideal eye 62.5ps

proteanTecs Agent + analytics enables ps level measurement and insights on device aging

Characterization results:
Implementation Comparison

- Compare implementations
- Sensitive, in-line measurements
  - Per speed
  - Per PVT

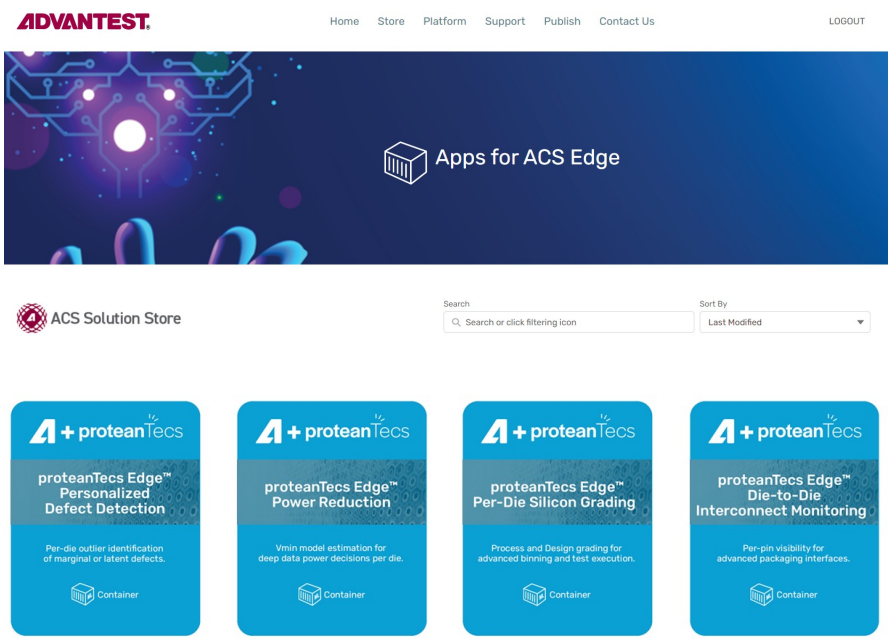


- **Design of experiment showed that ”default design” had better performance at 16Gbps in red boxes**

Deploying D2D insights into ATE

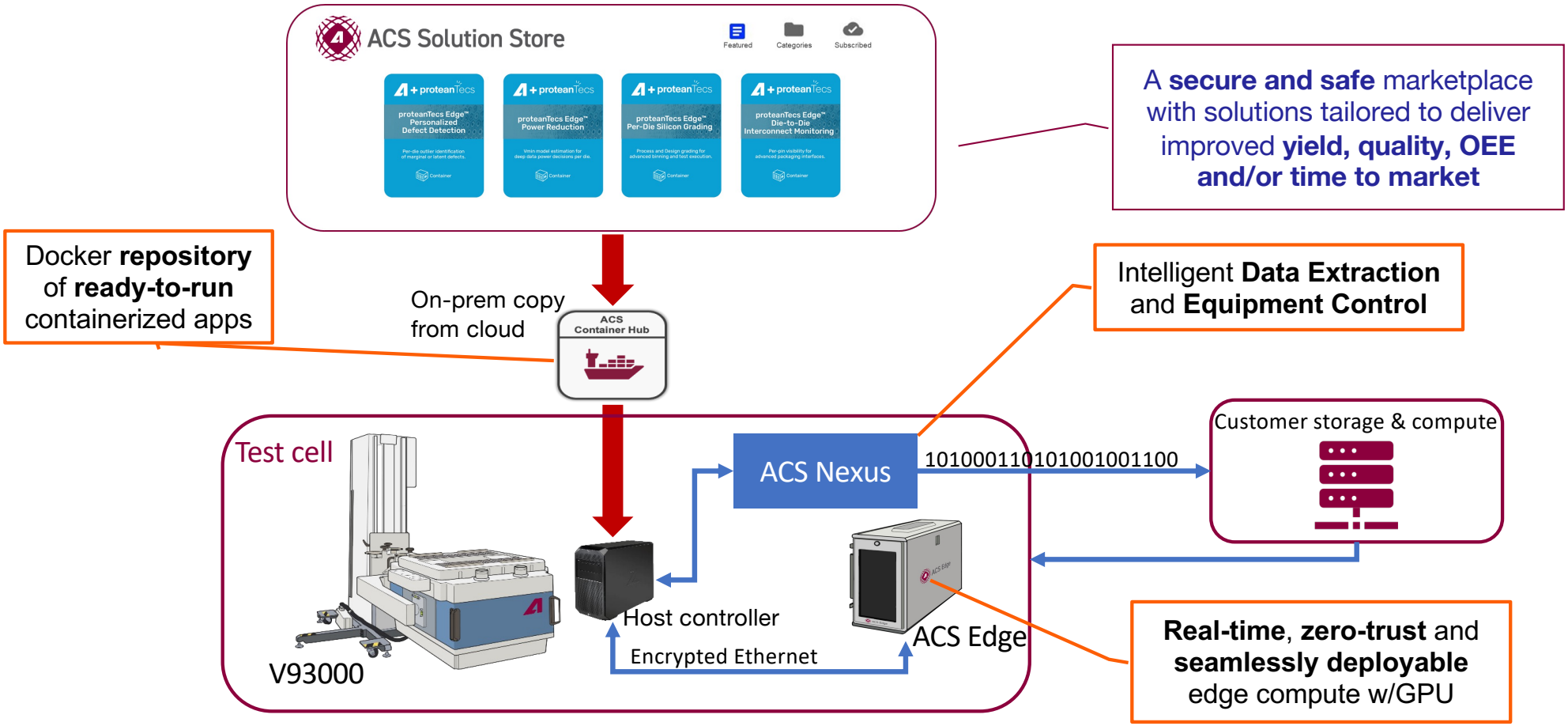
ACS Solution Store – An Open Solutions Ecosystem

- Online marketplace for applications from multiple partners
- Usable for adaptive test, outlier screening, others
- User manuals, app notes, data sheets
- More partners and applications being added continuously



http://acs.advantest.com

Deploying D2D Test Into Production on ACS Real-Time Data Infrastructure



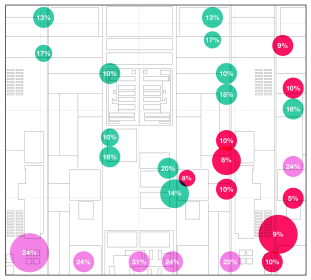
A Short List of Analytics Use Cases

Category	Use Case	Benefit
Outlier detection	Dynamic part average test at package	Quality, reliability
	Univariate, multivariate outliers	Quality, reliability
Adaptive test	Adaptive scan-based diagnostics	Yield
	Adaptive test time reduction	Test cost, quality
	Adaptive test flow (test or sensor data)	Test cost
Inferencing	Shift left of tests	Test cost, throughput
	Real-time predictive modeling	Test cost, throughput
	Stuck part detection	Quality, throughput
Speed up test computation	RF demodulation	Test cost, yield, quality
	RF digital predistortion	Test cost, yield, quality

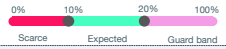
proteanTecs Integrations with Advantest

proteanTecs Proteus Analytics

- Direct measurement
- Local for millions of paths
- Grading
- At test & in mission mode



Timing margin
vs clock cycle time



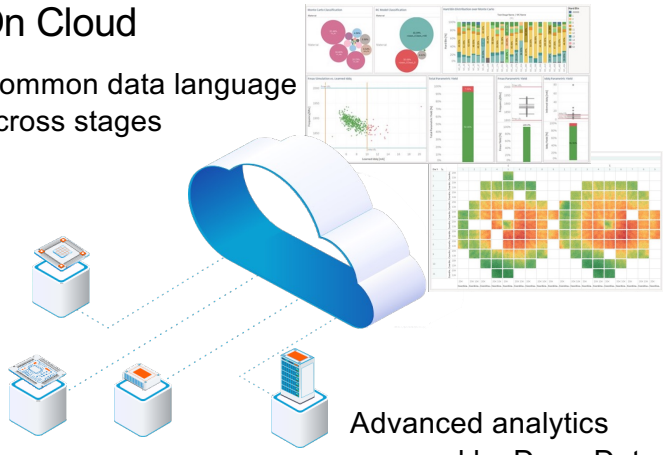
DUT

ACS Solution Store

ACS Edge + Solution Store

On Cloud

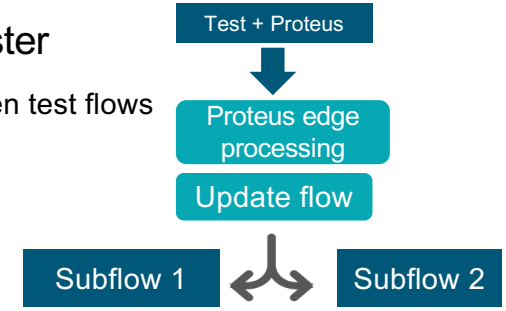
Common data language
across stages



Advanced analytics
powered by Deep Data

On Tester

ML driven test flows



Containerization of proteanTecs Functions

Tester running Smartest

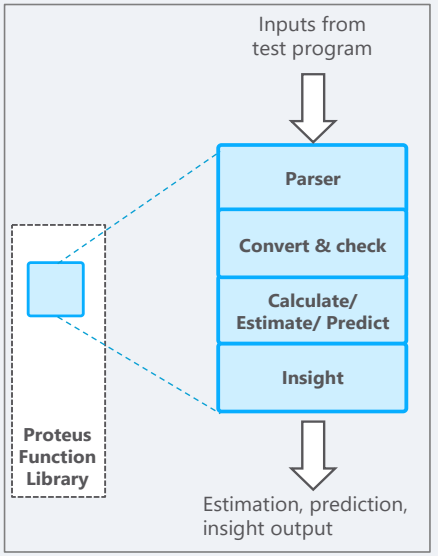
Data to container

Chip ID
Site ID
Agent config
Agent Data
Computation request

Insights from Container

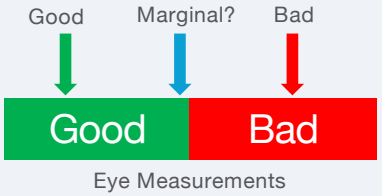
Runtime information
Insight generated

Applications
- Per-die silicon grading
- Personalized defect detection
- Power reduction

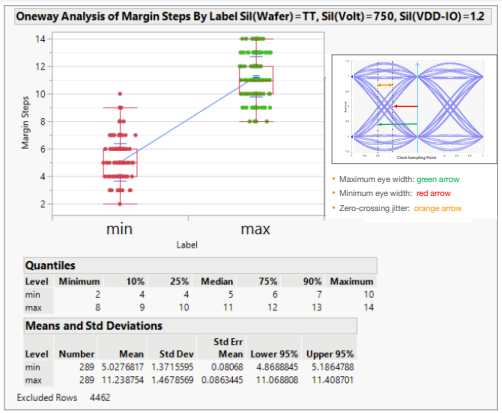


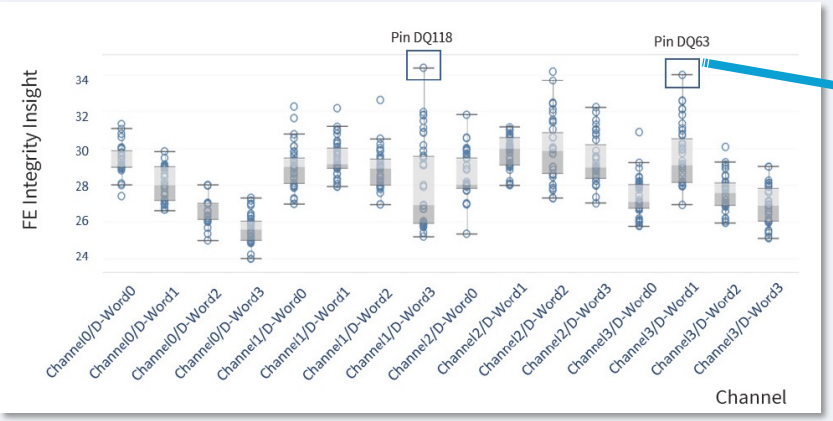
Deep Data Lane Repair

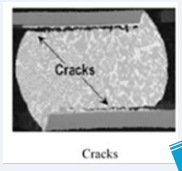
Today Repair based on P/F functional test limiting visibility of robustness of repair

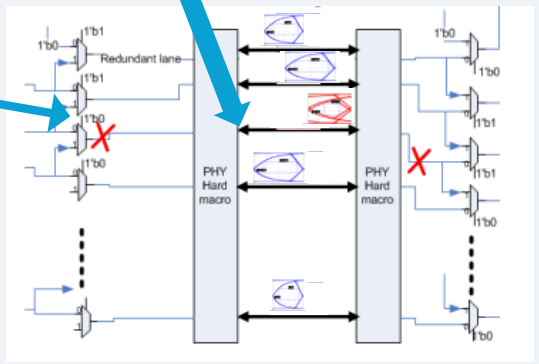


- Deep Data driven for parametric understanding of eye characteristics
- Enables lane shift and IO control repairs
- Diagnose fabrication and assembly faults
- Maximizes for peak operation –margin, performance, power,









Die-to-Die Applications Supported

Yield Learning

- Per-lane parametric eye-width grading assessment including max, min, average and jitter
- Advanced characterization of eye parameters across manufacturing variability, speed grades, temperature and voltage

High Volume Manufacturing

- Outlier detection across lanes and pin group, across full population, reducing risk of RMAs
- Improved yield and test time by quickly and easily identifying weak lanes as candidates for spare lane swap during FT
- Improved repair algorithms for testing and aging in field
- Advanced alerts due to interconnect faults

Conclusions

- Die to Die interface testing is vital for enabling System In Package applications
- Provides new level of device level visibility at Package
- Combining Agents, machine learning and analytics have enabled diagnosis of latent defects
- Additional benefit can be realized with Advantest ACS and proteanTecs Functions

proteanTecs
Electronics visibility. From within

ADVANTEST

iMAPS

Thank You