

# Universal Chiplet Interconnect Express (UCIe $\Gamma$ )

*Building an open ecosystem of chiplets  
for on -package innovations*



# Moore Predicted “Day of Reckoning”

*“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”\**

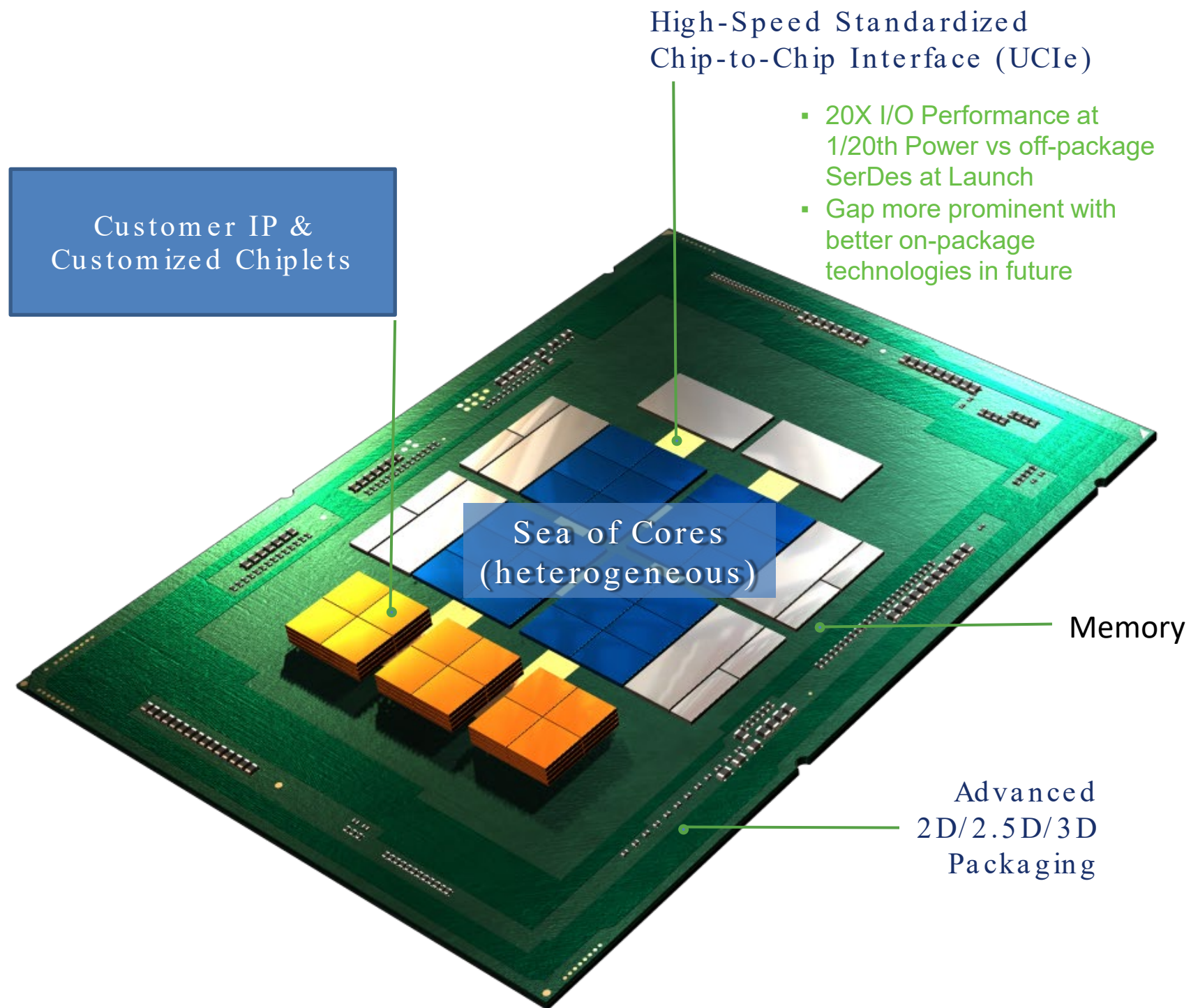
*- Gordon E. Moore*

\*[“Cramming more components onto integrated circuits,”](#) Electronics, Volume 38, Number 8, April 19, 1965



# Motivation

## OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem  
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

## Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)

# Key Metrics and Adoption Criteria

UCle - Architected and specified from the ground -up to deliver the best KPIs while meeting wide adoption criteria

## Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+ Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost
  - Standard vs advanced packaging

## Factors Affecting Wide Adoption

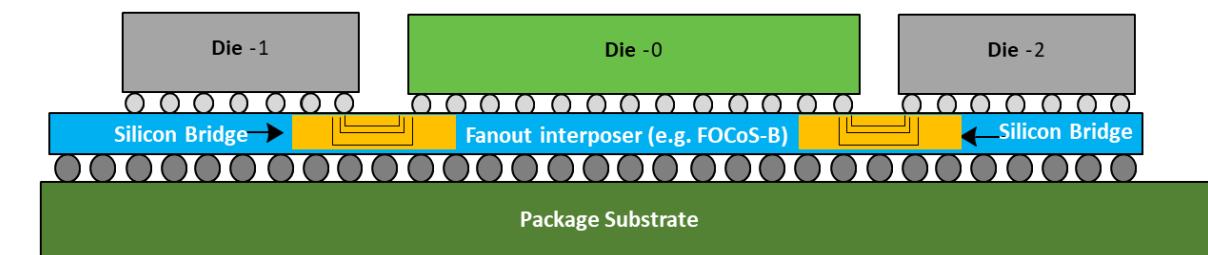
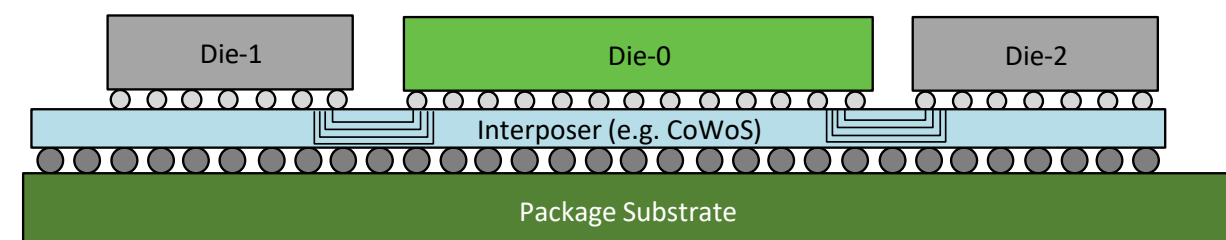
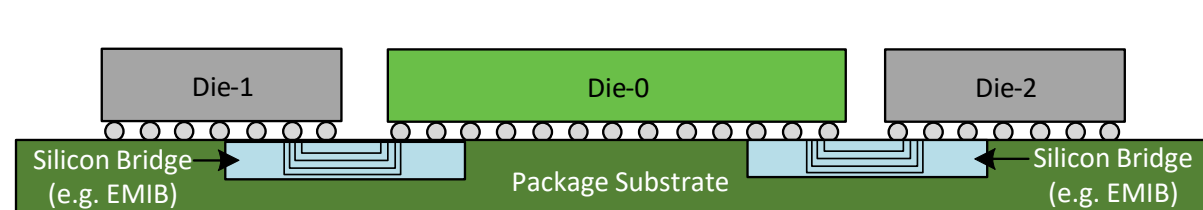
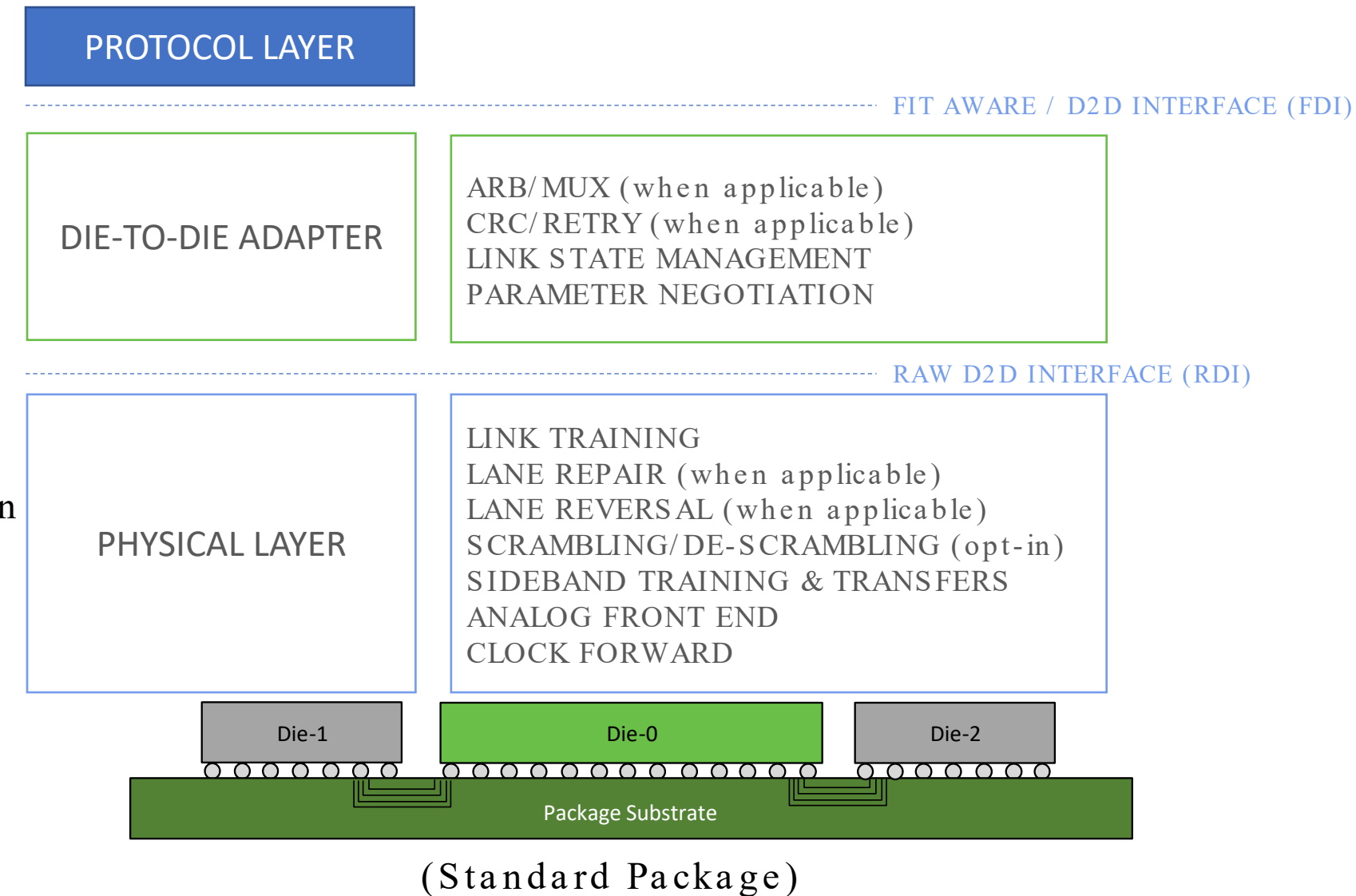
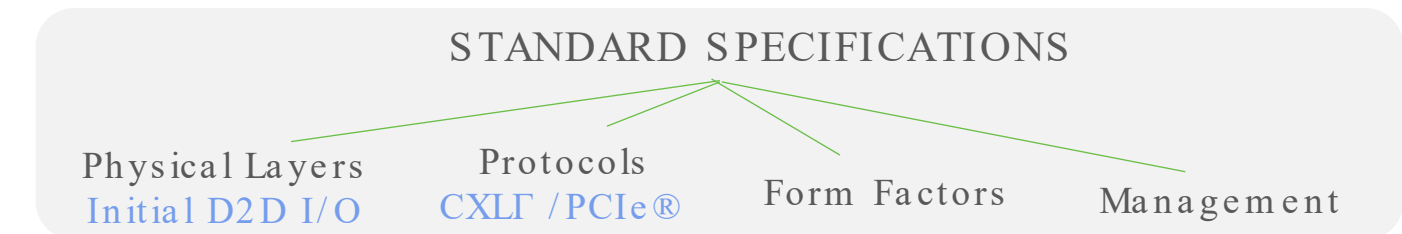
- Interoperability
  - Full-stack, plug-and-play with existing s/w is+
  - Different usages/segments
  - Technology
    - Across process nodes & packaging options
    - Power delivery & cooling
    - Repair strategy (failure/yield improvement)
    - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts



# Jumpstarting UCle

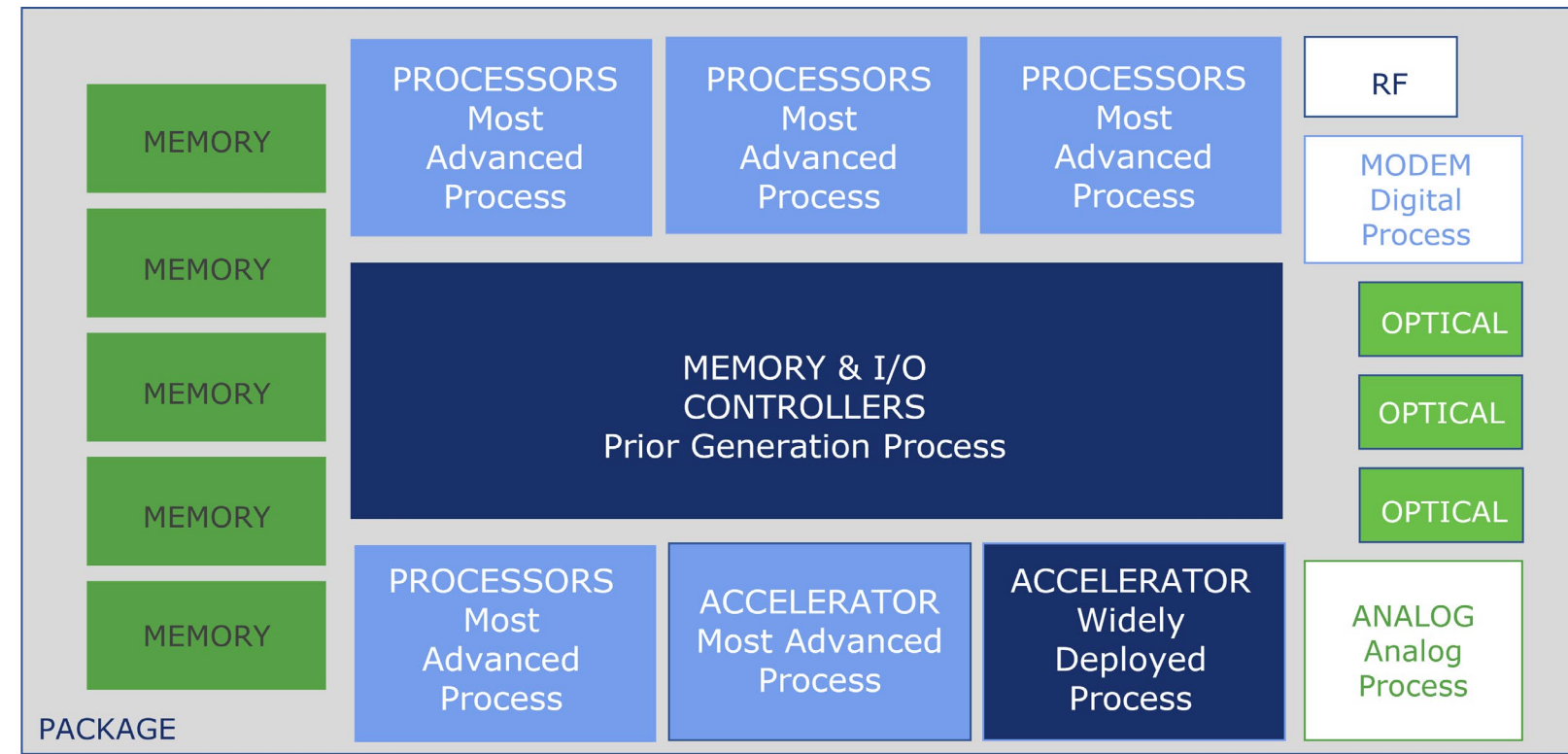
## Intel donates initial specification

- **Focus of UCle 1.0 Specification**
  - **Physical Layer:** Die-to-Die I/O with industry-leading KPIs
  - **Protocol:** CXL / PCIe® for near term volume attach
    - SoC construction issues are addressed since CXL/PCIe is a board-to-board interface
    - CXL/PCIe addresses common use cases
      - I/O attach with PCIe/CXL.io
      - Memory use cases: CXL.mem
      - Accelerator use cases: CXL.cache
  - **Well defined specification** : ensure interoperability and future evolution
- **Future:** the chiplet journey is just starting!!
  - Other protocols
  - Advanced Chiplet form-factors (e.g., 3D)
  - Chiplet management
  - More to come ...



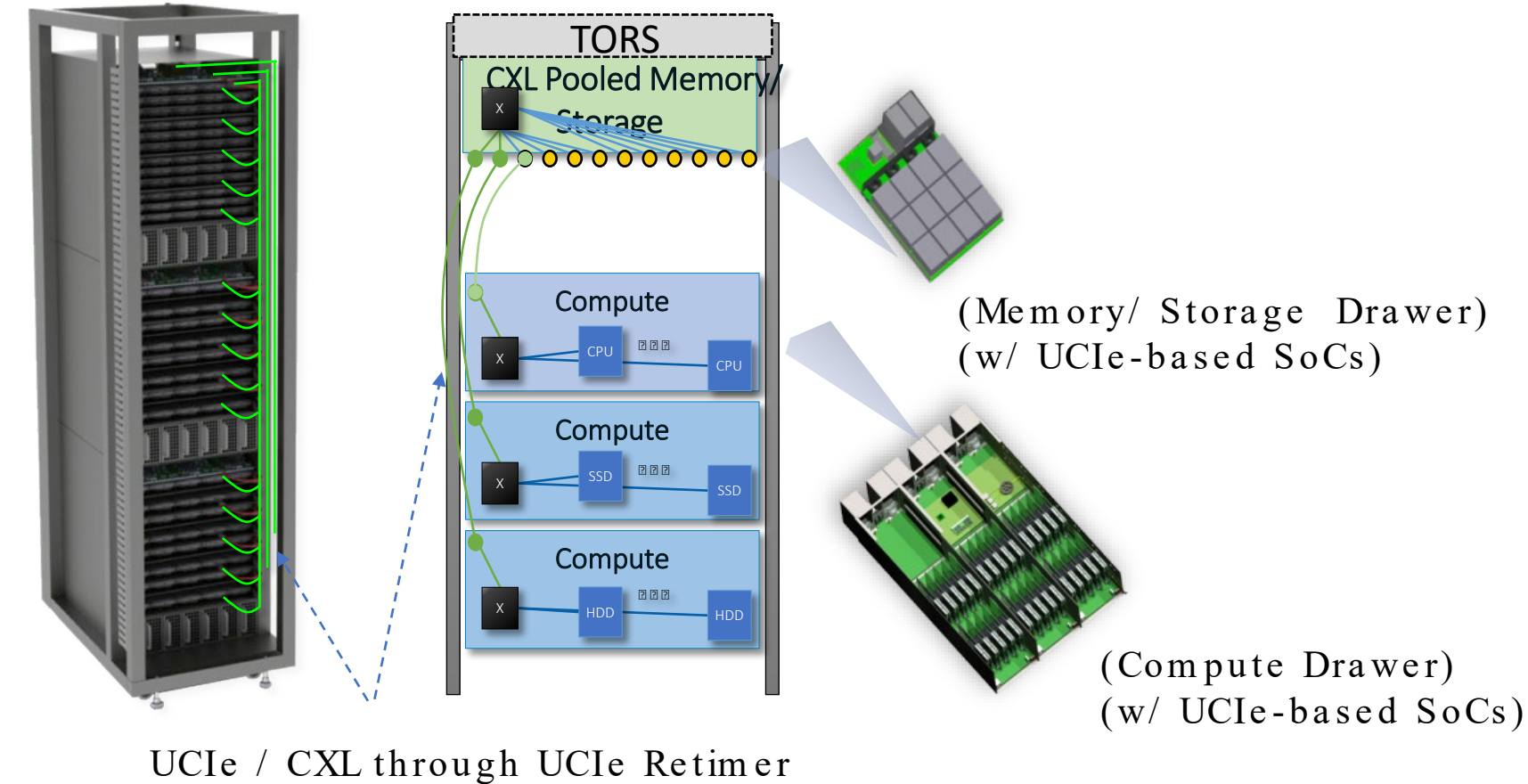
(Multiple Advanced Package Choices)  
(Different flavors of packaging options supported to build an open ecosystem)

# Usage Models Supported by UCIe



SoC Package level construction for wide range of usages from Hand-held to high-end servers

- ✓ Mix and match dies from multiple sources with different packaging options



Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics, electrical cable, mm Wave)

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years. Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.



# UCIe 1.0: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	$\leq 25$	$\leq 2$	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm <sup>2</sup> )	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns $\leq$ 16G, 0.5-1ns $\geq$ 24G		Power savings estimated at $\geq 85\%$
Latency (Tx + Rx)	$< 2$ ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 $<$ FIT (Failure In Time) $\ll 1$		FIT: # failures in a billion hours (expecting $\sim 1E-10$ ) w/ UCIe Flit Mode

# Organizational Update

UCIe Consortium is now **incorporated!**

- 100+ member companies
- 6 working groups working on evolving technology
- Intellectual Property Rights (IPR) protection is in place for members.
- Members include:
  - Adopters: Companies interested in building products
  - Contributors: Companies invested in helping to define future standards (working group participants)
  - Promoters: Board of Directors and leadership





# Summary

- **Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers join forces** to launch new **Universal Chiplet Interconnect Express (UCle)** technology to standardize the chiplet ecosystem today and future generations of chiplet technology.
- **UCle 1.0 Specification** ratified to provide a complete standardized die-to-die interconnect with physical layer, protocol stack, software model, and compliance testing that will enable end users to easily mix and match chiplet components from a multi-vendor ecosystem for System-on-Chip (SoC) construction, including customized SoC.
- **New open standard establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.**
- Interested companies and institutions are encouraged to join. **Learn more, including how to join:** [www.UClexpress.org](http://www.UClexpress.org)

# Thank You

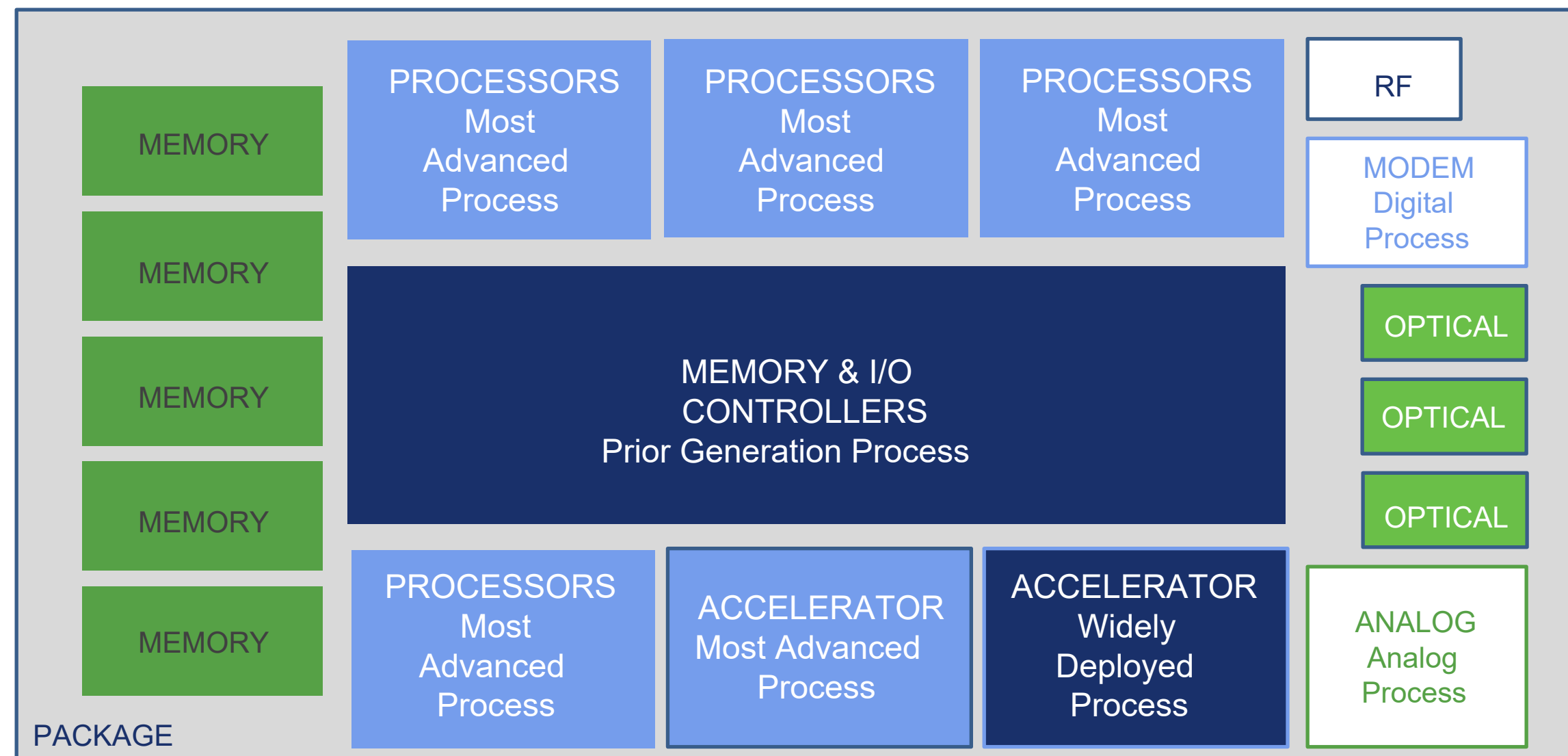
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# Backup Content

# Heterogeneous Integration and Open Chiptlet Ecosystem

SoCs will consist of chiptlets designed, manufactured and assembled by various companies.



Heterogeneous chiptlet integration is the future of the semiconductor industry.