Chiplets Integration: Simplifying the Landscape

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Agenda

1. Chiplet and Heterogeneous Trends
2. Packaging Landscape and Tradeoffs

Compute: Follow the Data

Connected Devices

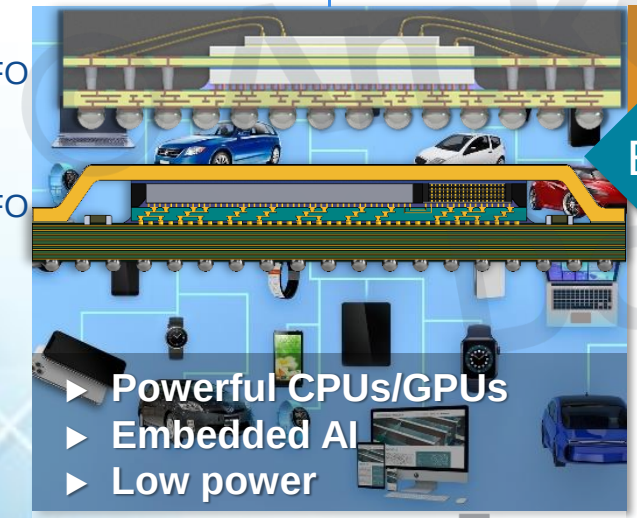
Internet Gateways

Edge IT

Data Centers

HDFO

HDFO



Huge Databases Created

New product constructions required
In both ends of the data spectrum

Data Center: AI Teaching

Embedded Systems

Big Data

3D

Chiplets

2D Modules

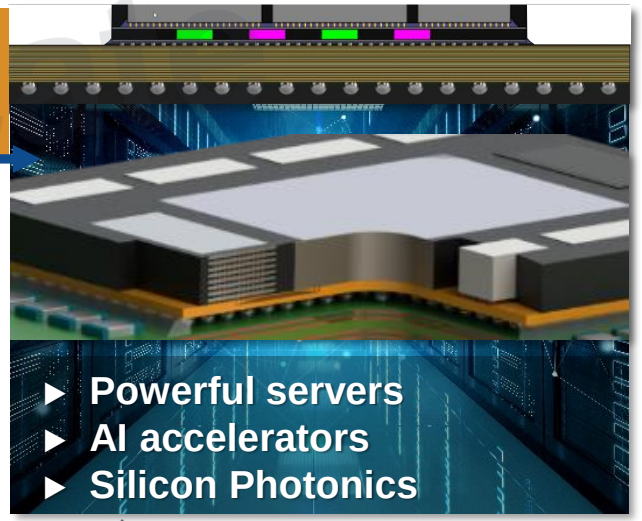
In Pack Memory

HDFO: High Density Fan-Out

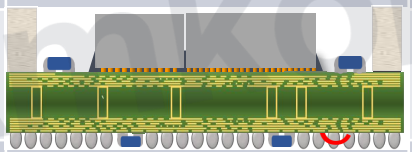
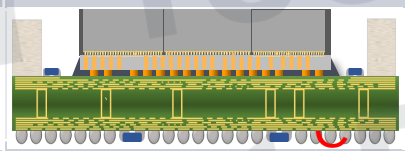
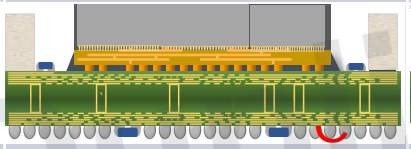
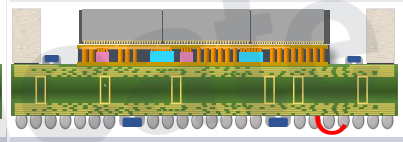
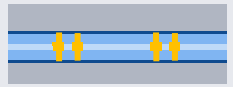
IPDs

Bridges

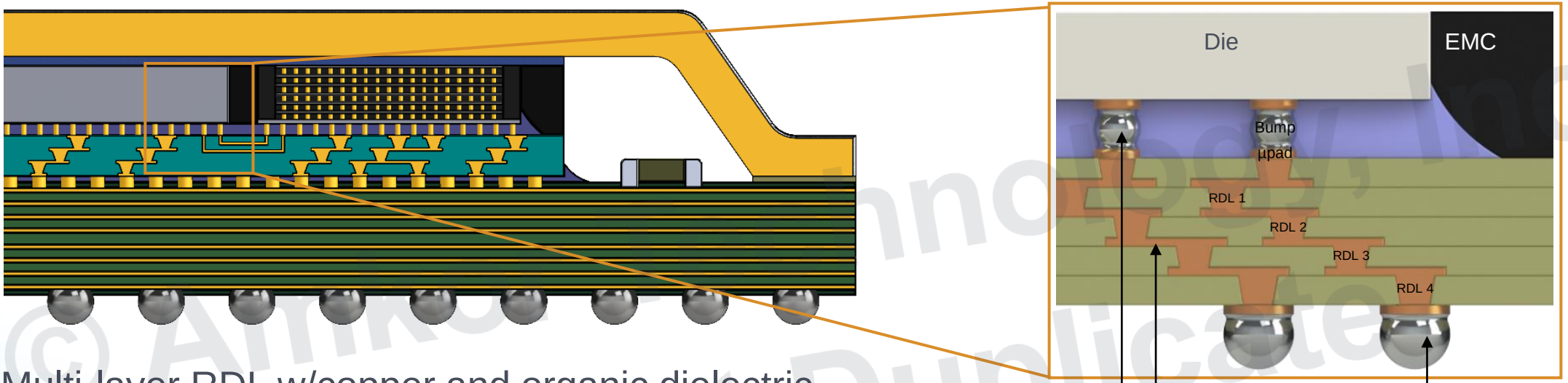
Cu Hybrid



Advanced Packaging Solutions for Chiplets

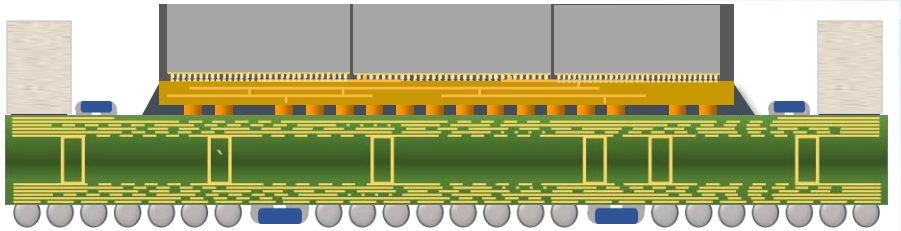
Amkor Packages	FCMCM	2.5D (TSV)	S-SWIFT® HDFO (RDL)	S-Connect HDFO + Bridge Die	3D Stack (Cu Hybrid Bonding)
Status	HVM	HVM	Qualified/ Customer projects	Development/ Customer projects	Development/Internal
Package structure					
Market	Computing, Automotive	Computing	Computing, mobile	Computing	Computing
Drivers	Multi-die High thermal	Large modules HBM memory	2-10 chiplets Form factors	Large modules Improved PDN	Ultra-fine pitch 3D chiplets

Substrate SWIFT® (S-SWIFT®)



- Multi-layer RDL w/copper and organic dielectric
- Max 6 layer w/2 µm line/space capability
- 3 µm nominal Cu line height
- 3 µm nominal PI between Cu
- Flexible solution
  - Fine pitch support for L1 down to 40 µm pitch
  - Plated Cu pillar or LF solder for L2 bumps

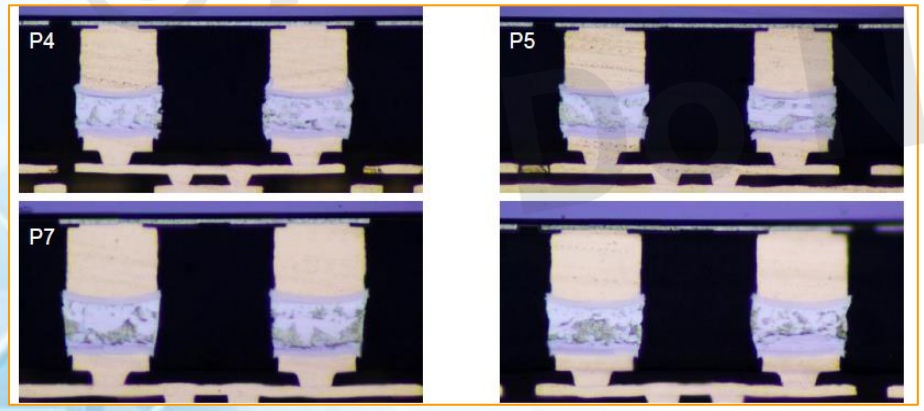
HDFO (S-SWIFT®)



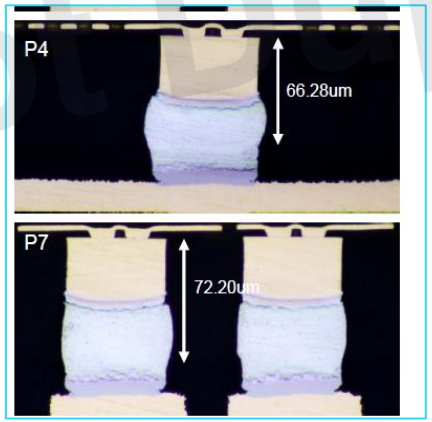
6L RDL Stack, Full Qual Pass

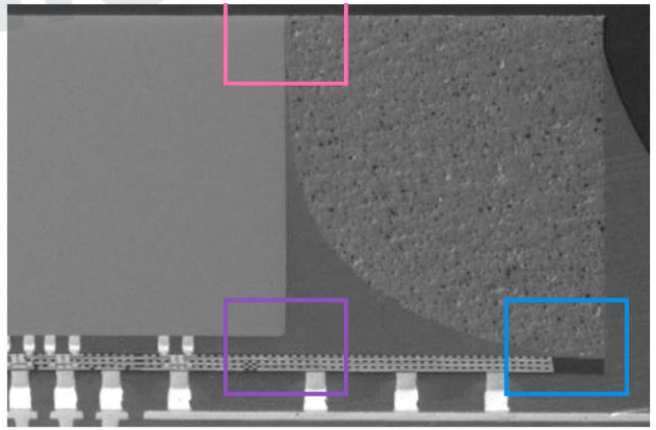
- TC Condition G: 5000x PASS
- **TC Condition B: 5000x PASS**
- uHAST 256 Hrs: PASS
- HTS 1000 Hrs: PASS

- 2022-2023: 4L and 6L Qualified
- 2024: Capacity and Readiness
- 2025: Production



Die to HDFO Cu Pillar

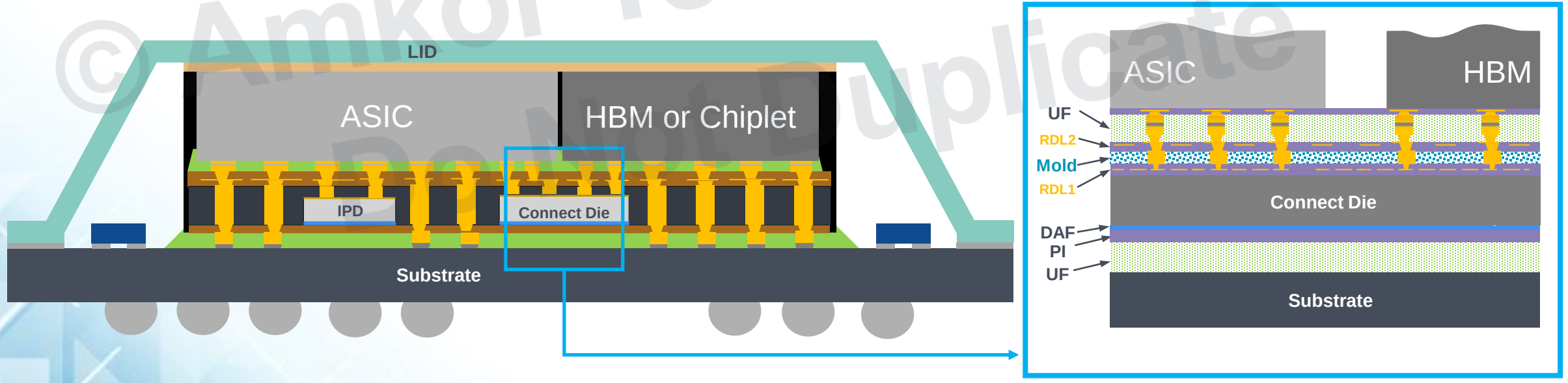




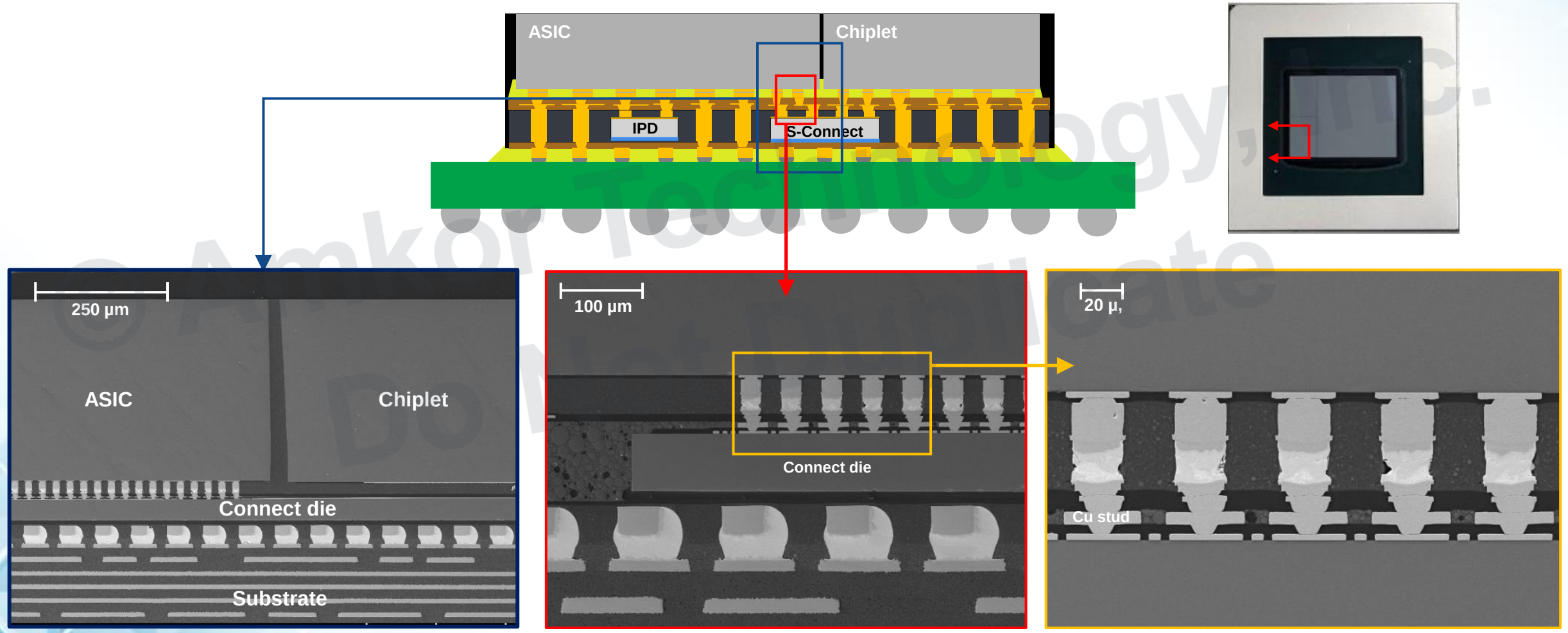
Module to Subst. Cu Pillar

Bridge Technologies (S-Connect)

- Extended technology of SWIFT® and S-SWIFT®
- Bridge technology with embedded silicon connect die for inter-chip connection
- IPD embedment for better power and signal integrity



S-Connect Build Image – TV1



S-Connect (Bridge)

- Platform development ongoing
- Roadmap is customer driven

2022	2023	2024	2025	2026
TV1 reliability Platform development	TV2 qualification	Initial production Qualification 2024	First product ramp	Capacity expansion

Package Construction Tradeoffs

Die-to-Die Interface Requirements

- Total die-to-die BW
- Line speeds
- Latency
- Bump pitches
- L/S
- Layer count

Power Delivery Requirements

- V = Ldi/dt
- Power supply strategy
- Proximity to the die
- Cap locations & value

Module Size Substrate Requirements

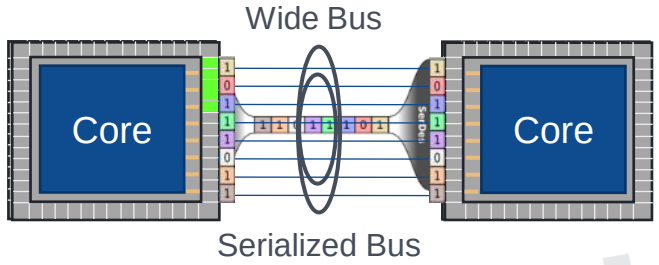
- Number, size and physical configuration of the multiple die
- Module warpage
- Defect density = yield

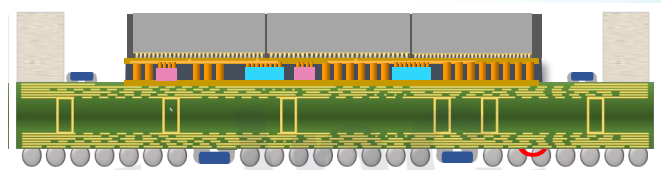
Power Dissipation Requirements

- Operating frequency
- Clocking strategies
- Power density
- Theta J_c

Module Definition

Package Construction Tradeoffs (typical)





Die-to-Die Interface Requirements

- Bump pitches
- L/S
- Layer count

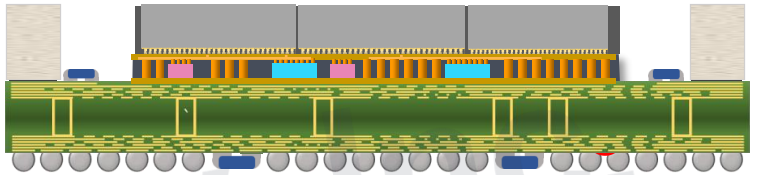
Module Definition

L/S	Bump Pitch	Layer Count	Construction
>10 µm	>100 µm	2 layer	Substrate
1.5-10 µm	30-40 µm	4 layer	RDL
<1.5 µm	<30 µm	6 layer	Silicon
		>6	

Package Construction Tradeoffs

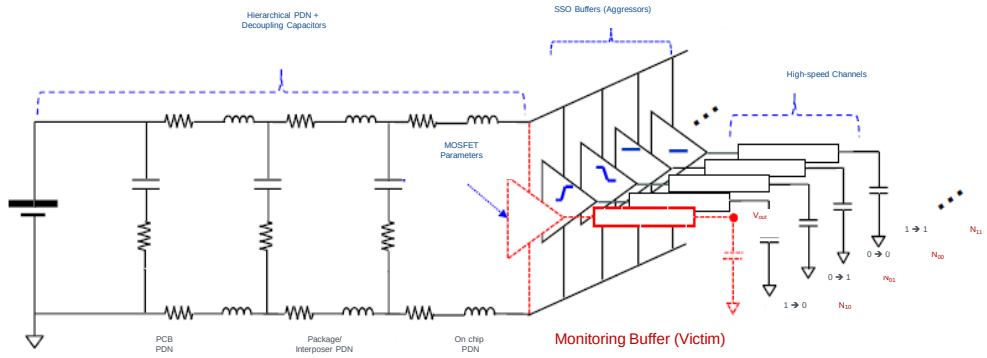
Power Delivery Requirements

- Proximity to the die
- Cap locations & value



Passive Type	Distance to Die Edge	Distance to Die Core	Terminal Pitch	Construction
Ceramic	mm	mm	0.1-1.0 mm	FCBGA
DTC Type	>50 µm	30-50 µm	>100 µm	HDFO (S-SWIFT®)
		10-30 µm	<100 µm	Bridge: S-Connect

Module Definition



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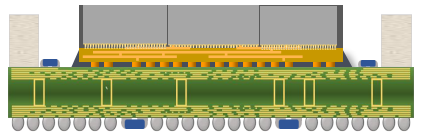
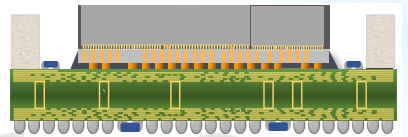
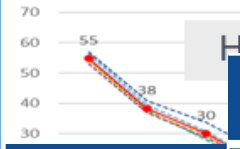
Design Considerations

Module Size Substrate Requirements

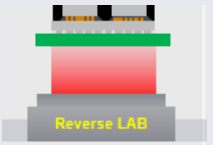
- Module warpage
- Defect density = yield







HDFO Module

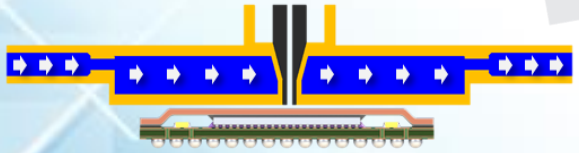
	fcCSP	FCBGA	CoW	BSM SOC	DRAM/ Molded Die	Modules 2.xD	SiP
MR	O	O	O	O	O	Conditional	O
TCB	O	O	Conditional	O	Conditional	X	X
Top LAB	O	O	O	X	X	X	Conditional
Reverse LAB	O	O	O	O	O	O	O
Application	 Silicon chip bonding				 Molded package	 Silicon interposer	 Passive component

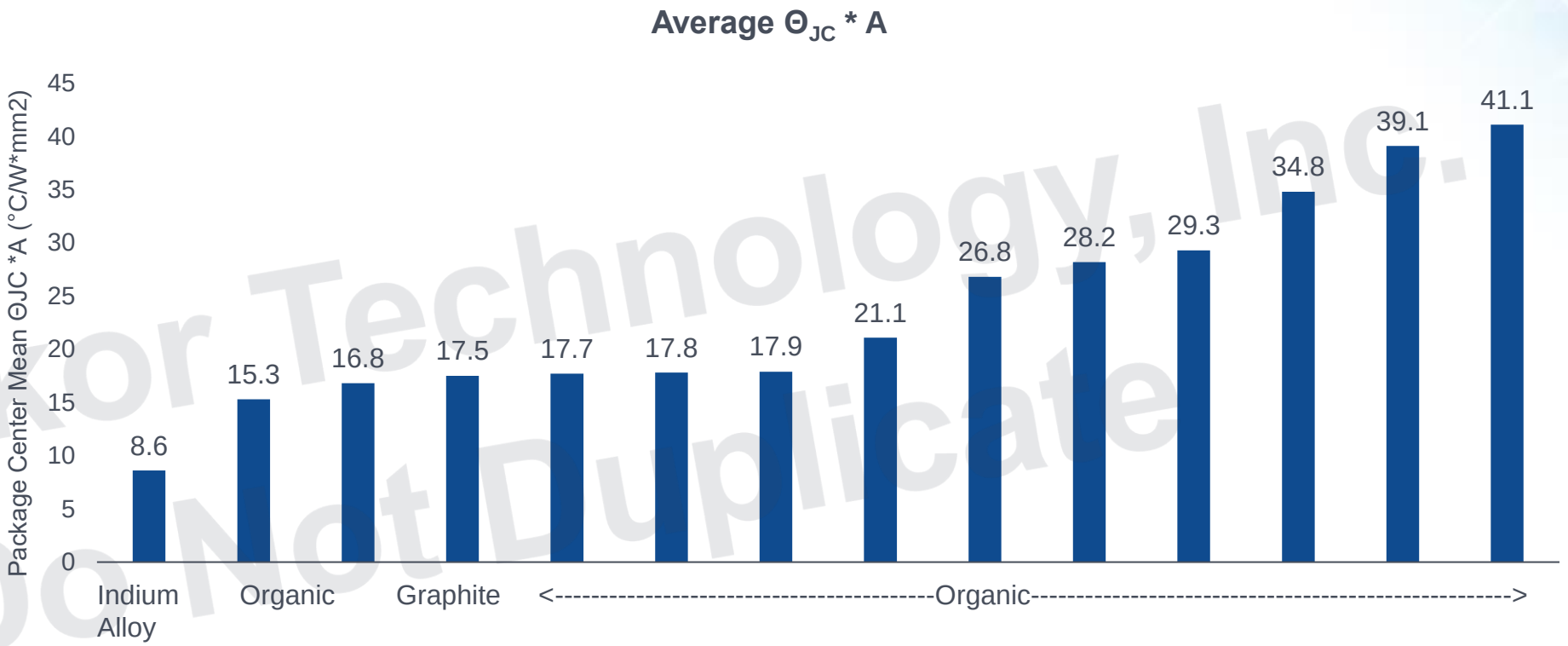
Module Definition

Power Dissipation Requirements

Power Dissipation Requirements

- Power density
- Theta J_c

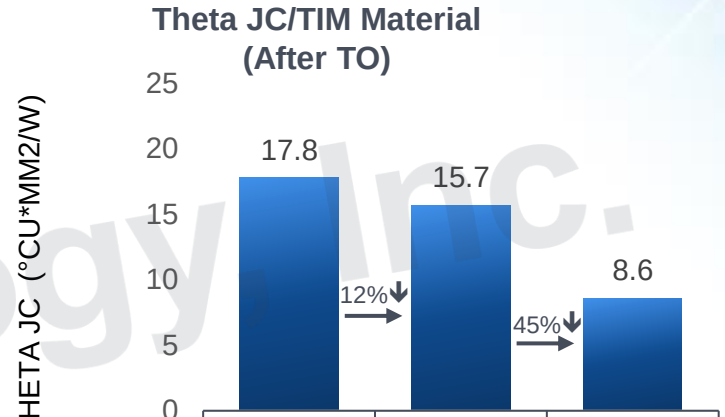




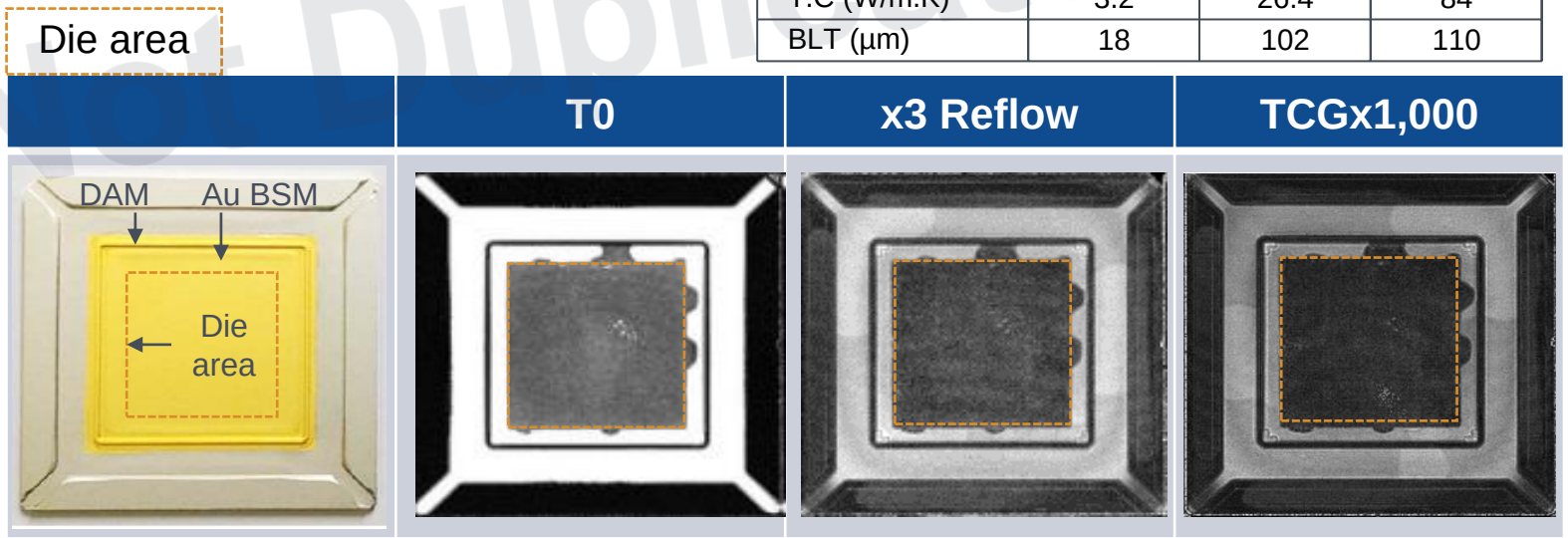
- TV: 60 BD TTV (25.6 x 25.6 mm^2 die)
- Cooling method: Cold plate with water (20°C)
- Center Θ_{JC} results

Amkor Metal TIM Status

- FCLBGA 52.5 mm BD/25.6 x 25.6 mm^2 die
- Process optimization completed
- Internal qualification completed
  - >95% metal TIM coverage after reliability test
- Modules (2.xD) 2023-2024



	SHA1-EL	Graphite TIM	In10Ag
Theta JC (Center)	17.8	15.7	8.6
T.C (W/m.K)	3.2	26.4	84
BLT (µm)	18	102	110



Conclusions

- Chiplets and heterogeneous integrations are here to stay
- These approaches offer many new ways to achieve new product architectures
- Keeps PPAC on track for the future of our industry
- Requires more from advanced IC packaging
- OSATs and Foundries are responding in a logical, straightforward manner to enable this (this despite the plethora of new acronyms)
- 2D module first, augmented by 3D as required for performance and differentiation

Thank You

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