Scaling Interconnect Densities

Meeting the Growing Demand for Chiplet Integration

Robin Davis – Director of Business Development

Tim Olson - CEO

19TH INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
FOUNTAIN HILLS, AZ • WWW.DEVICEPACKAGING.ORG • MARCH 13-16, 2023

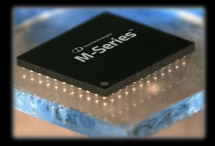
Outline

- Introduction
- Industry Perspective
- Leading Examples
- What’s Next
- Conclusion

Company Introduction

2009 — Initial Funding
CYPRESS EMBEDDED IN TOMORROW™ & SUNPOWER
Founding of Deca USA & Philippines

2013 — Market Intro
M-Series & Adaptive Patterning Introduced

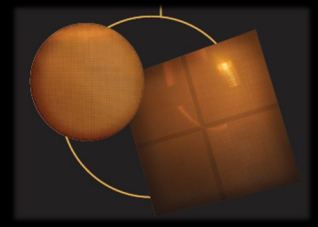


& Adaptive Patterning

2016 — 2nd Funding
Qualcomm & ASE GROUP
Qualcomm Adopts & ASE Becomes 1st TTLA Licensee

2020 — 3rd Funding
Nepes Becomes 2nd TTLA Licensee
nepes

2021 — Industry #1



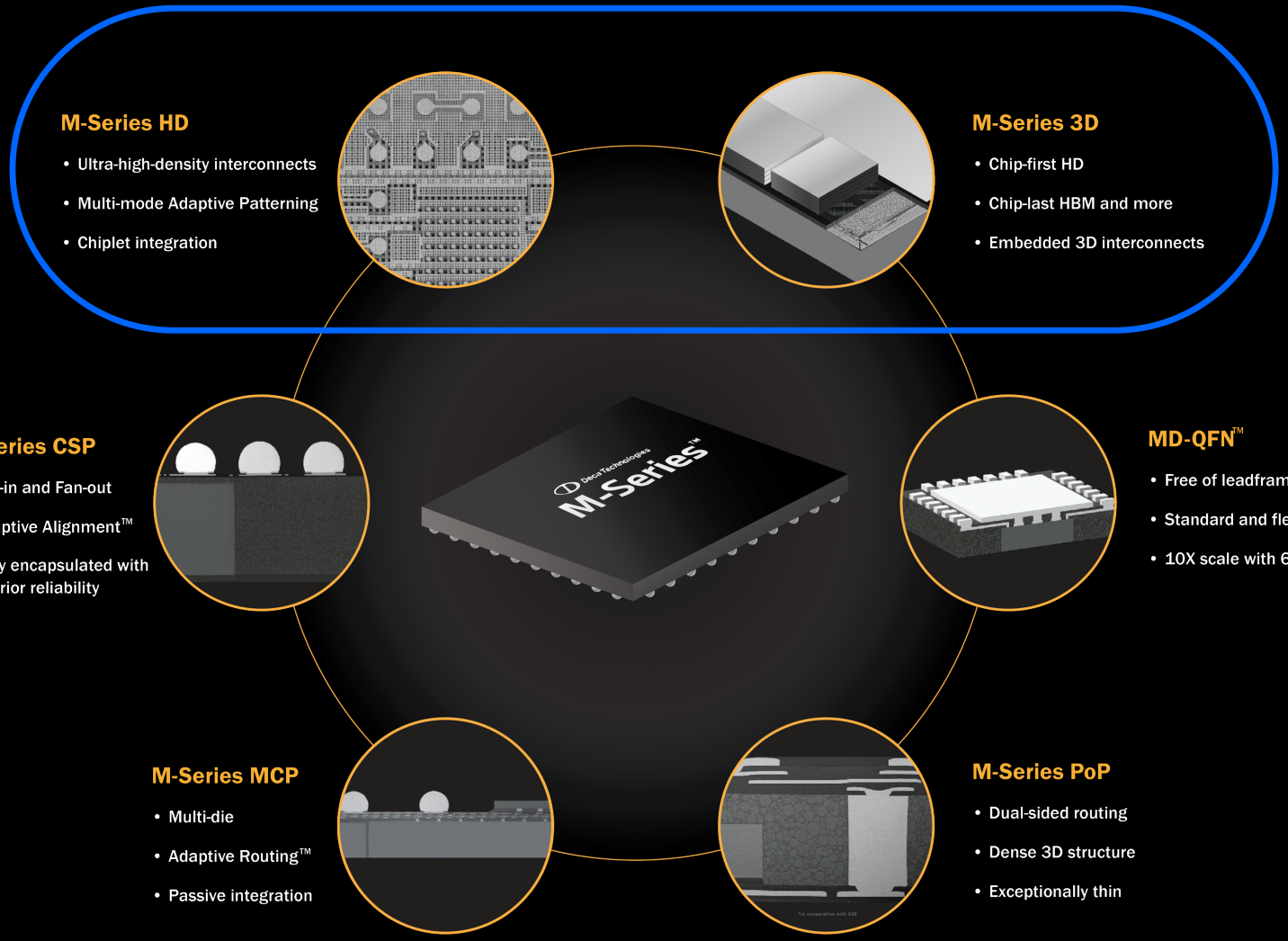
M-Series highest volume fan-out in history

Deca is the #1 independent technology development & licensing company in the advanced packaging industry[1]

[1]*Fan-out WLP & PLP Technologies 2021- Markets & Technology Report, Yole Developpement, June 2021*

DECA Technology Introduction

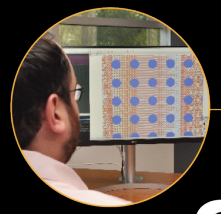
M-Series™



DECA

DECA Technology Introduction

Adaptive Patterning®



STUDIO™

Full designer control

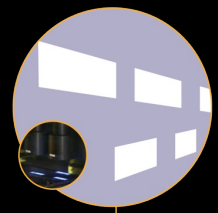
- Deterministic results
- APDKs for leading EDA tools

APDK™

ENGINE™

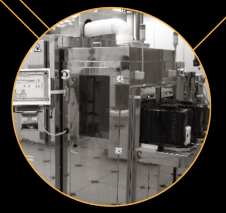
Design-during-manufacturing

- Natural variation removed
- Every device, every wafer or panel



Maskless lithography

- Laser direct imaging
- No reticle limits
- High throughput



CONNECT™

Factory integration

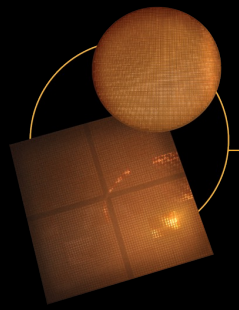
- Connection to fab equipment
- Proven turn-key solutions
- Multiple equipment options

Natural variation captured

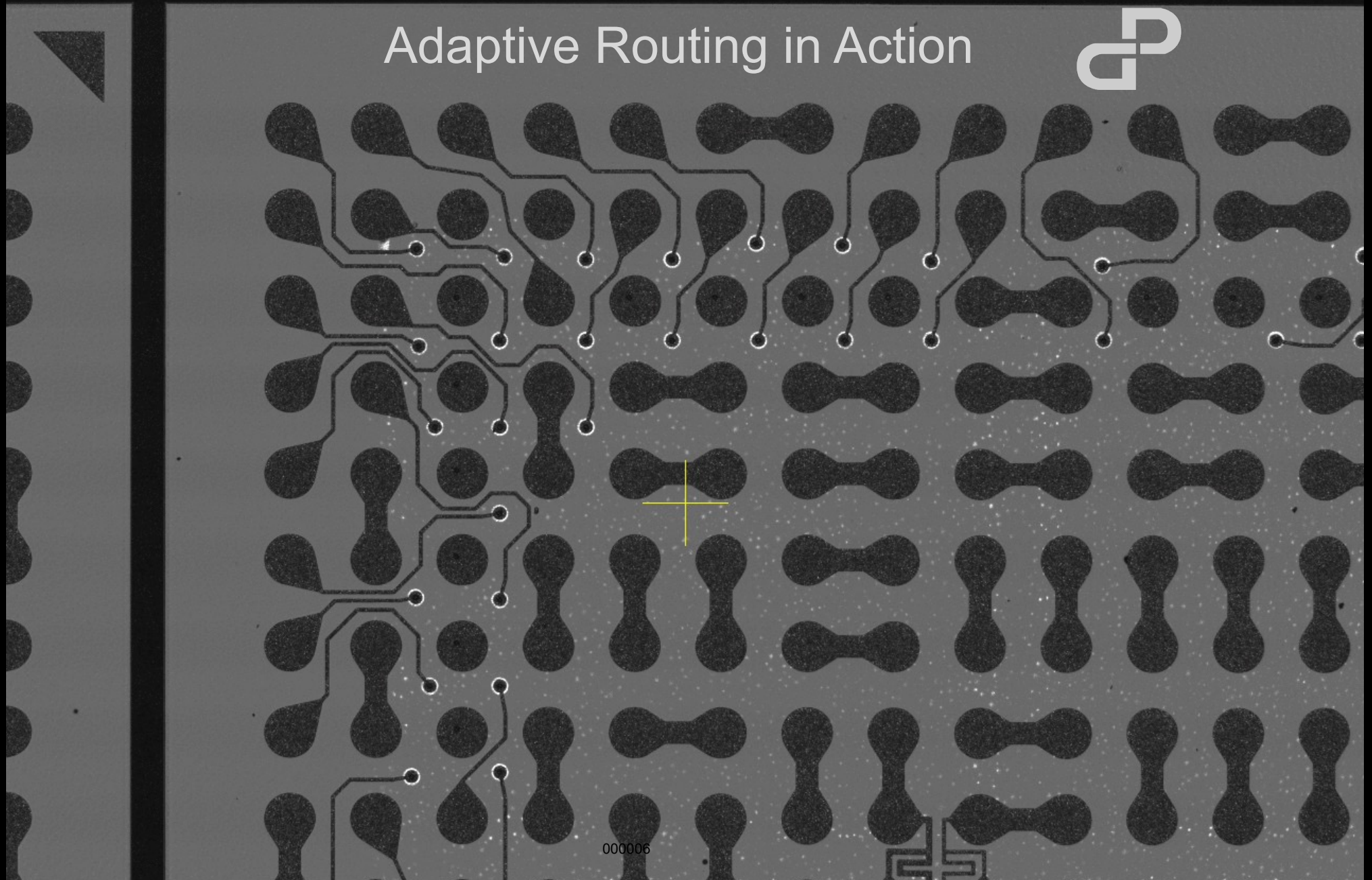
- High speed 100% optical scan
- True position measurement

Flexibility in manufacturing format

- 300mm round
- 600mm square
- Extensible to others



Adaptive Routing in Action



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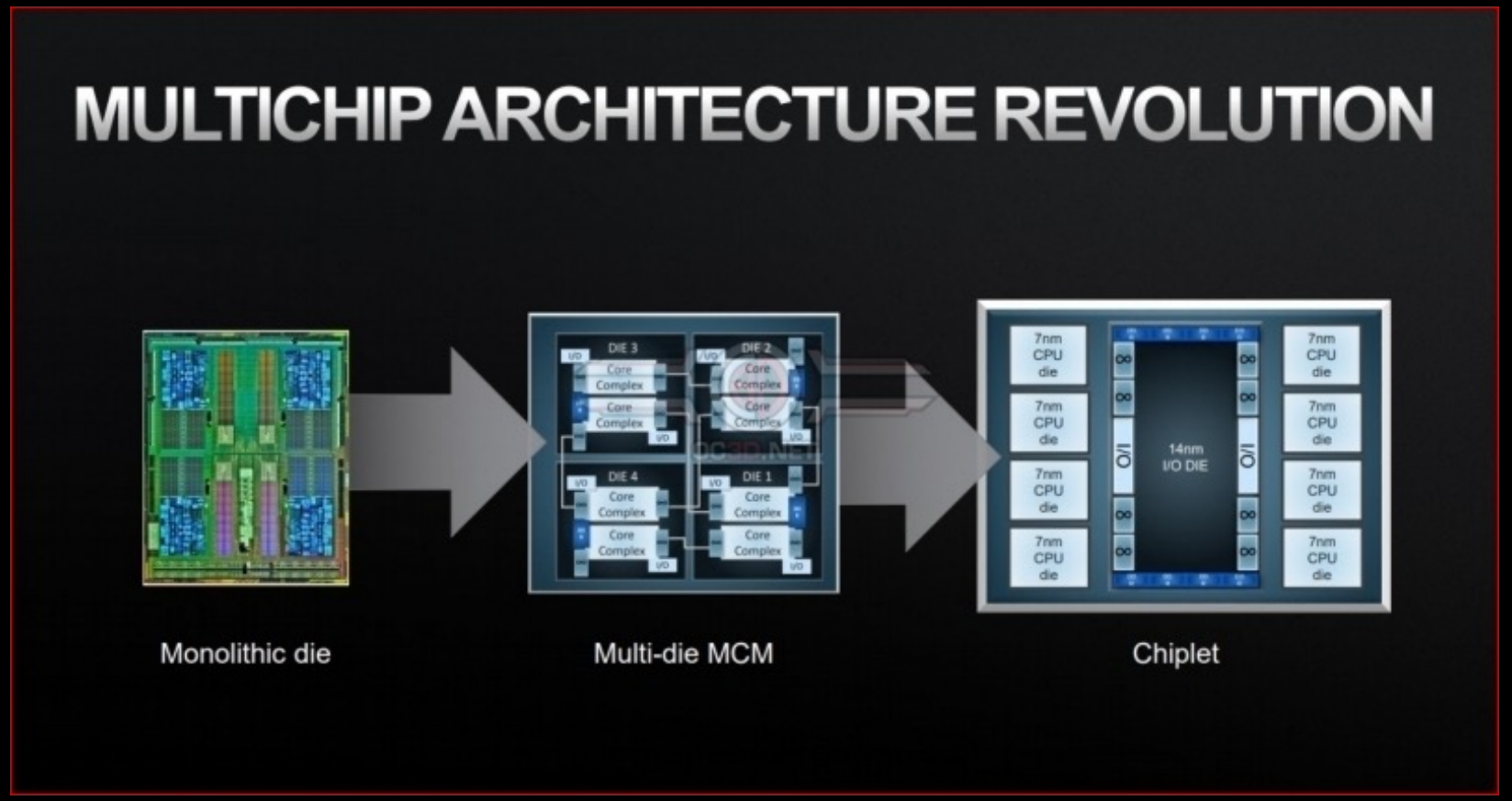
- Industry Perspective
- Leading Examples
- What's Next
- Conclusion

Industry Perspective

Industry leading semiconductor companies are moving on from the monolithic IC invented 60 years



AMD

intel

Qualcomm

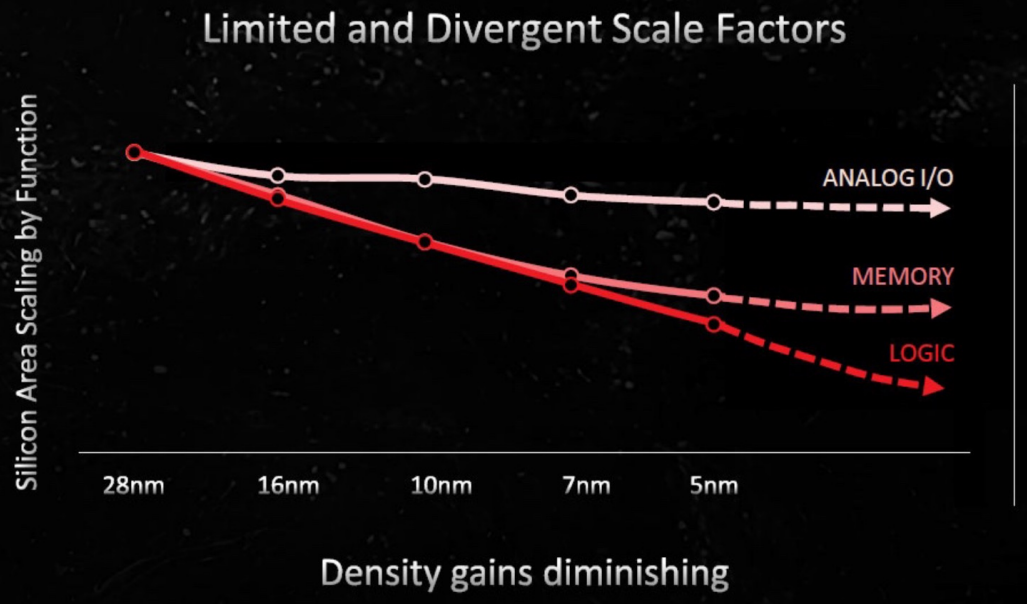
&

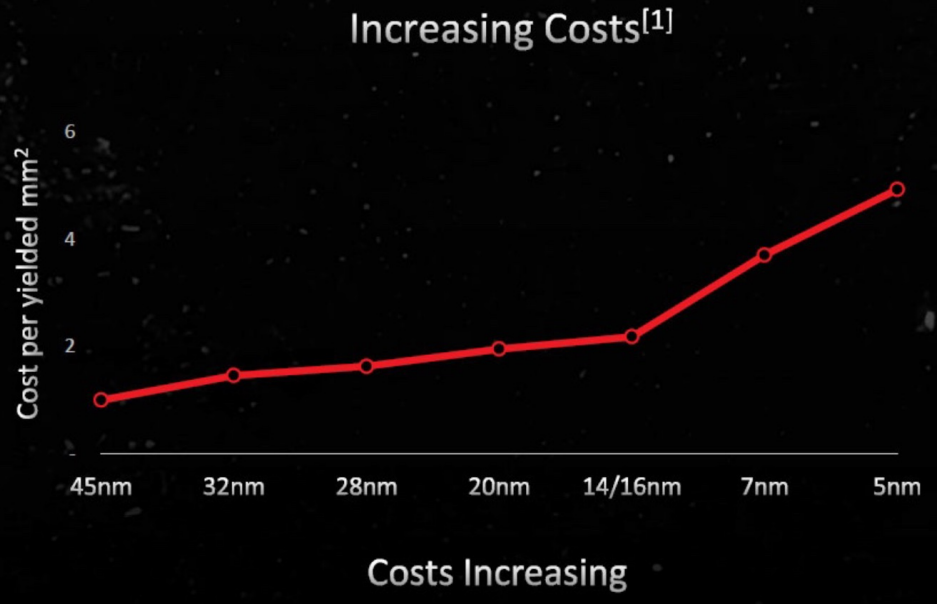
Many more

... to chiplets & heterogeneous integration

Industry Perspective

CHIPLET TECHNOLOGY
OUR MOTIVATION

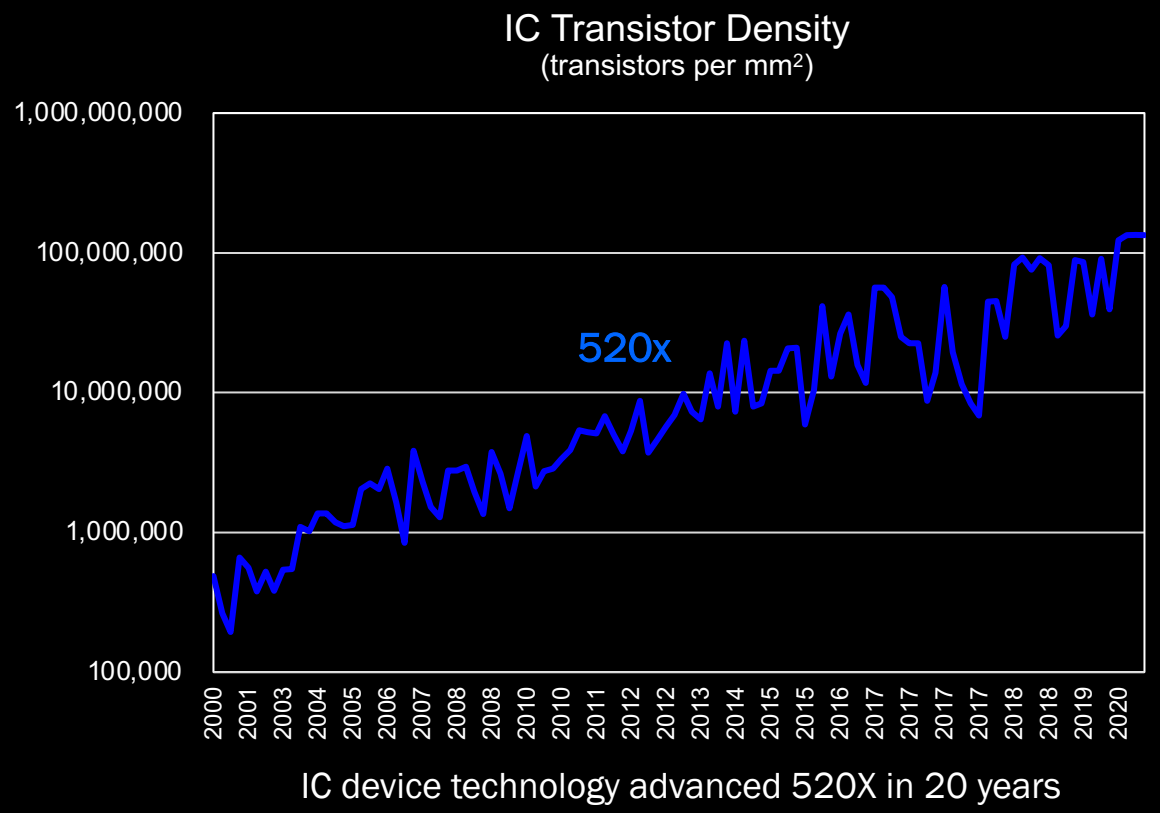




[1] AMD Internally estimated cost per yielded mm2 for a 250mm2 die

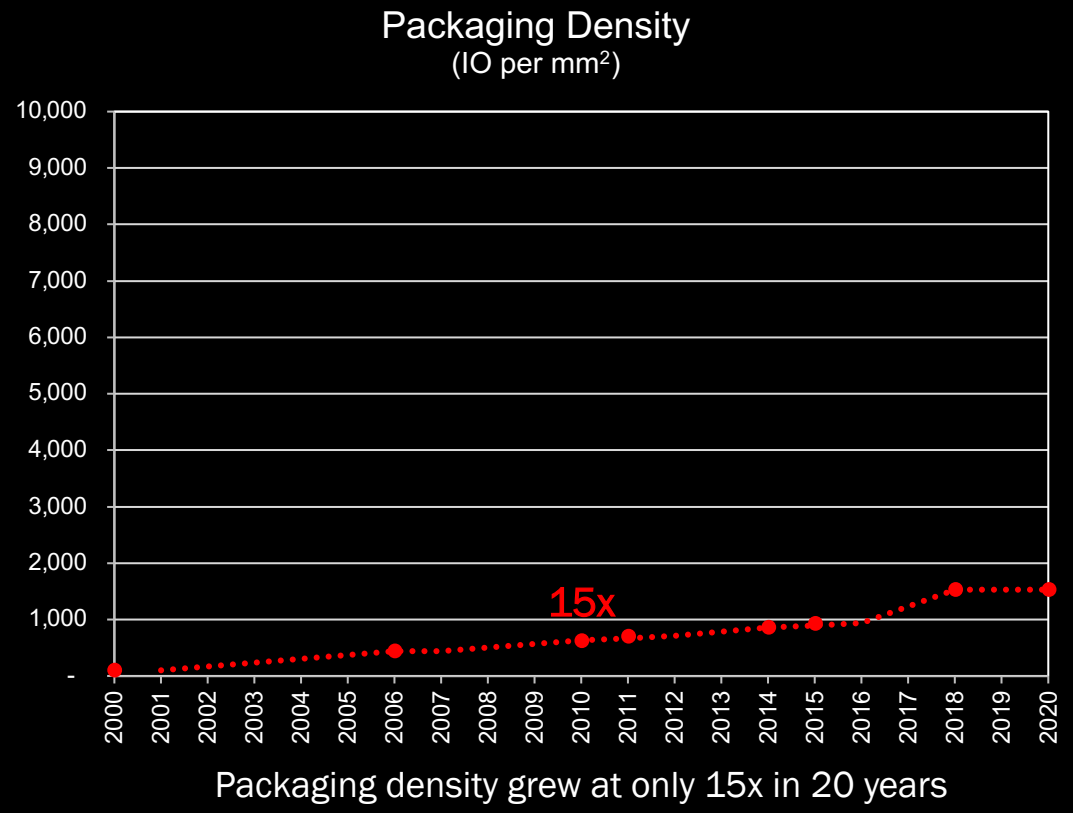
Moore's Law Slowing – Packaging Far Behind

Semiconductor ICs > 500X density increase in past 20 years vs. 15X for packaging



IC device technology advanced 520X in 20 years

Source: Multiple industry sources compiled at en.wikipedia.org/wiki/Transistor_Count



Packaging density grew at only 15x in 20 years

Sources: 1. Chip scale Review: March-April 2020, IO/mm² derived from die pad pitch data
2. Tech Search Intl, Advanced Packaging Update, Vol 2, 2020

Packaging interface density lagging ICs by orders of magnitude

However, some recent breakthroughs have occurred!

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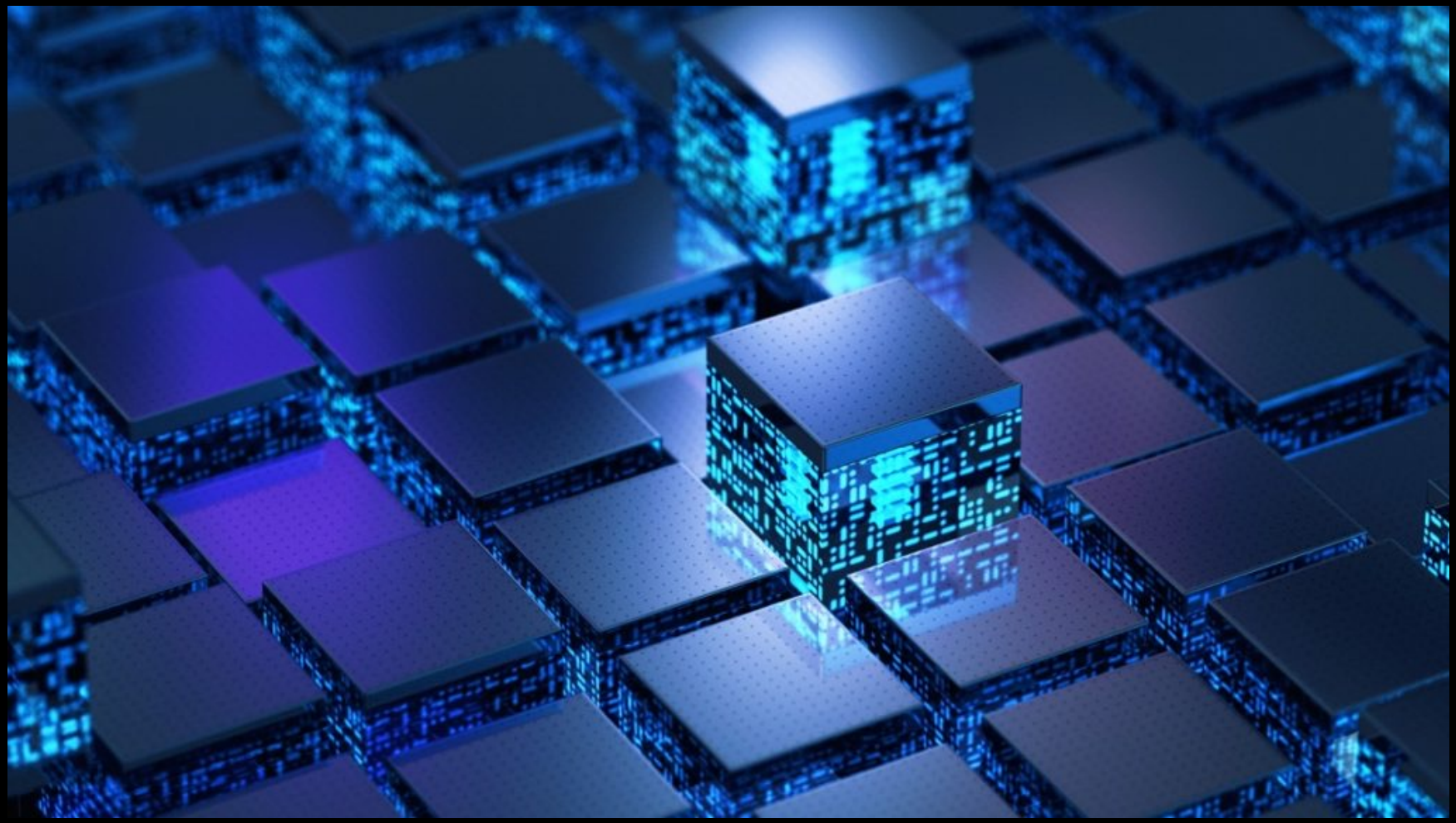
Industry Perspective

How will the industry connect all the chiplets?



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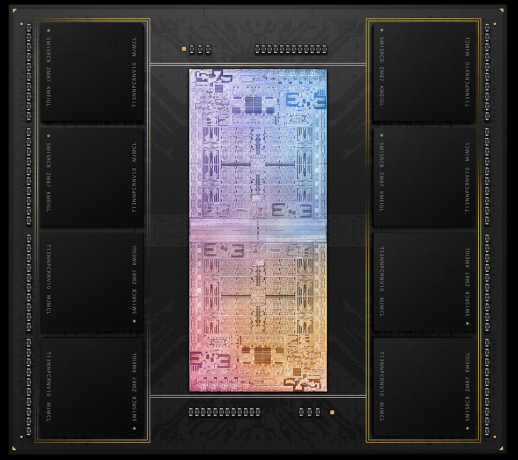
Apple Mac Studio with M1 Ultra Processor – March 2022

M1 Ultra Processor
(Created with advanced packaging)



- Two 5nm M1 Max die, 840mm2 (total both die)
- 64 or 128GB DRAM (total in 8 packages)

The world's most powerful personal computer, over 22 trillion operations per second

DECA

A Look Inside the Apple M1 Ultra

1. M1 Max die-to-die spacing: 110µm
2. M1 Max die A thickness: 587µm
3. InFo-L ball pitch: Variable 100-150µm

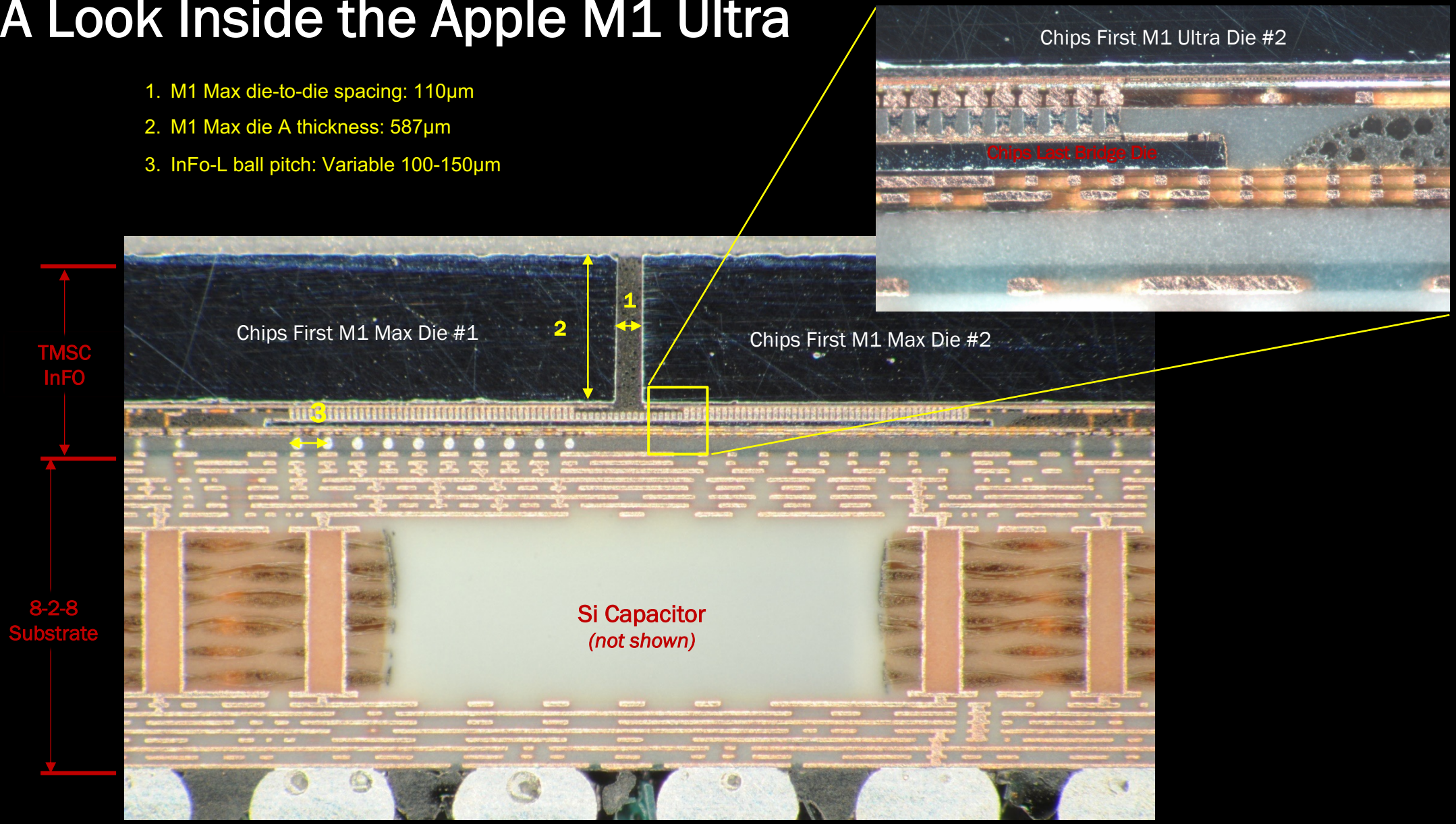


Photo source: Prismark/Binghamton University

A Look Inside the Apple M1 Ultra

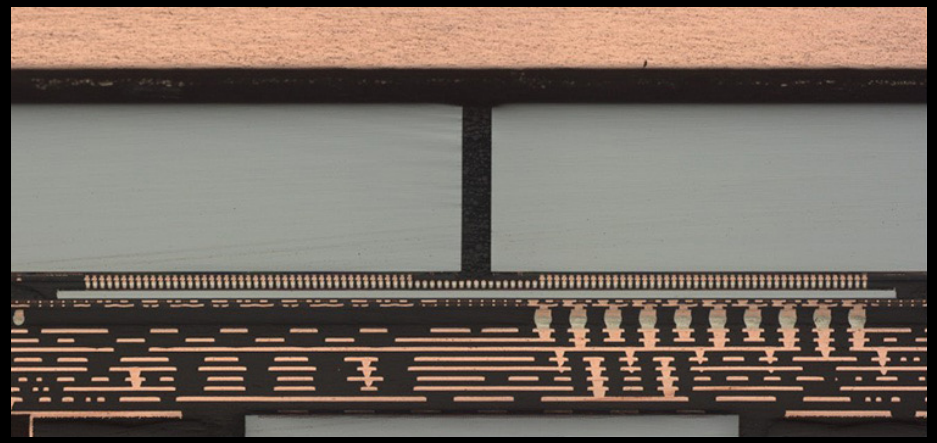
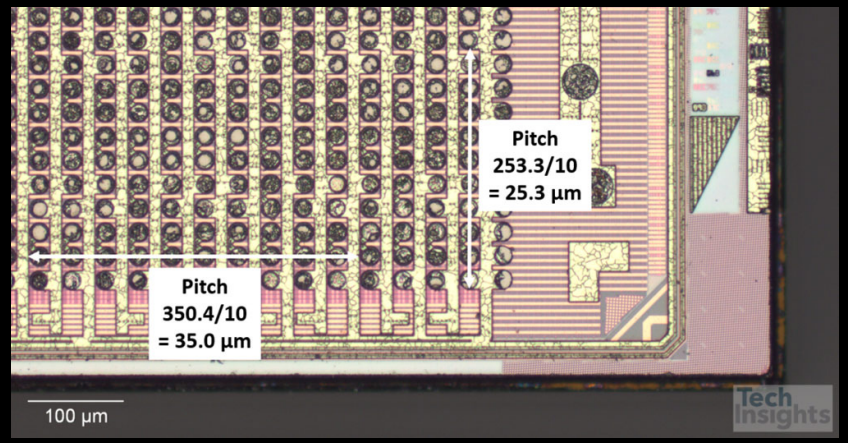


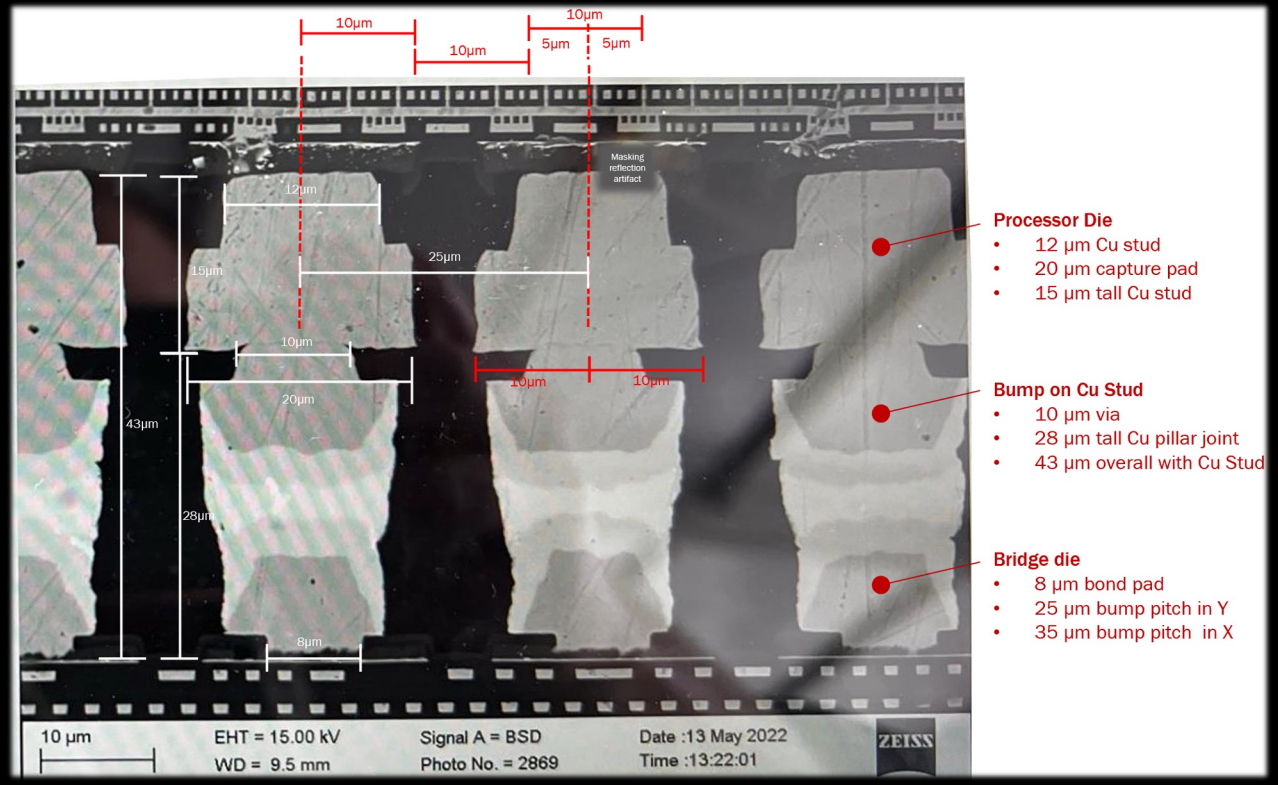
Photo source: Apple M1 Ultra SoC, Yole SystemPlus 2022



https://www.techinsights.com/blog/apple-joins-3d-fabric-portfolio-m1-ultra

Semiconductor Industry's Most Advanced Packaging (1st half of 2022)

- Ultra fine pitch Cu pillar flip chip bridge die (25µm x 35µm)
- 10,000 bond pads per die for bridge (leading density when introduced)
- **2.5 TB/s estimated bandwidth**



65x72mm TSMC InFO-L fan-out on substrate

- Chips up chips first M1 Max die (2 die)

Major challenge in manufacturing with < 4µm die shift required (x, y & θ after chip attach & mold)

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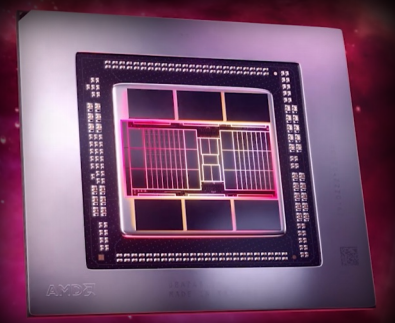
High-end Gaming PCs with AMD RDNA3 – August 2022

AMD

RDNA3 GPU

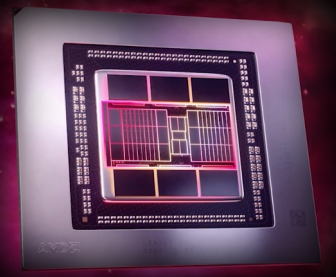


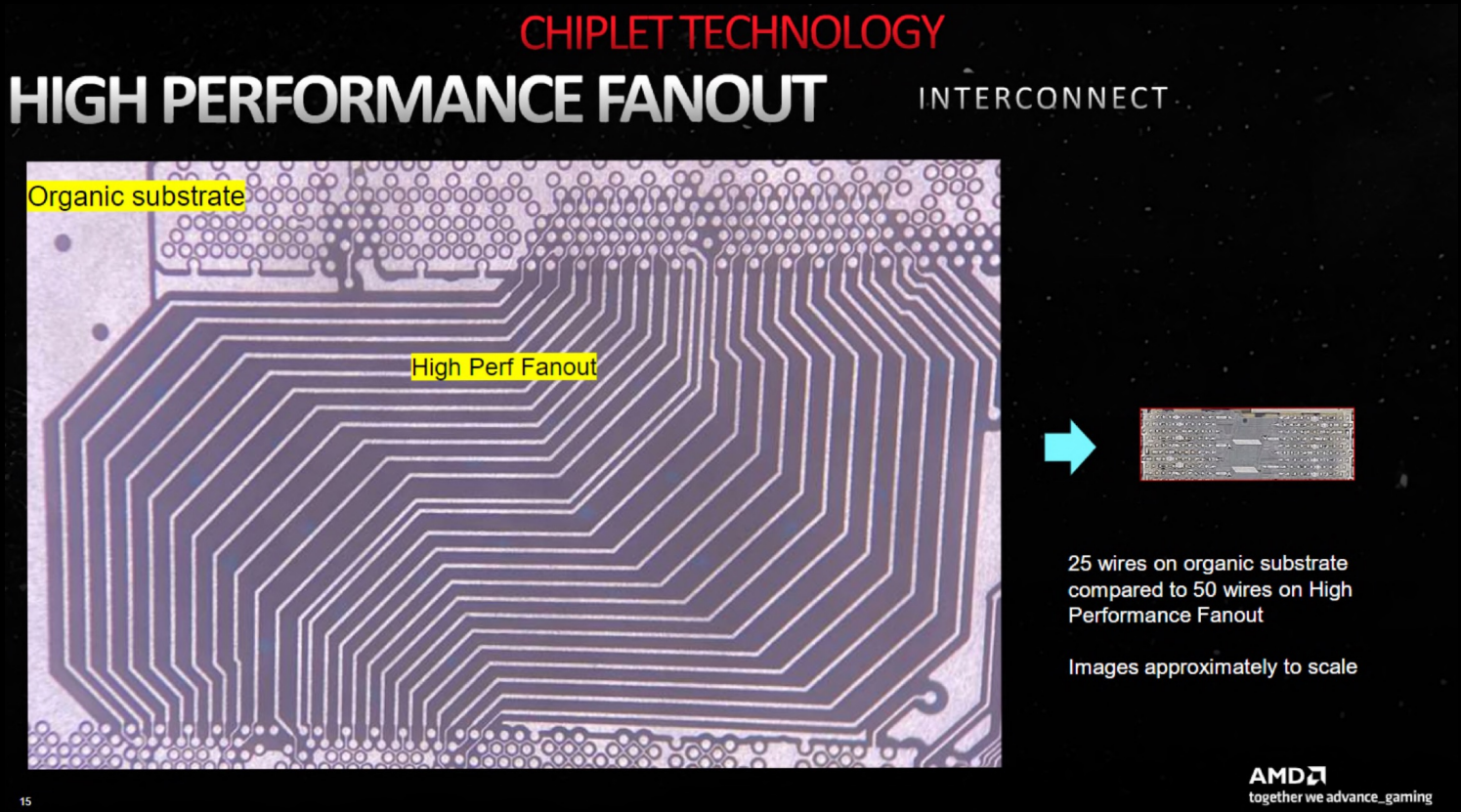
The world's most powerful gaming computers, over 28 teraflops of performance

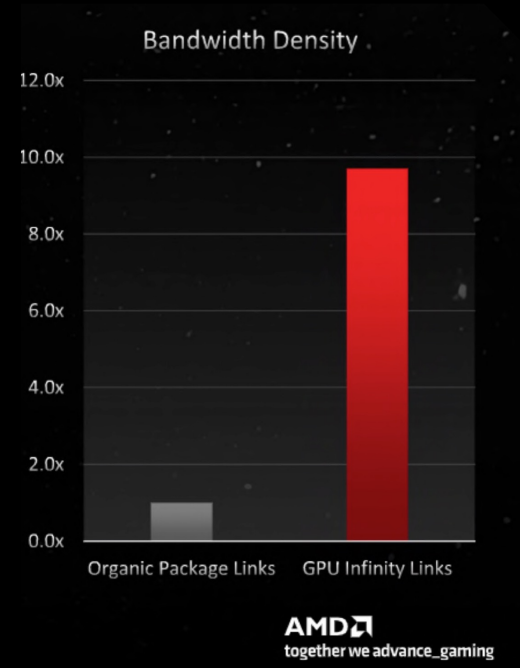
DECA

A Look Inside AMD's RDNA3

Breakthrough density increase moving from laminate substrates to **chips first fan-out technology**







- *98% size reduction in size with advanced packaging technology (fan-out)*
- *Order of magnitude increase in bandwidth*

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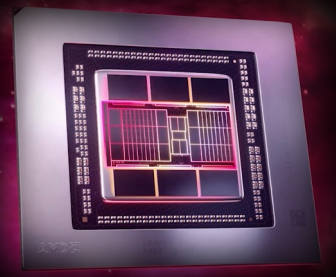
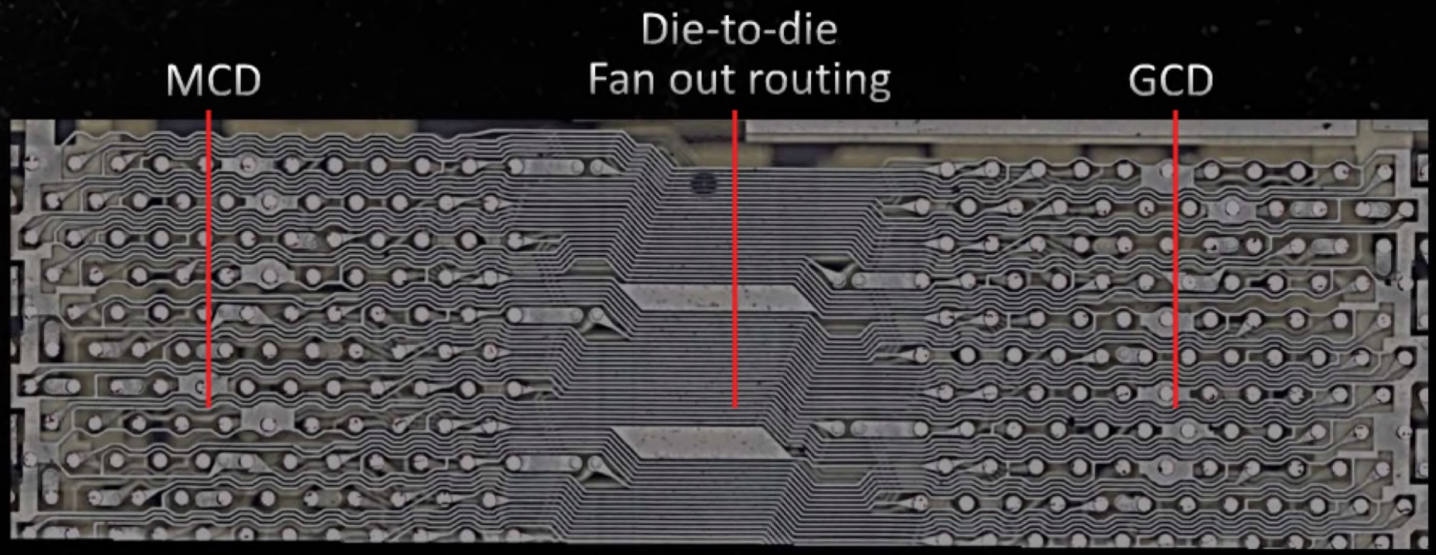
A Look Inside AMD's RDNA3



The New Most Advanced Packaging (2nd half of 2022)

- Very fine pitch 35µm pitch die bond pads
- 4 layers of RDL – no complicated bridge die required (RDL only)
- 5.3 TB/s spec performance (double the Apple A1 of six months earlier)

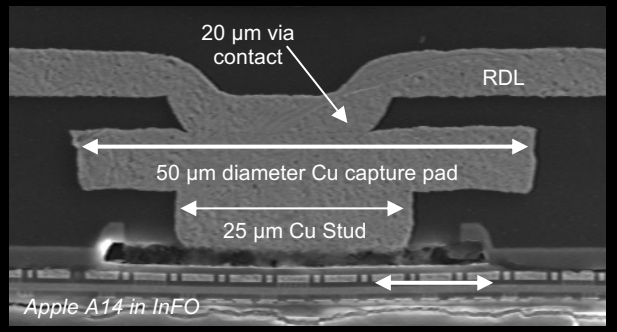


8µm via & 13µm capture pads

- Again, like the M1 ultra, < 4µm total die shift required (x, y, & Θ after chip attach & mold)
- Significant manufacturing challenge

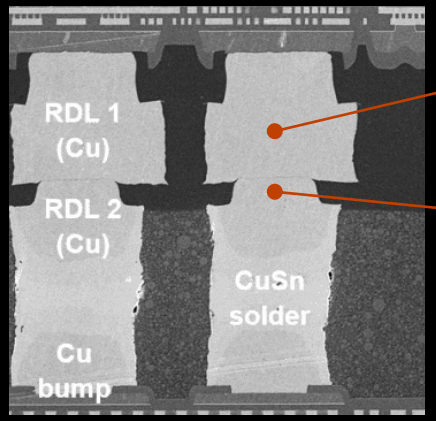
Accounting for die shift in the M1 Ultra

TSMC InFO



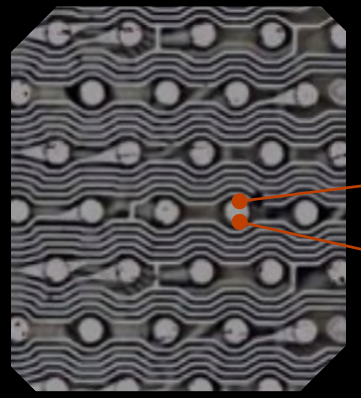
Source: Prismark iPhone 12 Analysis Jan'21

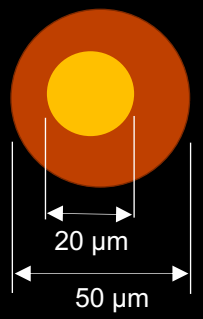
Apple M1 Ultra



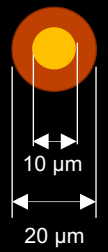
https://www.semiconductor-digest.com/apples-m1-ultra-does-use-info_lsi-or-is-it-cowos-l/

AMD RDNA3





Large Cu capture pad
(extra layer added to Cu stud)



Small ratio
precision die attach
low throughput

Have we reached the practical limits of fan-out scaling?

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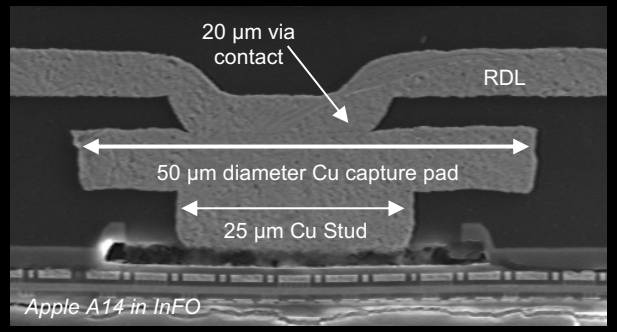
Adaptive Patterning Eliminates the Capture Pad

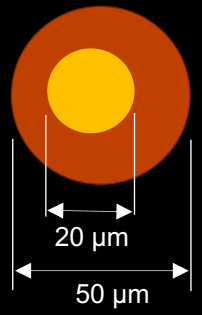
Breaking through the die bond pad interface barriers of the past

TSMC InFO



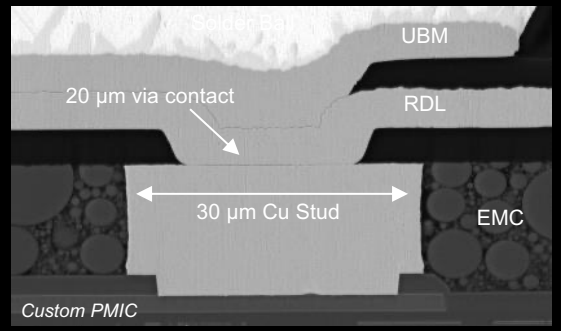
Source: Prismark iPhone 12 Analysis Jan'21

Via connection without Adaptive Patterning



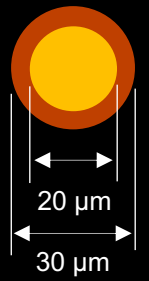
Large Cu capture pad *(extra layer added to Cu stud)*

M-Series with Adaptive Patterning



Source: Prismark iPhone 12 Analysis Jan'21

Via connection with Adaptive Patterning



Cu stud size *(no need for extra Cu layer)*

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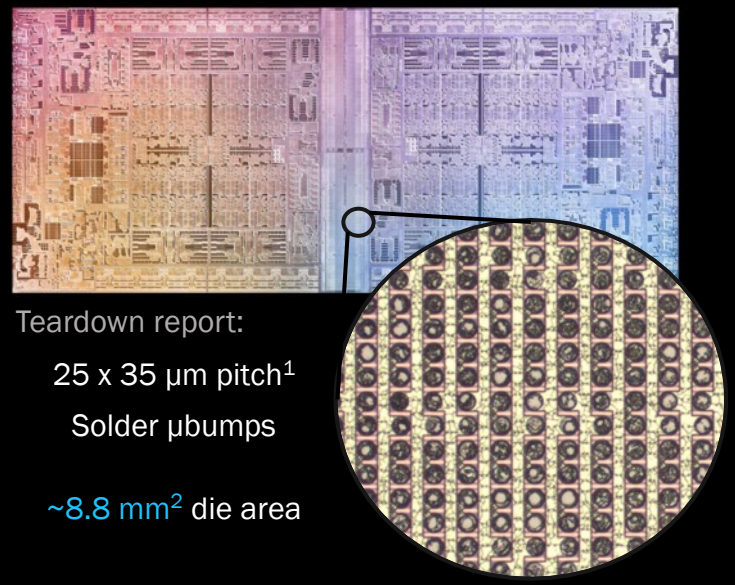
Industry Leading Die-to-Die Bandwidth (M-Series™ with Adaptive Patterning®)

- Industry's most advanced die-to-die interconnect density as of today
- Integrates two M1 Max die
- > 10,000 die-to-die connections

Silicon Bridge



Teardown report:

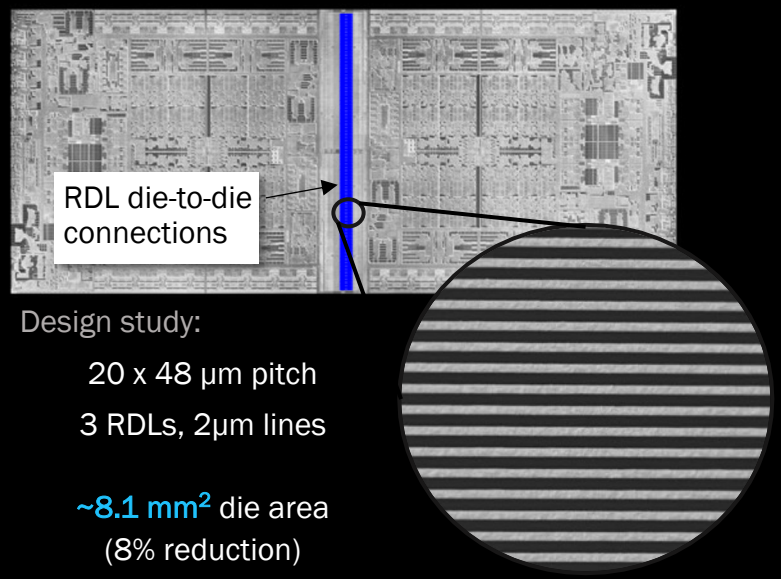
25 x 35 µm pitch[1]

Solder µbumps

~8.8 mm² die area

[1]Techsearch International Inc.

M-Series Gen 2



Design study:

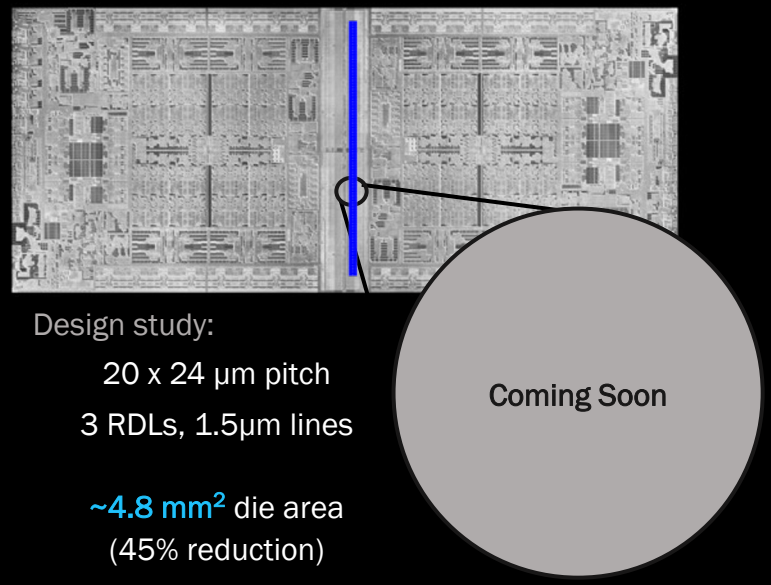
20 x 48 µm pitch

3 RDLs, 2µm lines

~8.1 mm² die area

(8% reduction)

M-Series Direct - MDx



Design study:

20 x 24 µm pitch

3 RDLs, 1.5µm lines

~4.8 mm² die area

(45% reduction)

MDx removes capture pads all together

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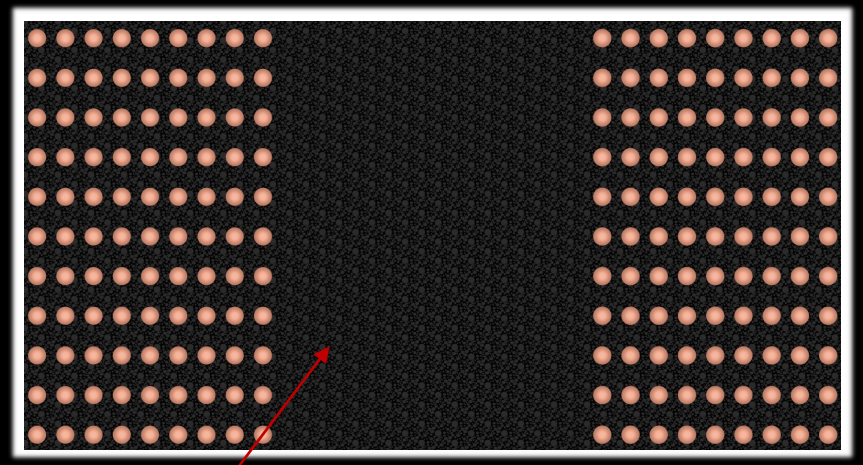
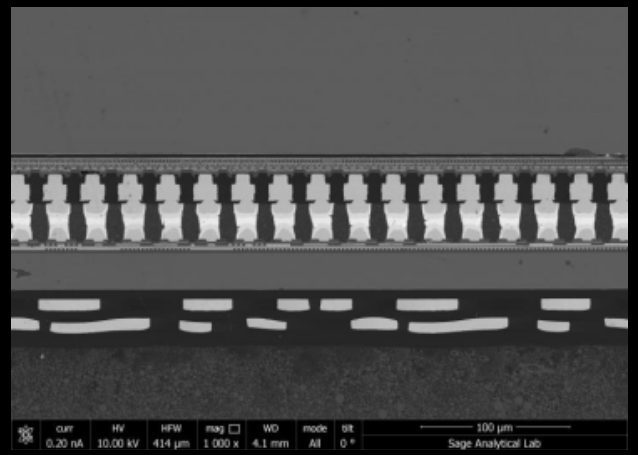
Industry Leading Die-to-Die Bandwidth (M-Series™ with Adaptive Patterning®)

Matching TSMC's Apple M1 Ultra benchmark & significantly outperforming it

1. TSMC InFO Bridge Die Solution



Die-to-Die requires bridge die
15.8 µm UBM pad
25 x 35 µm pitch

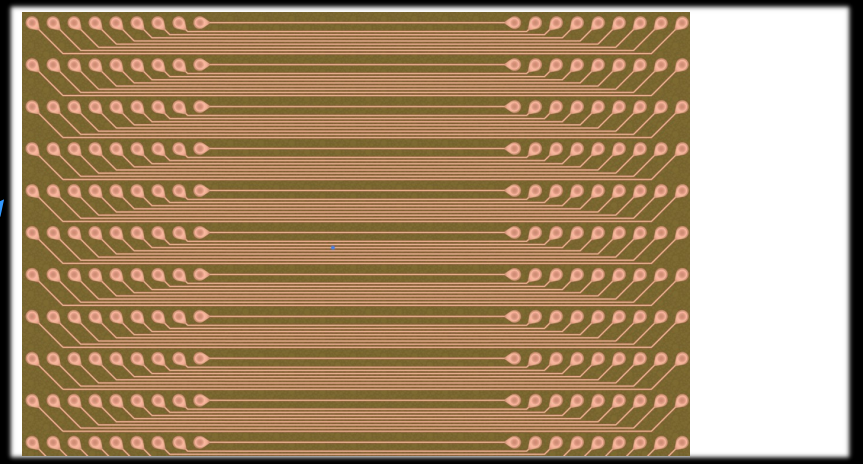


TSMC requires bridge die with challenging flip chip attach

All drawings to scale

Deca solutions much simpler with RDL-only

2. Deca M-Series Gen 2C (to scale)



Die-to-Die interconnect in RDL
1.5 µm line & space, 14um capture pad
20 x 40 µm pitch

White box = TSMC M1 Size

3. Deca Gen 2 MDx (M-Series Direct with no capture pads)

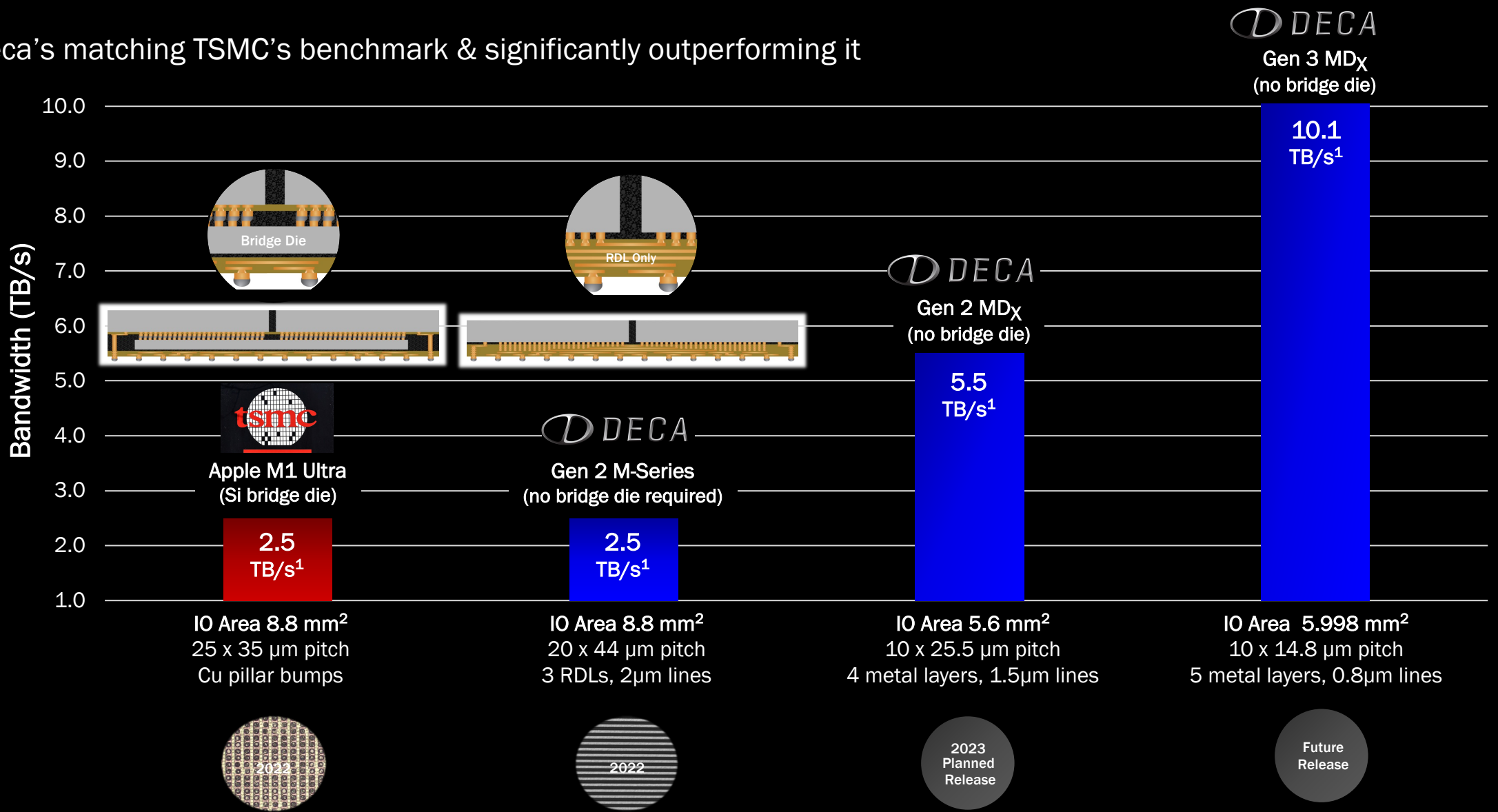
MDx interface size
(image under NDA)

DECA

Note: Multiple patents issued & pending

Industry Leading Die-to-Die Bandwidth *(M-Series™ with Adaptive Patterning®)*

Deca's matching TSMC's benchmark & significantly outperforming it



[1] Assumes 20mm beachfront with the same per-wire bandwidth (Gbps) for all cases

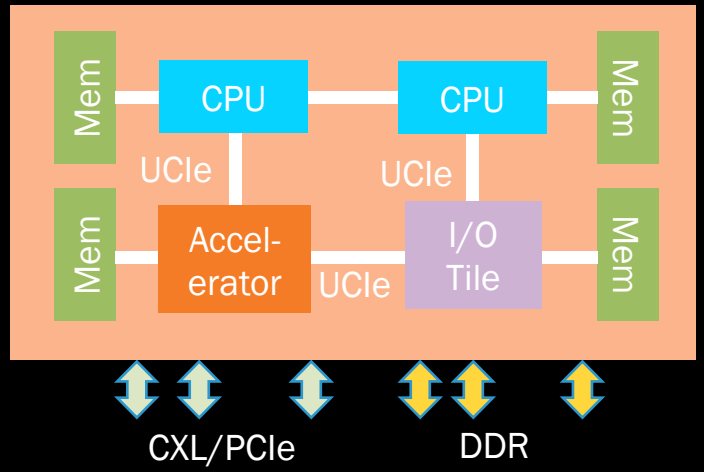
[2] Estimated IO area includes signal bumps for one die; ground bumps and guard traces vary depending on implementation

Note: Multiple patents issued & pending

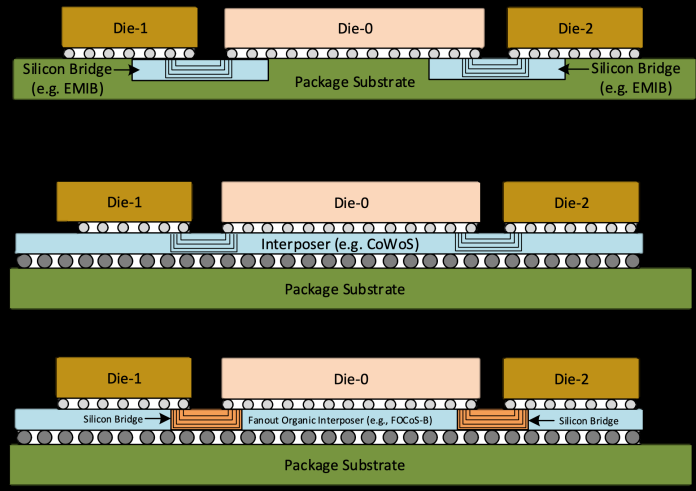
DECA

Chiplet Standardization

Primary goal: provide an open, multi-protocol, on-package interconnect standard for connecting multiple dies



Example use-case from UCIe specification



Example implementations from UCIe specification

Standard UCIe footprint originally targeting Si bridge, Si interposer, CoWoS

Major IP suppliers are now offering UCIe PHYs and controllers

DECA SYNOPSYS® cadence Alphawave

Chiplet Standardization

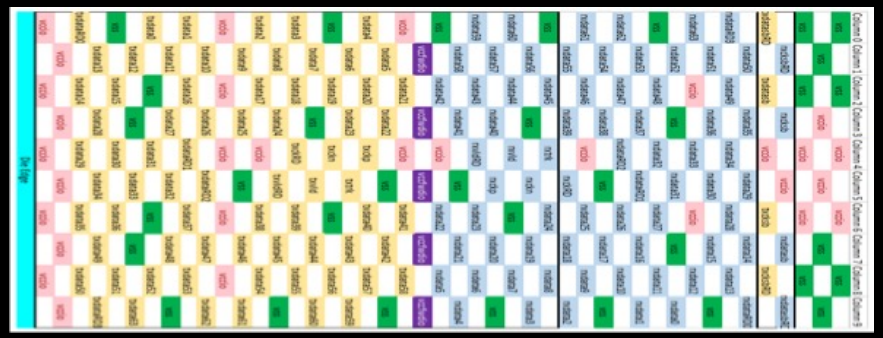
Alphawave collaboration underway for UCIe layout and electrical simulation

✓ Initial electrical extraction completed for two layout options:

45µm Staggered Pitch

Standard Footprint

0.41mm²



1043µm

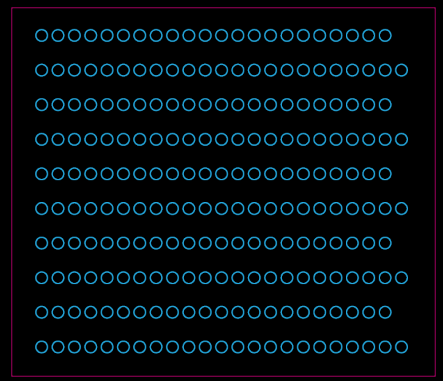
389µm

44% less area

20x48µm Pitch

Area Optimized

0.23mm²



522µm

446µm

- Standard UCIe footprint originally targeting Si bridge, Si interposer, CoWoS
- Layout completed with Gen 2 M-Series 5-RDL stack-up

- Optimized for Gen 2 M-Series capabilities
- Layout completed with 5 RDL Gen 2 M-Series stack-up
- Simulation results show 4 RDL stack-up is feasible

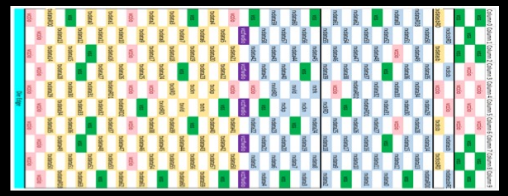
Simulation results show excellent insertion loss and low crosstalk

Chiplet Standardization

Alphawave collaboration underway for UCIe layout and electrical simulation

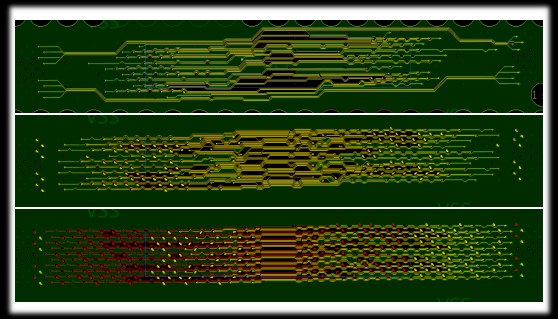
45µm Staggered Pitch

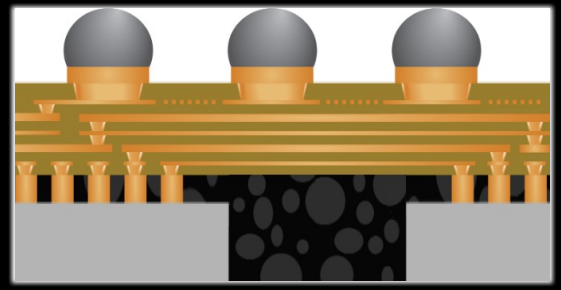
standard footprint



Gen 2 M-Series 5-RDL stack-up

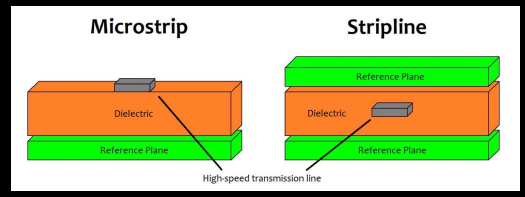
three signal layers, two reference plane layers





Optimized for low crosstalk

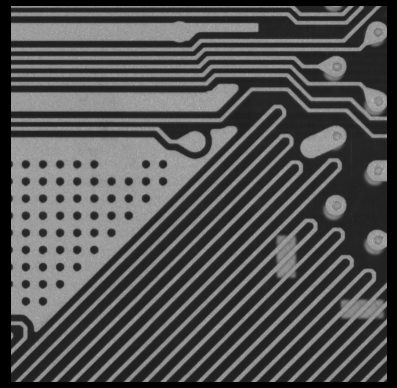
one stripline, two microstrip



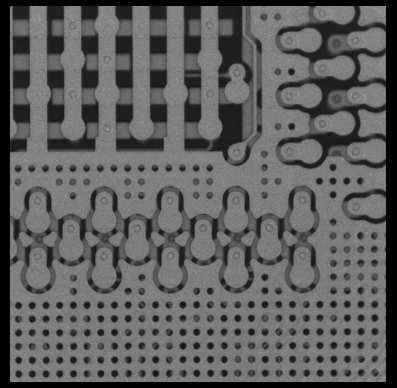
Stack-up optimized for low crosstalk without guard traces

Five Layer RDL on M-Series

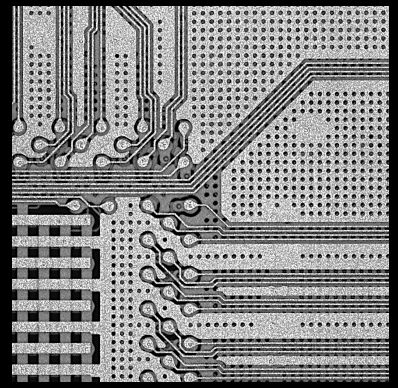
- Successfully designed & fabricated advanced CPU device - 24mm body size & 6 layers of metal (5 RDL + UBM)
- Second generation in 2023 delivers ultra-high-density chiplet integration with RDL-only solution



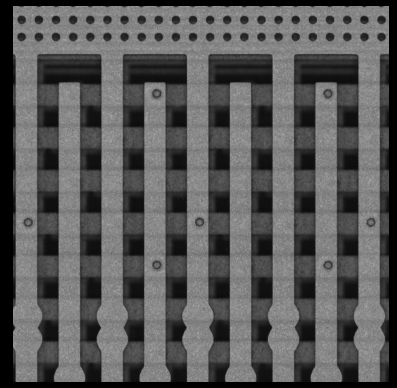
RDL 1



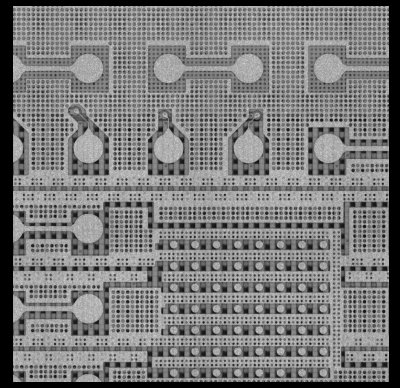
RDL 2



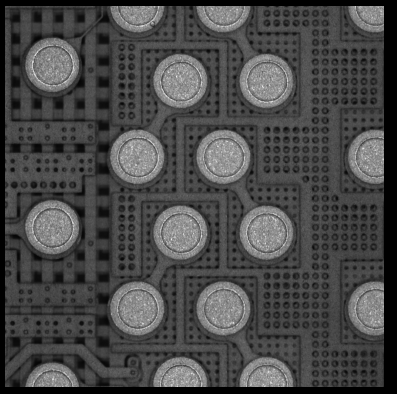
RDL 3



RDL 4



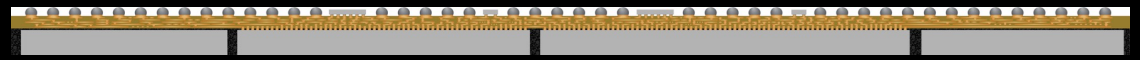
RDL 5

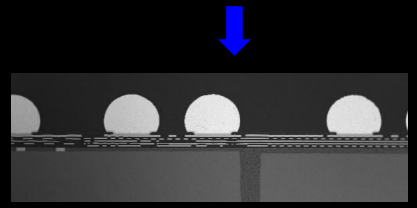


UBM

Phase 1
2022
Monolithic SoC

Phase 2
2023
Chiplet-based SoC



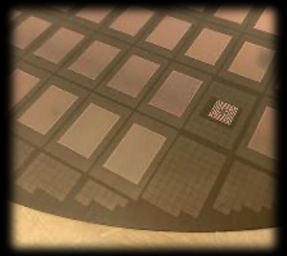


CPU **device split into chiplets**

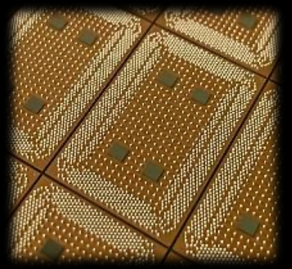
- 5-layer RDL (no bridge die req'd)
- 20 µm device bond pad pitch
- 60 µm die to die spacing
- Structural silicon added
- IPDs on UBM layer
- No bridge die required

Phase 1 device

- After panelization



- After IPD & ball attach



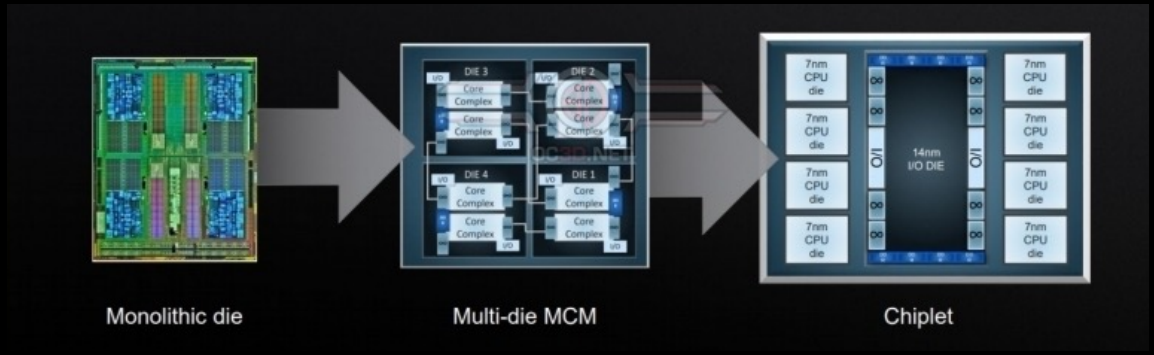
DECA & nepes

Outline

- Introduction
- Industry Perspective
- Leading Examples
- What's Next
- Conclusion

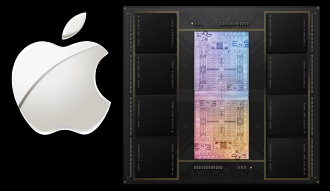
Conclusion

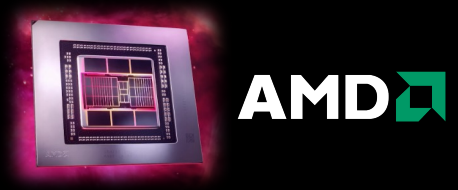
Semiconductor industry is moving to chiplets & heterogeneous integration



Advanced packaging technologies play a critical role today, and, in the future

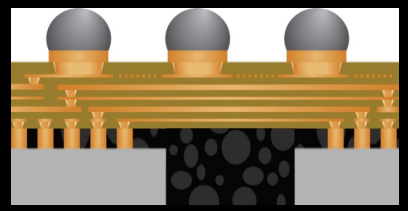
Fan-out capabilities are already proving successful in chiplets today





AMD

New capabilities enable the next generation of fan-out density



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Thank you from