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Influence of Rigid Carrier Substrates & its Release Layer on Ultra Fine Pitch chip last FO-WLPs.

Mitsui Mining and Smelting Co., Ltd.,
Business Creation Sector
HRDP Business Development Unit

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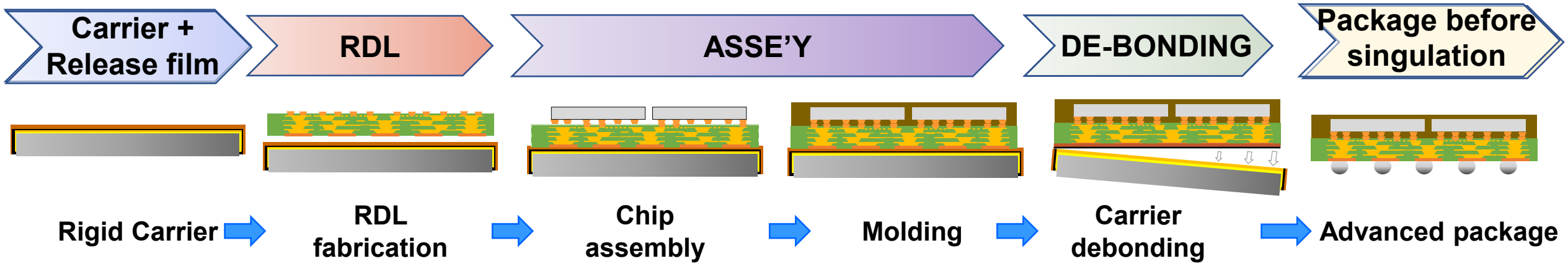
Presentation Outline

- Introduction
  - ➔ Challenges in assembling FO-WLP
  - ➔ Need for Carrier substrates & Release Layer
- Requirements for Rigid Carrier Substrates
  - ➔ Features (constructed structure)
- Requirements for Release Layer
  - ➔ Features (constructed structure)
- Current bonding & Debonding practice in assembly
- Novel alternate solution through HRDP®
  - ➔ Features (constructed structure)
  - ➔ How does it influence? (Results & Observation)
- Advantages of HRDP® over current practices
- Conclusion

Carrier based "Fan-Out Chip last" process flow



Carrier + Release Film Provides:

- Ultra fine line RDL (2/2μ ➔ > 1/1μ)
- Minimize warpage
- Easy and quick carrier debonding
- Reduce "total cost of ownership"

INFLUENCE AND CHOICE OF
- TEMPORARY **CARRIERS**
- **RELEASE FILMS**

WILL BE FOCUSED IN THIS TALK

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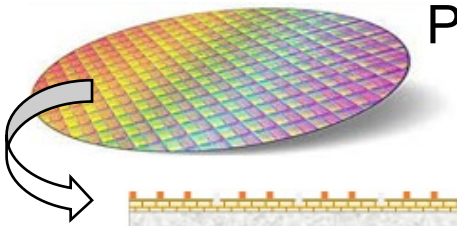
Warpage during Assembly

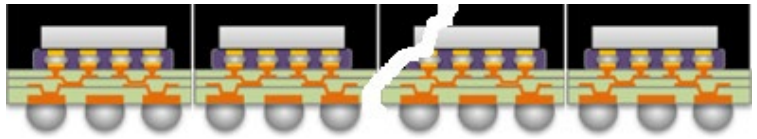


Processed Wafer

Background Wafer with chips

Processed through final packaging

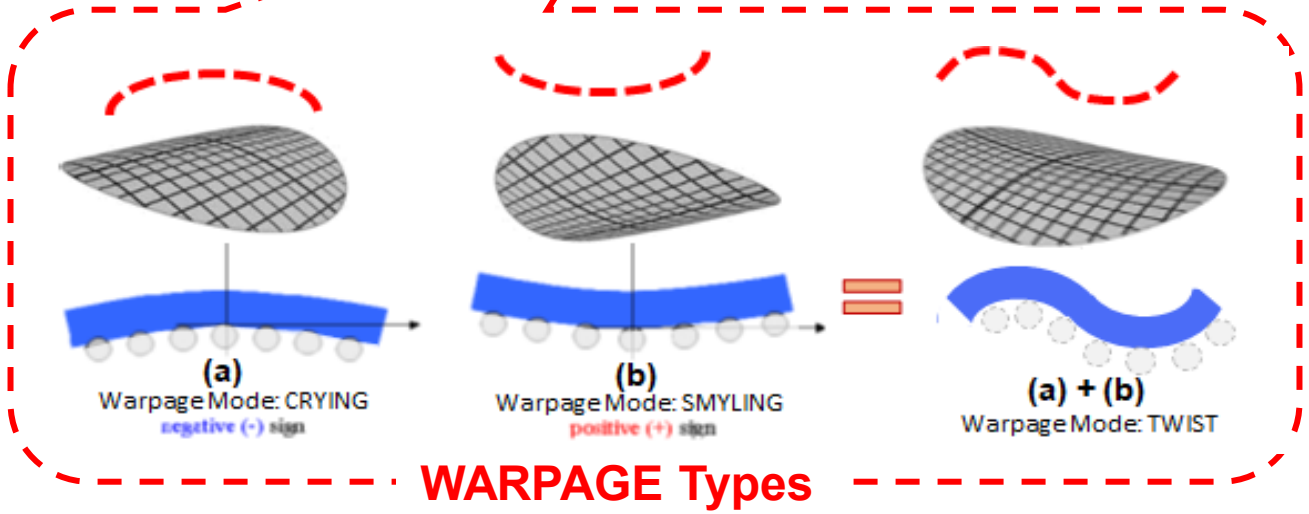
Assembled Structure



⚠WARNING

If FO-WLP assembly process is not carefully designed, then it is likely to result in **WARPAGE**, causing yield loss

Primary reason for **WARPAGE** is CTE mismatch between various materials used in package ~ especially after molding



WARPAGE Types

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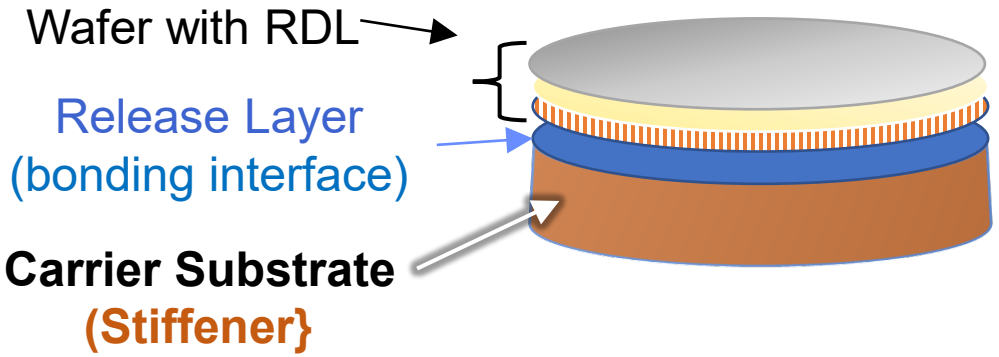
Need for Carrier Substrate

To Control Warpage



CARRIER SUBSTRATE
holds the wafer structure firmly during assembly process to control against warpage

PURPOSE

Requirements of Carrier Substrates:

- High Rigidity (*i.e.,* high modulus)
- CTE close to bulk CTE of assembly structure materials
- Good surface flatness

Substrates **MATERIALS** used:

- CTE matched **Borosilicate Glass**
- **Soda-lime Glass**
- **Silicon** (thicker than silicon device)

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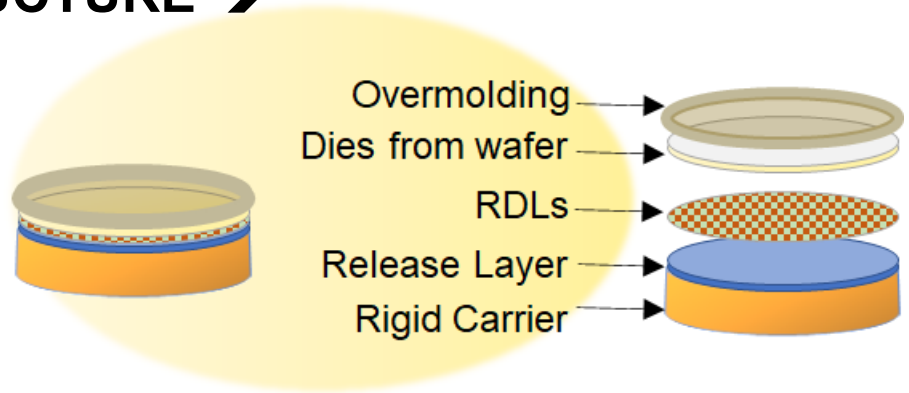
Need for Release Layer

To help Bonding & Debonding

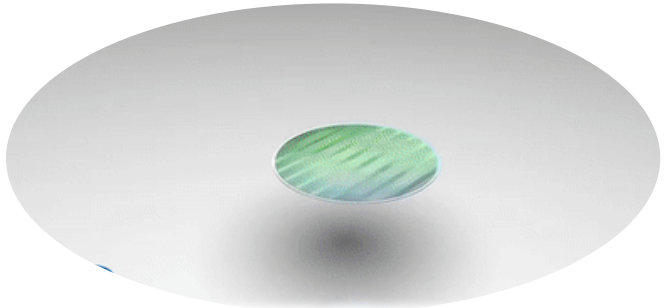
❖ **PURPOSE ➔**

RELEASE LAYER <u>bonds</u> carrier & grows RDL with the wafer and finally **<u>releases</u>** assembled wafer before singulation process

❖ **STRUCTURE ➔**

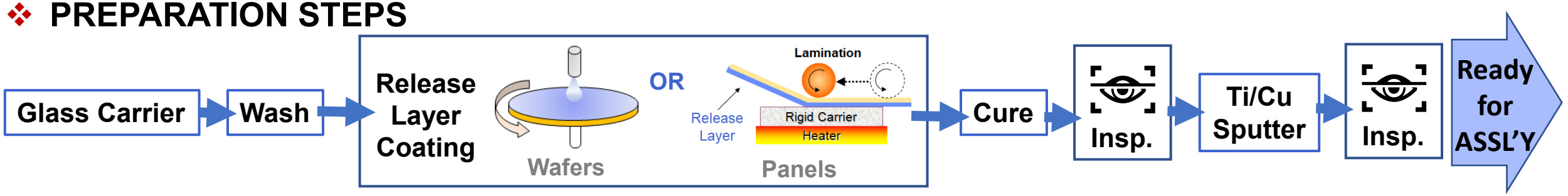


RDL on Carrier Substrate



Courtesy Intel ➔ Google Images

❖ **PREPARATION STEPS**



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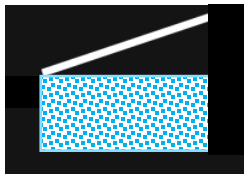
Release Layer Separation

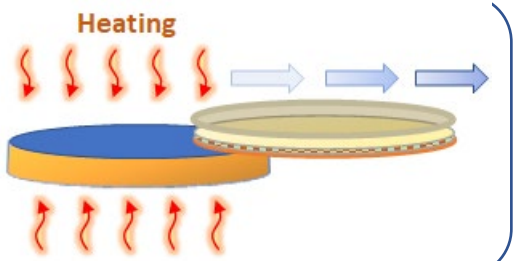
SEPARATION



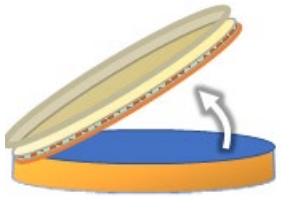
Debonding

CURRENT SOLUTIONS

Slide Off
- Thermal



Lift Off
- Laser (LLO)
- Mechanical
- Chemical



ISSUES in DEBONDING using current solutions:

During Preparation (pre-assembly) –
- Contamination
- Surface Roughness
- Flatness /Thickness
- Porosity / Pinholes
- Material loss in spin coating (>60%)

During Assembly Process –
- Adds to preparation time, quality & cost
- **Surface Roughness & Planarization of 1st layer RDL patterns ➔ limiting fine L/S RDL resolution**
- Heterogeneous separation during debonding

LIMITATION: Cannot feature < 2/2μ L/S pitch RDL for chip last FO-WLPs

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New platform carrier solution ➔ HRDP®

(High Resolution Debondable Panel) Technology

HIGHLIGHTS

- Most compatible solution for Fan-Out chip last process
  - ➔ Capabilities for ultra-fine RDL structures (<2µm L/S)
  - ➔ Lithography can be done directly on copper seed layer of flat **HRDP ®**, thus eliminating seed layer sputter during 1st RDL
  - ➔ Smooth sputtered carrier surface, resulting in increased assembly yield.
- Wafer Level & Panel Level Packaging Capability in varied dimensions
- Release Layer is made of 100% inorganic material,
- Stabilizes dimensions and minimizes warpage during assembly work in progress
- Easy & low release force at room temperature mechanical debonding of **Inorganic** releasing material – with low release energy and increased UPH
- Simple “Drop-in Solution”, eliminating conventional carrier preparation process steps & issues associated with them.
- During processing, this inorganic release layer (IRL) demonstrates higher chemical resistance and heat resistance than alternative technology such as the laser lift-off (LLO) release layer.

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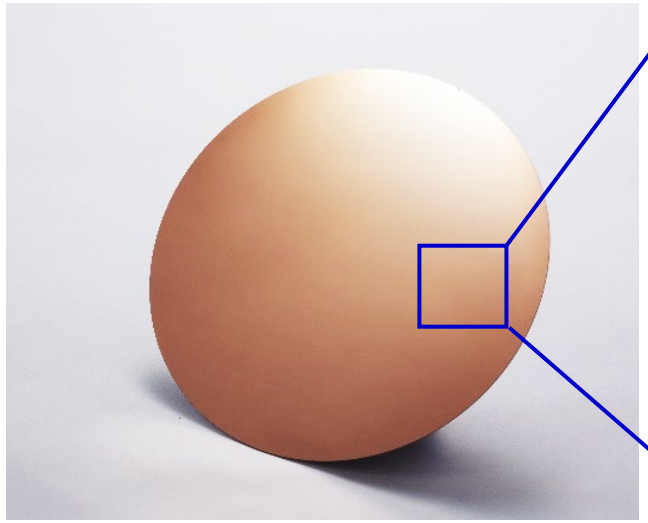
About HRDP®

Product Configuration

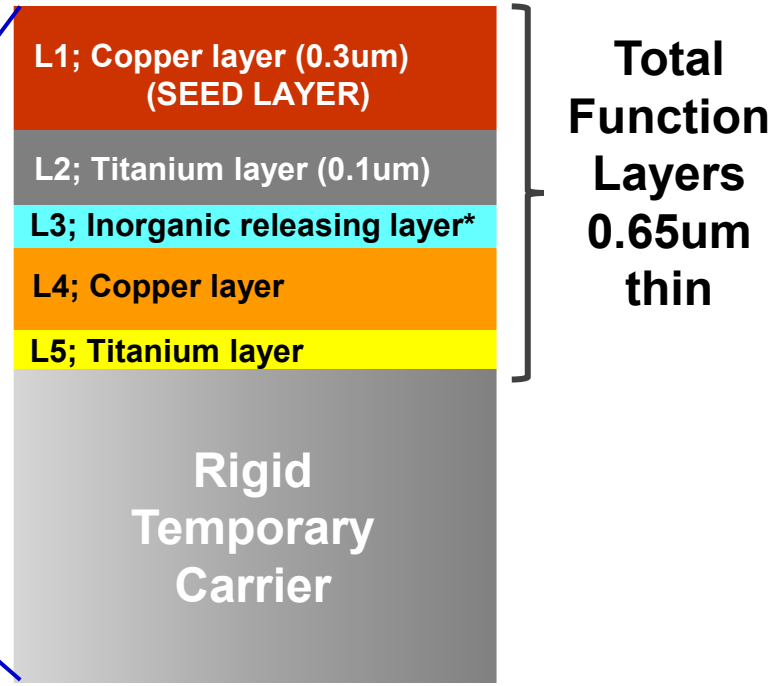
- HRDP® carrier is offered in various dimensions and thicknesses as round wafers and square/rectangular panels with glass or silicon to match customer s' CTE requirements.
- Inorganic Release Layer (IRL) is laid sandwiched between flat sputtered layers

Panel format



Wafer format

(a) Exterior



(b) Structure

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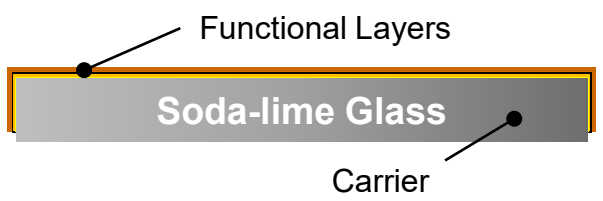
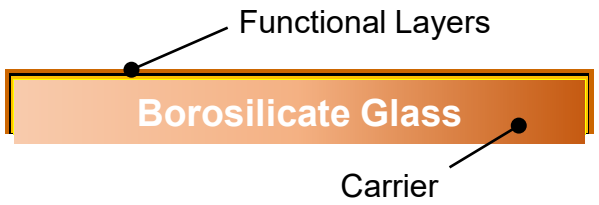
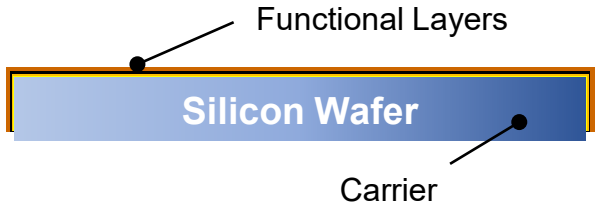
HRDP® Product Offerings by Carrier Material Types

Features	Glass		Silicon
	HRDP-GL	HRDP-GB	HRDP-S
Carrier type	Soda-lime Glass 	Borosilicate Glass 	Silicon Wafer 
Carrier CTE※1	8.5	3.4～12.1※2	3.6
Carrier Size Format (mm)	Wafer : φ200 & φ300	Wafer ※2 : φ200 & φ300	Wafer : φ200 & φ300
	Panel : 200×200～600×600	Panel ※2 : 200×200～600×600	-
Carrier Thickness	0.7mm、1.1mm、1.8mm	0.7mm～1.8mm※2	0.750mm
Total Thickness Variation (TTV)	≦20um	≦5um	≦5um
Young's Modulus	7.5×10^3 kg/mm^2	7.4×10^3 kg/mm^2	19.3×10^3 kg/mm^2

Notes: ※1 CTE is a reference value.
※2 Specific application specific CTE & Rigidity can be customized.

Typical properties by carrier material options for HRDP®

Physical Properties	Carrier Types			
	Soda Lime	Borosilicate	Silicon	units
Density	2.5	2.4	2.5	2.3	$\times 10^3$ kg/m^3
Young's Modulus	7.5	7.4	7.3	19.3	$\times 10^3$ kg/mm^2
Poisson's Ratio	0.22	0.23	0.21	N/A	-
Mohs Hardness	6.5	N/A	N/A	N/A	-
Thermal Expn. (CTE)	8.5	3.4	9.4	3.6	$\times 10^{-6}$ ℃ (at 20-350℃)
Specific Heat	0.19	0.77	N/A	N/A	cal/g℃ (at 0-50℃)
Thermal Conduct.	0.86	N/A	N/A	160	kcal/m·h·℃
Strain Point	523	669	553	N/A	℃
Annealing Point	540-560	722	602	N/A	℃
Softening Point	720-740	971	N/A	N/A	℃

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Process Flow Comparison

HRDP® increases productivity

CONVENTIONAL ORGANIC RELEASE LAYER PREPARATION STEPS:

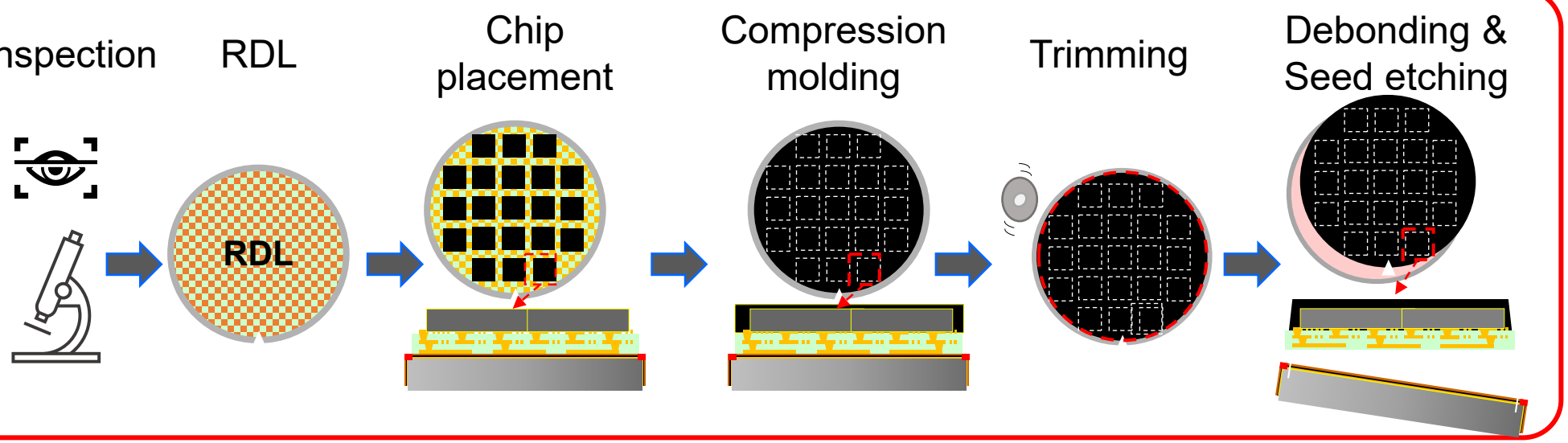
Glass Carrier → Wash → Release Layer Coating On Carrier Wafers / Panels → Cure → Insp. → Ti/Cu Sputter

ASSEMBLY PROCESS STEPS

ORGANIC

Ready for ASSEMBLY

HRDP®



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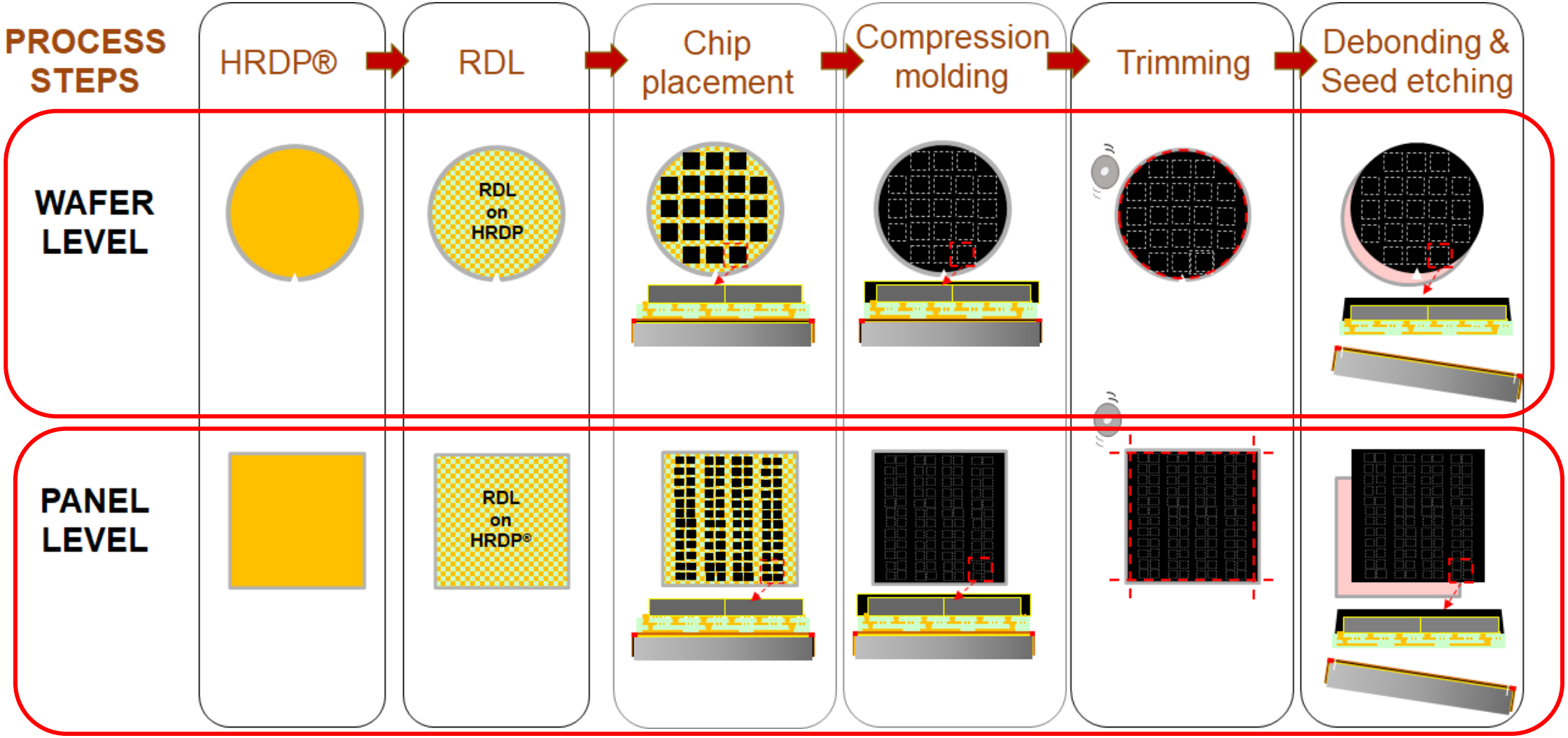
Fan Out Chip Last process flow using HRDP®



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Manufacturing of HRDP ®

Glass inspection

Carrier cleaning

- Brush roll
- Alkaline cleaning
- Ultrasonic cleaning

Function layers sputtering

- Particle monitor during sputtering

HRDP® inspection

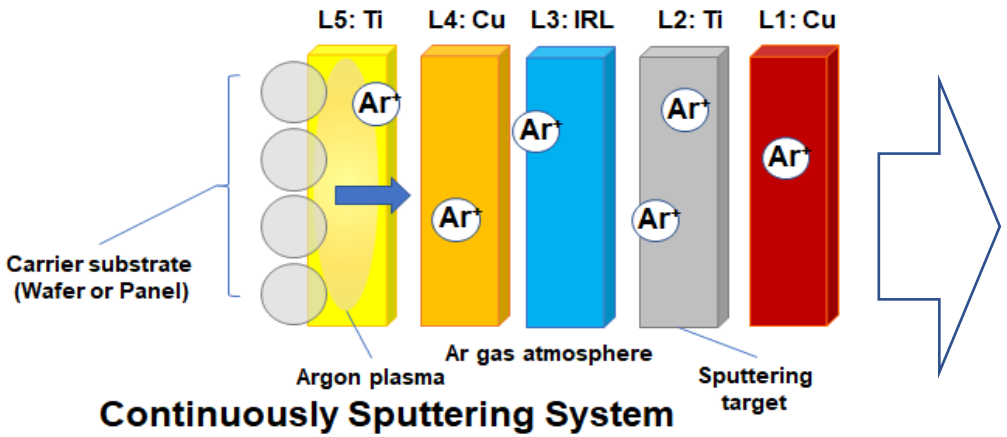
- Automatic particle inspection
- Film thickness measurement etc.

Packing and shipping

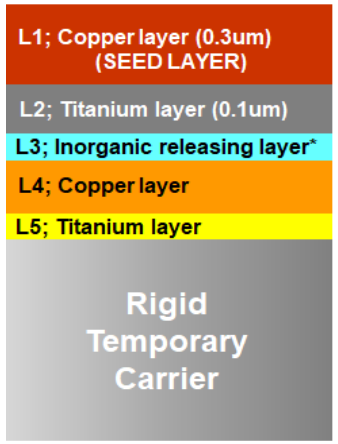
Panel packing

Wafer packing

Clean room; Class 100



Continuously Sputtering System



Sputtered Structure

HRDP after sputtering
(Wafer format : Φ300mm)

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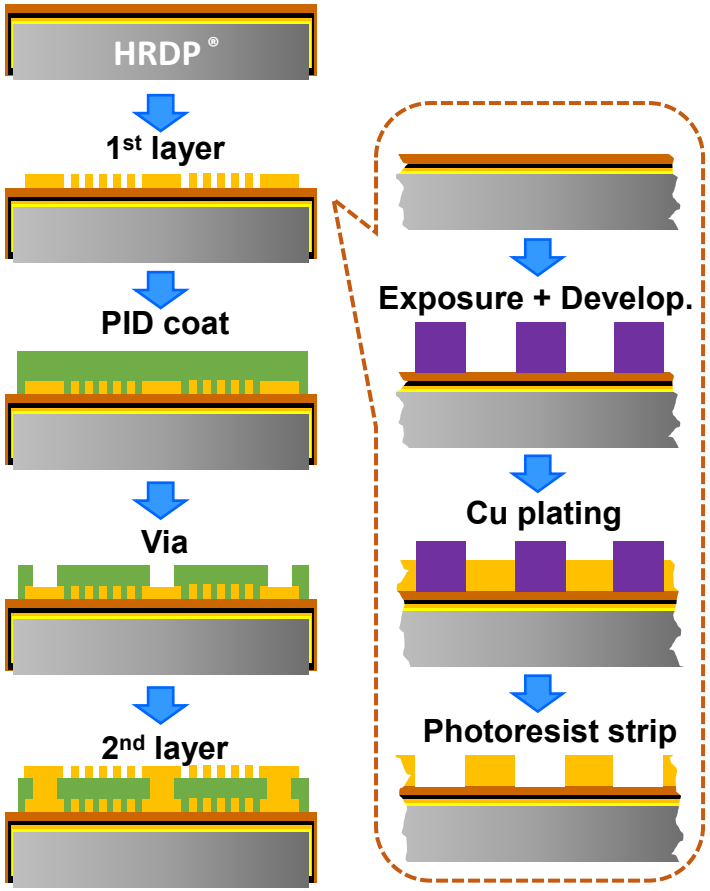
HRDP® helps lithography process optimize to form L/S of 2/2µm & below



Process	Company	Material / Equipment	Condition
Carrier	Mitsui	HRDP-GL (CTE: 8.5) HRDP-GB (CTE: 4.6) HRDP-S (CTE: 3.6)	Wafer: φ300mm Panel: 320mm sq. Thickness: 0.7mm, 1.1mm
Photo resist	Sumitomo Chemi.	XI-4920 (Liquid type)	Thickness: 4um
Exposure	Canon	Stepper: FPA-5520iV (Expose area 52x68mm)	Photo resist: 1600J/m^2 Photo Via: Dose 4500J/m^2
Pattern plating	UYEMURA	Copper plating	Thickness: 2um
PID (Photo Imageable Dielectric)	A company	Liquid/Negative-type	Thickness: 5um Via: φ8um, φ10um, φ15um, φ18um
Molding compound	B company C company D company	Granule type Granule type Liquid type	Thickness: 600um Cure temp & time: *
Mold equipment	TOWA	Compression mold	Wafer: φ297mm Panel: 300mm sq.

* Molding compound cure condition

- A: In-mold cure temp. and time: 150℃ x 10min , Post-mold curing temp. and time: 175℃ x 6hr
- B: In-mold cure temp. and time: 150℃ x 5min , Post-mold curing temp. and time: 150℃ x 4hr
- C: In-mold cure temp. and time: 125℃ x 10min , Post-mold curing temp. and time: 150℃ x 1hr

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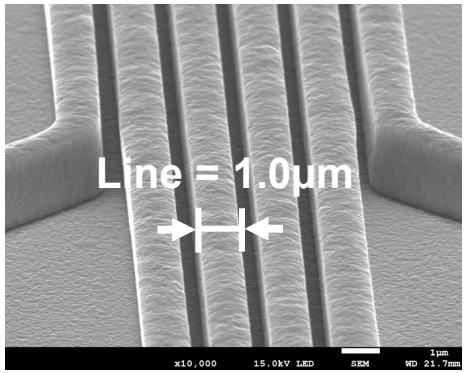
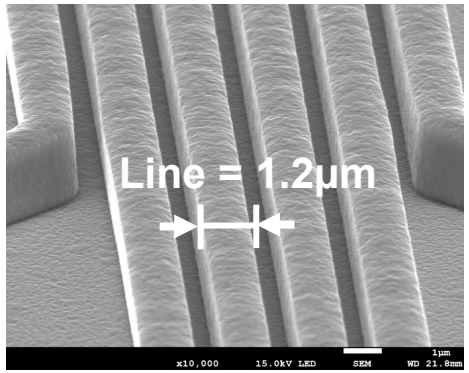
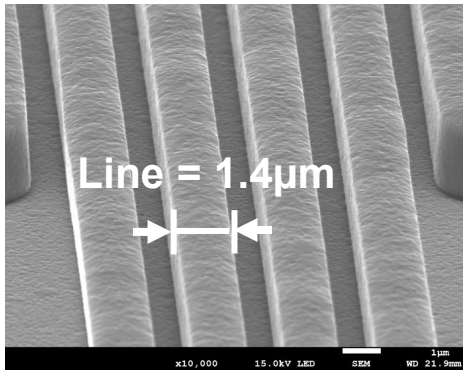
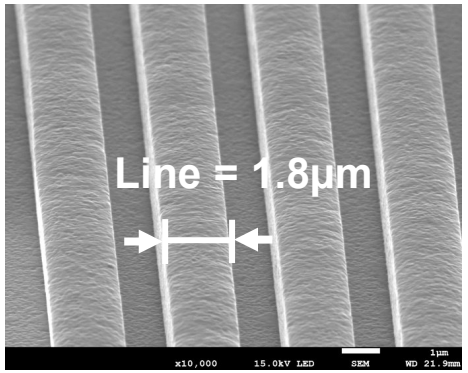
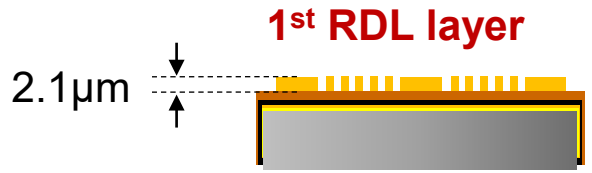
HRDP® helps lithography process optimize to form L/S of 2/2 and finer

Line & Space width	0.8/0.8 µm	1.0/1.0 µm	1.2/1.2 µm	1.5/1.5 µm
Aspect ratio	2.1	1.8	1.5	1.2
After photoresist strip (x 10000)				

- Cu plating thickness: 2.1µm
- Carrier : HRDP-GL (φ300mm wafer format)



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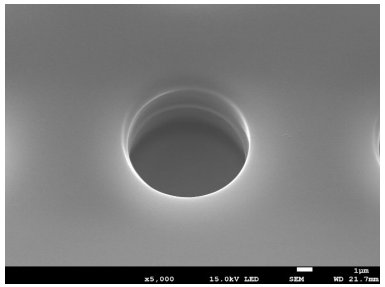
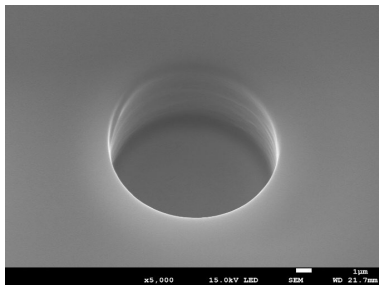
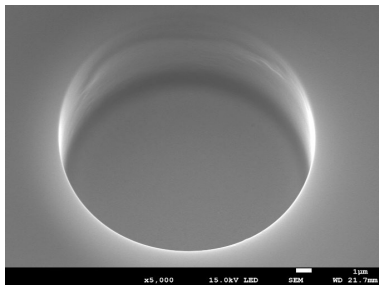
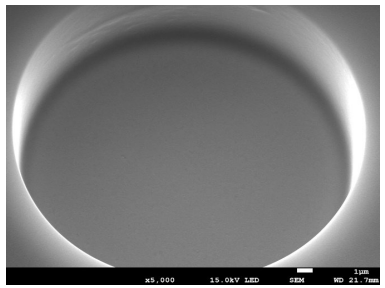
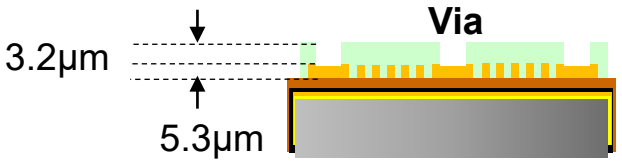
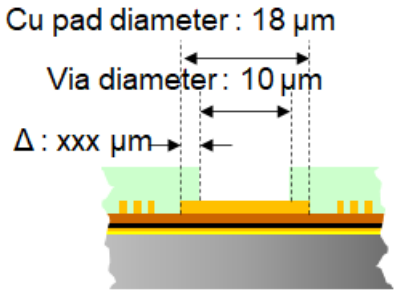
Process Optimize to form fine photo via

Via diameter	φ8μm	φ10μm	φ15μm	Φ20μm
Aspect ratio	0.4	0.32	0.21	0.16
After PID development Tilt 30° (x 5,000)				
Via diameter (Bottom)	7.5μm (σ: 0.3)	10.7μm (σ: 0.2)	15.2μm (σ: 0.2)	21.3μm (σ: 0.4)

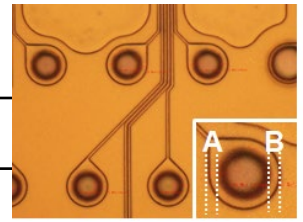
- Carrier : HRDP-GL (CTE: 8.5), φ300mm Wafer format
- PID thickness: 5.3μm





- Δ variation in wafer

	HRDP-GL	HRDP-GB	HRDP-S
A	3.5 (σ:0.1)	3.4 (σ:0.2)	3.7 (σ:0.1)
B	3.3 (σ:0.1)	3.2 (σ:0.1)	3.6 (σ:0.1)



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High chemical resistance during wet processing against variety of chemicals

Chemicals	temperature/ processing time	Result			
		Discoloration	Blister	Delamination	Corrosion
DI water	RT/10min,30min	10min:Pass 30min: Pass	Pass	Pass	Pass
5wt%KOH	RT/10min,30min	10min:Pass 30min: Discoloration	Pass	Pass	Pass
DMSO	RT/10min,30min,6 hours	10min:Pass 30min: Pass 6 hours: Pass	Pass	Pass	Pass
NMP	RT/10min,30min,6 hours	10min:Pass 30min: Pass 6 hours: Pass	Pass	Pass	Pass
Acetone	RT/10min,30min	10min:Pass 30min: Pass	Pass	Pass	Pass
EtOH	RT/10min,30min	10min:Pass 30min: Pass	Pass	Pass	Pass
2wt%H_2SO_4	RT/10min,30min	10min:Pass 30min: Pass	Pass	Pass	Pass
TMAH aq. (2.38%)	RT/10min,30min	10min:Pass 30min: Discoloration	Pass	Pass	Pass
※ PR stripper (ST-120)	50℃/10min,30min	10min:Pass 30min: Pass	Pass	Pass	Pass

HRDP® has excellent resistance to all processing chemicals customarily used.

※ **ST-120;** made by TOK Co., , It consists of DMSO, TMAH, NMP, Glycol etc.

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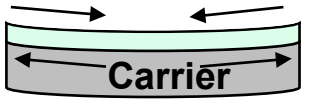
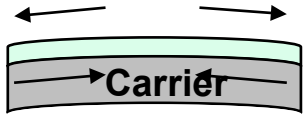
WARPAGE after Molding

Features	Glass	
	HRDP-GL	HRDP-GB
Carrier type	Soda-lime Glass	Borosilicate Glass
Molding		
Thermal Expn. (CTE)	8.5 ppm	3.4 ppm



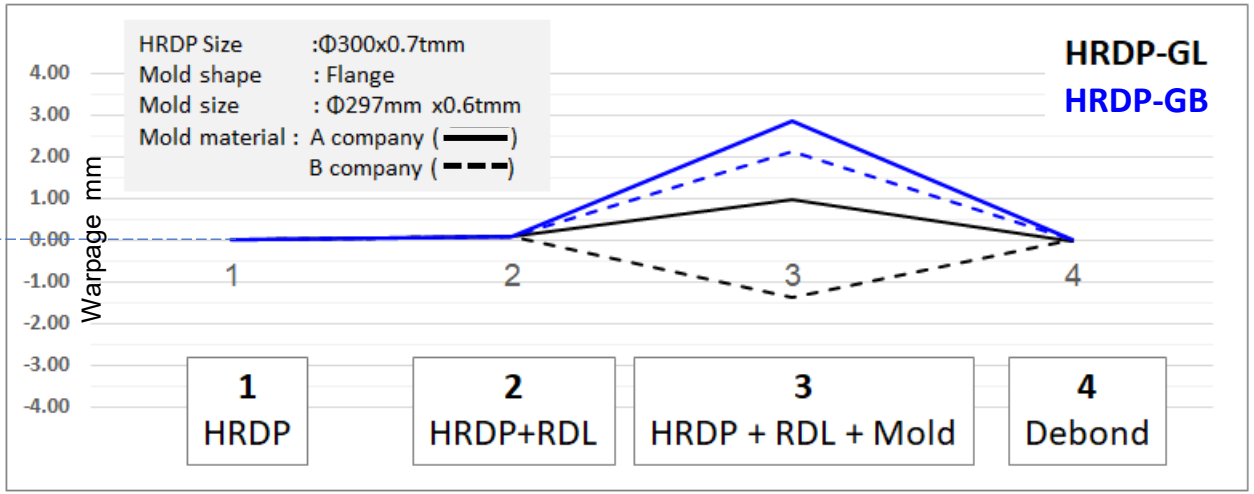
Smile

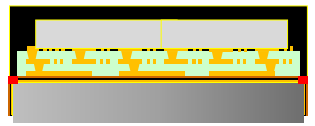
Tensile stress



Cry

Compression stress





4 Debond: RDL+Mold

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Results & Observation

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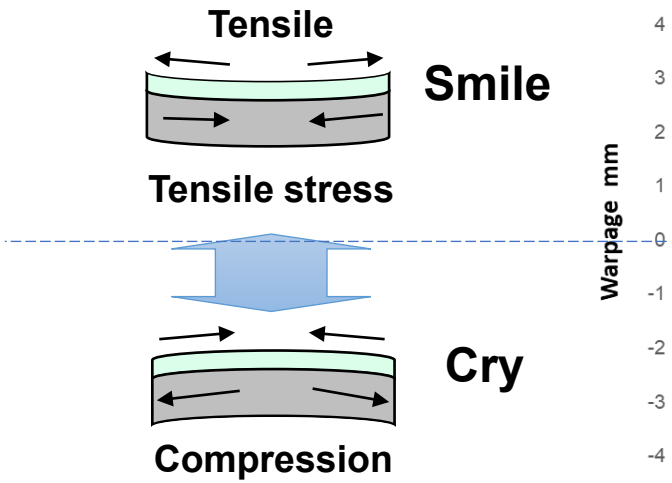
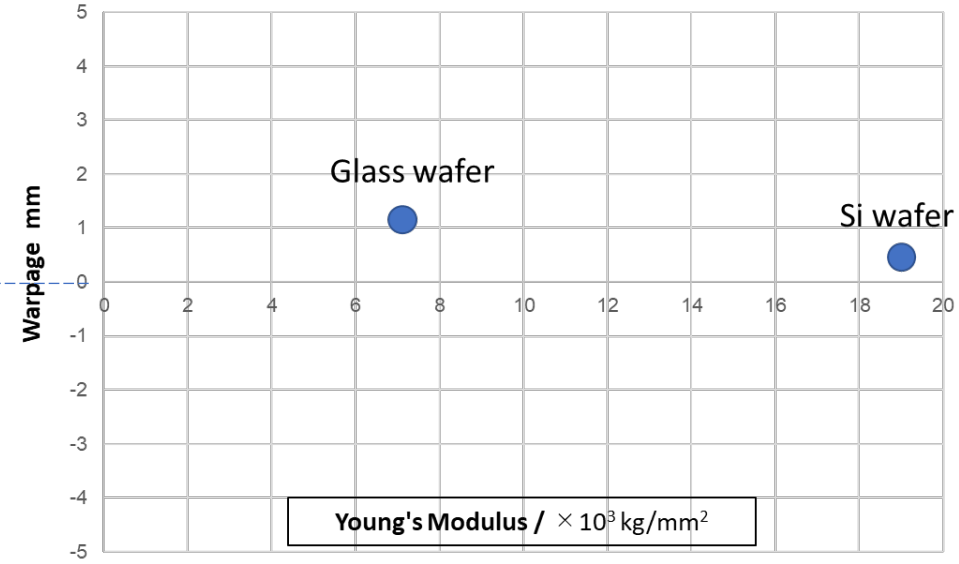
Influence of Carrier type on WARPAGE

Features	Glass	Silicon
	HRDP-GL	HRDP-S
Carrier type	Soda-lime Glass	Silicon Wafer
Molding		
Thickness:	0.7mm	0.7mm





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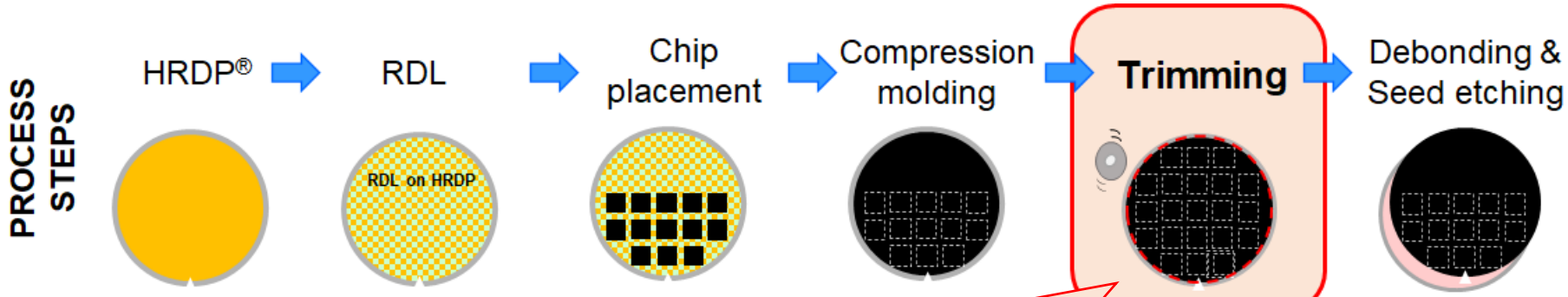
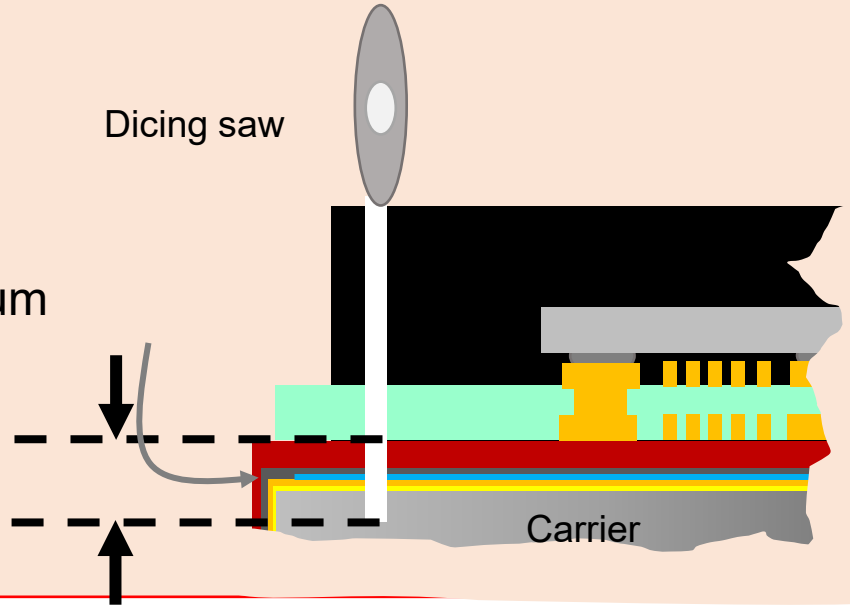
Mechanical debonding steps of Carrier



Cutting depth from carrier surface: <200um



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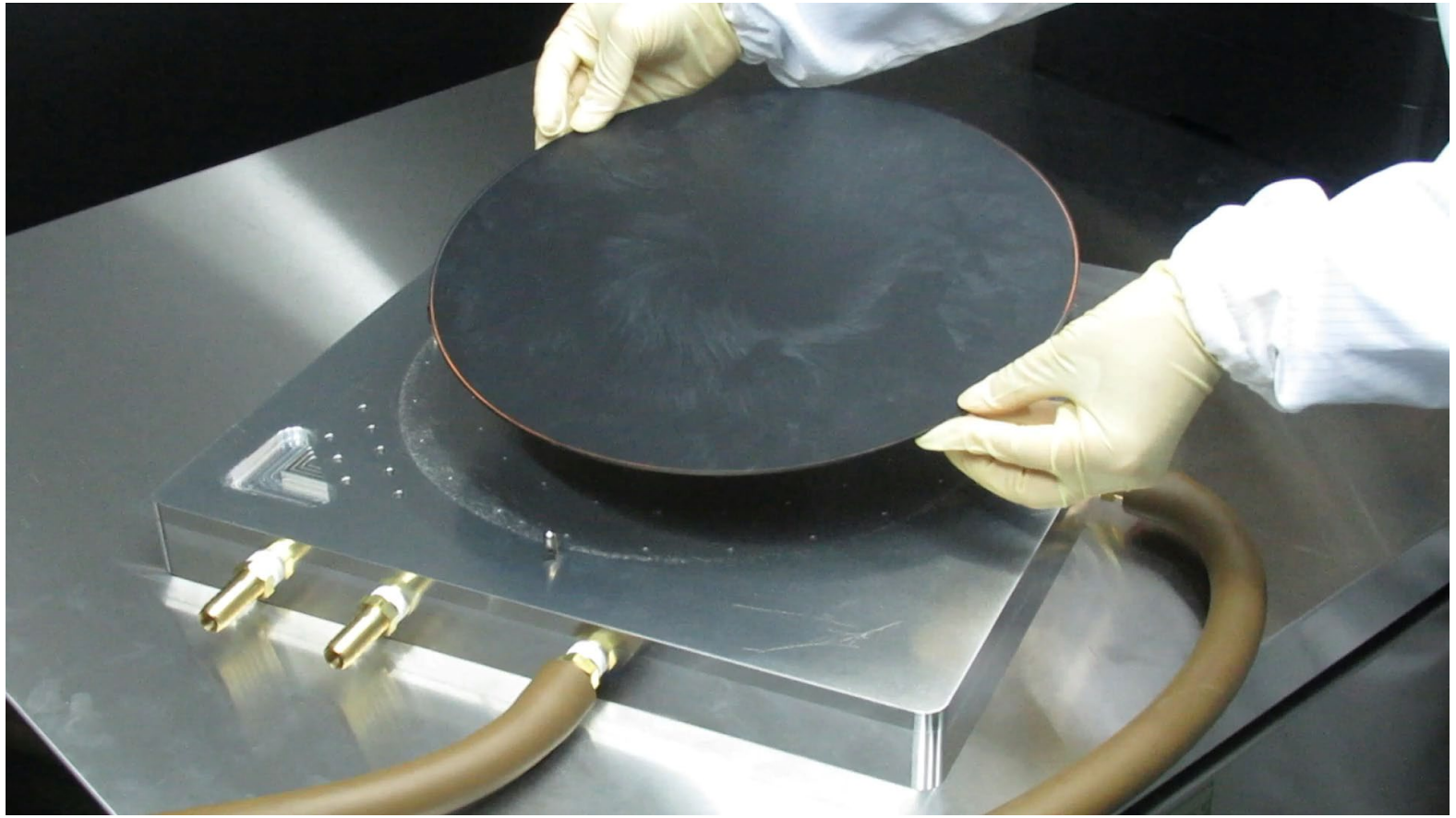
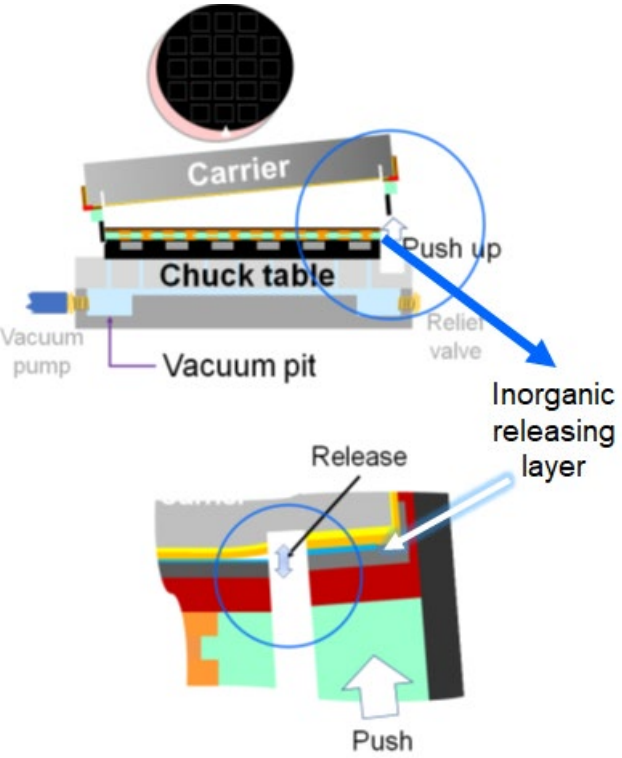
Mechanical Debonding



HRDP Separation

Easy and quick debond by pushing at the edge of carrier



Debonding force: 1.69kgf/cm^2

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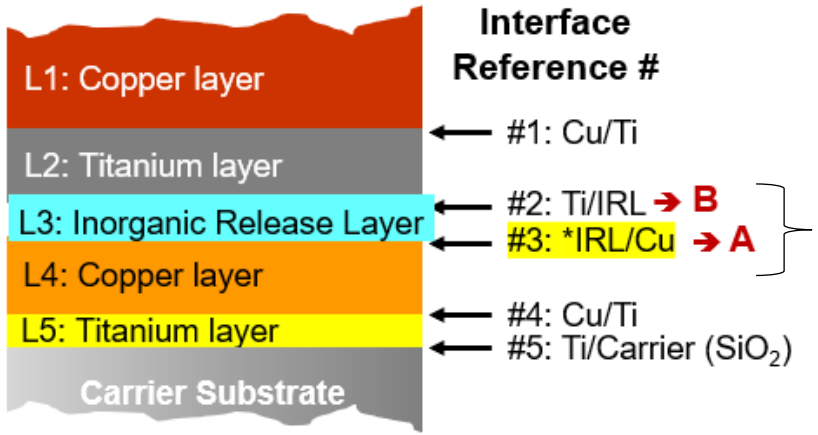
Mechanical Debonding & Weakest Interface

Cleavage Energy (ΔE) between **A** and **B**,

$$\Delta E = \frac{(E_A + E_B) - E_{AB}}{S}$$

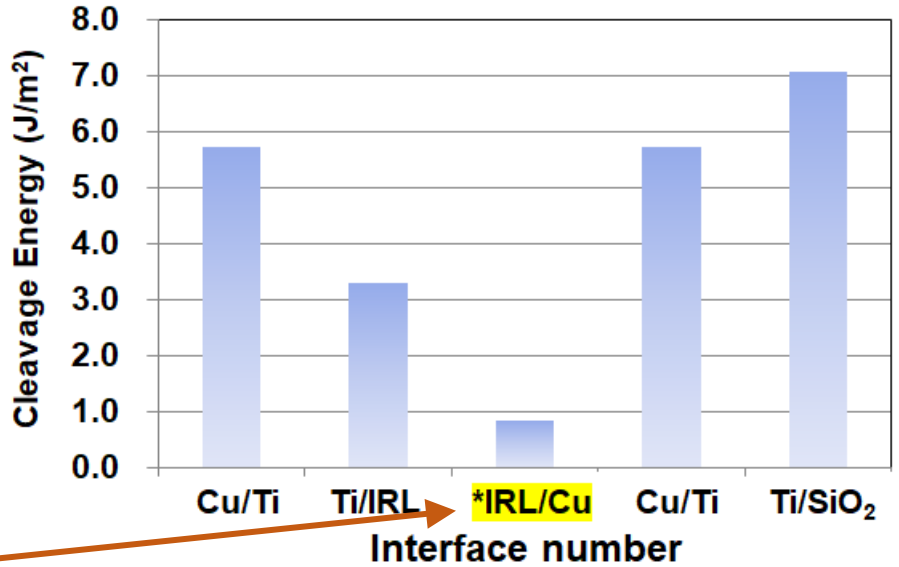
- First Principles Calculation
- Software: Castep
- Methods: DFT-D
- Task: Geometry optimization
- Functional: GGA-PBE
- Energy cutoff: 580eV
- Pseudopotential: OTFG ultrasoft
- Output: Cleavage Energy (ΔE)

HRDP configuration



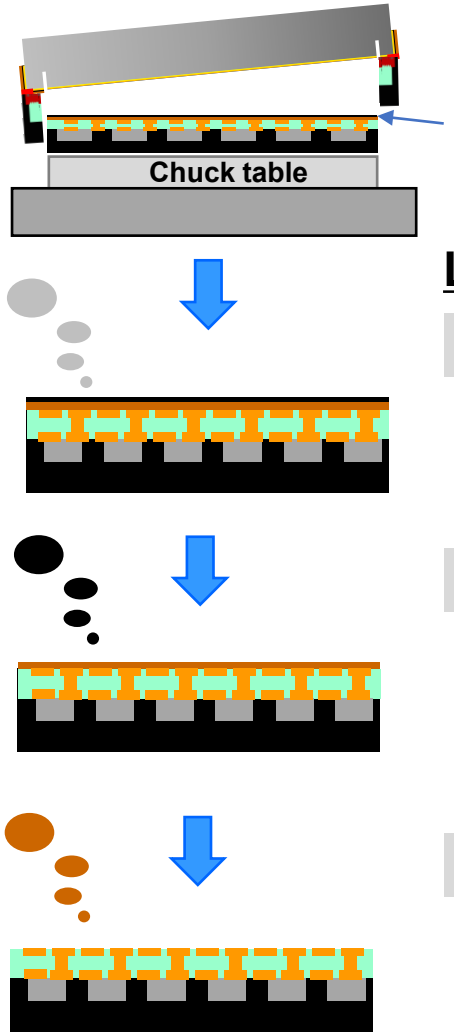
*** IRL: Inorganic Release Layer**

*IRL/Cu separation interface shows the weakest bonding among rest of the interfaces.



Mechanical debonding & Mechanism

Fast & Easy seed layer etching process post-debonding



After HRDP® de-bonding.
the inorganic releasing material
remains on RDL surface.

L1~L3 removal condition

L3 : Inorganic Release Layer

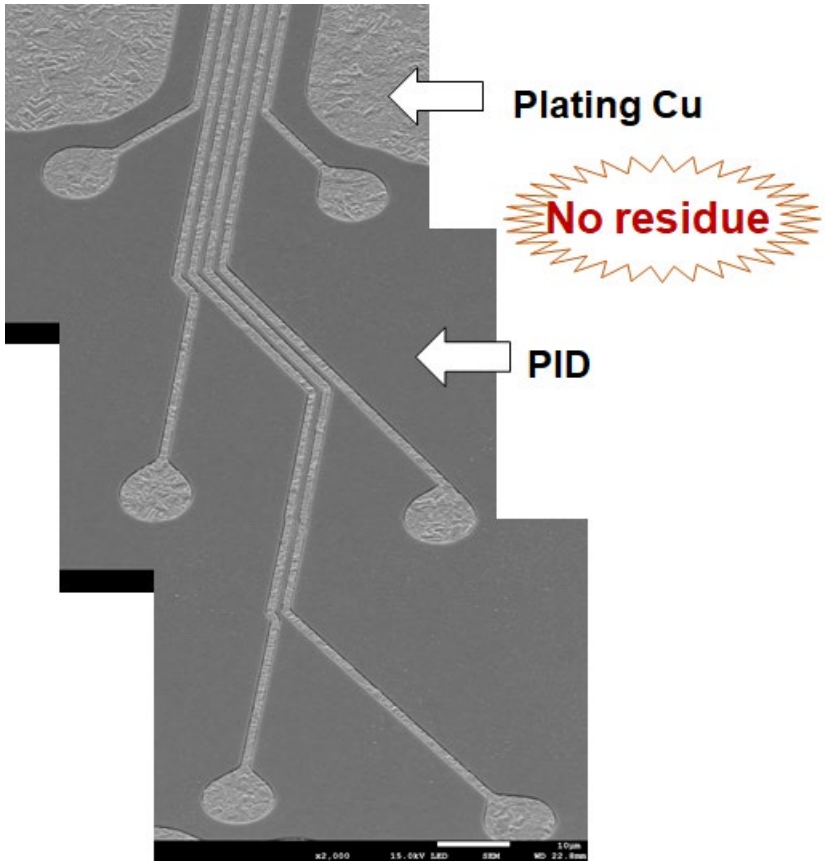
- Process gas: O_2=100scccm
- RF power: 100W (φ200mm)
- Pressure: 5Pa
- Time: 1 min

L2 : Ti layer

- Etchant: Ti etch : TI-3991 (Meltex)
- pH: 9 (Hydrogen peroxide)
- Etching temp.: 40 ℃
- Etching rate: 85 nm/min (90sec)
- Method: Dip

L1 : Cu seed layer

- Etchant: QE7300 (MEC)
- Etching temp. : 25 deg. ℃
- Etching rate : 1.09 um/min (41sec)
- Method: Spray



Expose the embedded
L/S=1/1μm RDL and pads.

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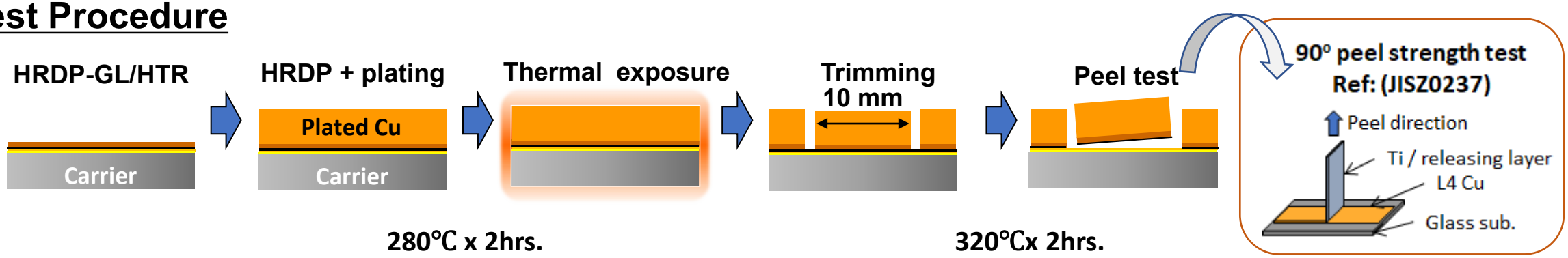
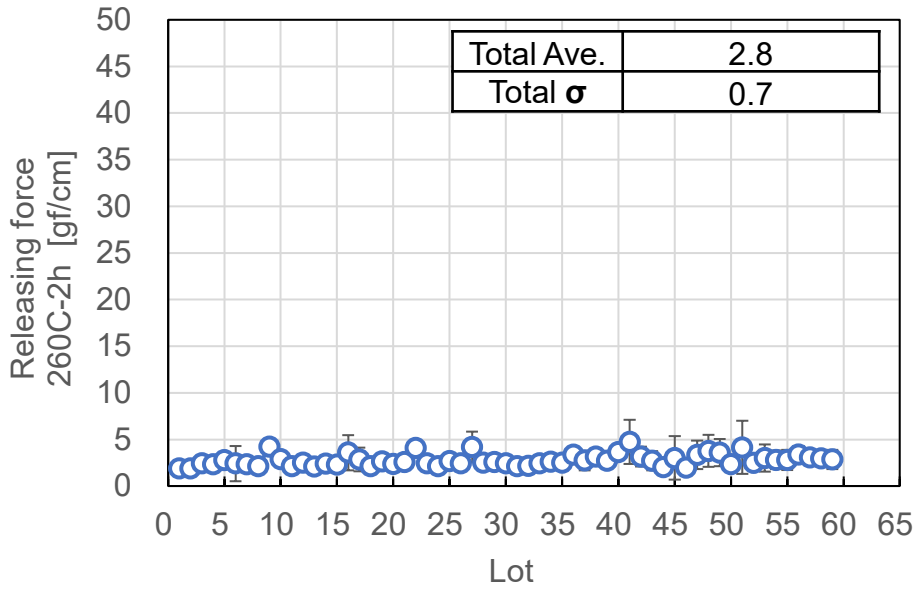
Releasing strength for IRL/Cu interface after processing temperature excursion

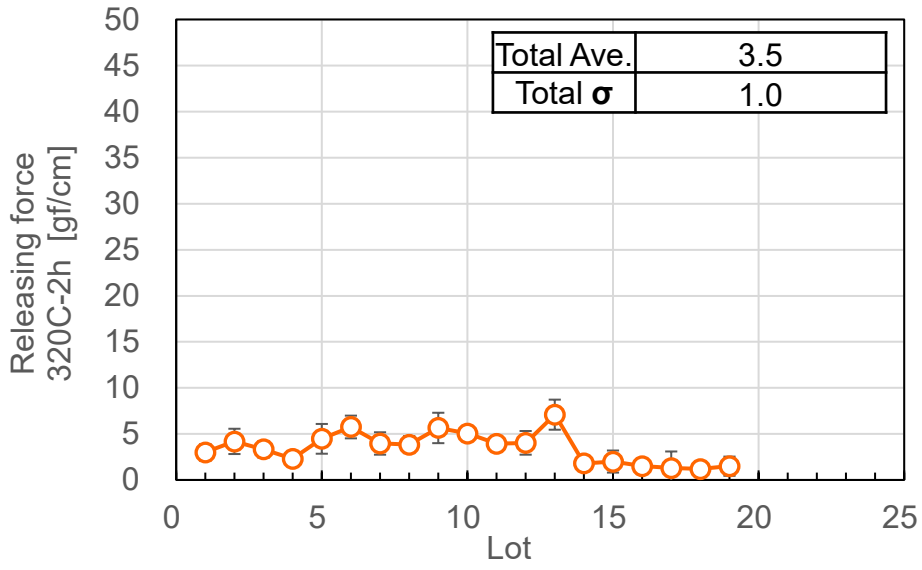
Test Procedure



280℃ x 2hrs.



320℃x 2hrs.



Release force of <30 gf/cm facilitates effective device release during debonding.

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Concluding Remarks

- Selection of Rigid Carrier Substrates & its Release Layer influences quality and productivity of FO-WLP
- Choice of Carrier substrate materials have been established
- There are limitations with currently used ‘polymer release layer’ and their debonding related issues in the industry
- HRDP ® is an alternate new Hybrid Carrier for fine pitch chip last Fan-Out solution, where a novel inorganic release layer is integrated with rigid carriers of choice
- Structure and evaluation results suggest HRDP ® as promising for fine pitch chip last Fan-Out solution
- HRDP ® reduces “total cost of ownership” in assembly