Influence of Rigid Carrier Substrates & its Release Layer on Ultra Fine Pitch chip last FO-WLPs.

Mitsui Mining and Smelting Co., Ltd.,
Business Creation Sector
HRDP Business Development Unit

Yoshinori Matsuura
y_matsuura@mitsui-kinzoku.com

Vivek B. Dutta
Vivek.b.dutta@gmail.com
Presentation Outline

• Introduction
  ➔ Challenges in assembling FO-WLP
  ➔ Need for Carrier substrates & Release Layer

• Requirements for Rigid Carrier Substrates
  ➔ Features (constructed structure)

• Requirements for Release Layer
  ➔ Features (constructed structure)

• Current bonding & Debonding practice in assembly

• Novel alternate solution through HRDP®
  ➔ Features (constructed structure)
  ➔ How does it influence? (Results & Observation)

• Advantages of HRDP® over current practices

• Conclusion
Introduction

Carrier based “Fan-Out Chip last” process flow

**Carrier + Release Film** Provides:
- Ultra fine line RDL (2/2μ \(\geq\) 1/1μ)
- Minimize warpage
- Easy and quick carrier debonding
- Reduce “total cost of ownership”

**INFLUENCE AND CHOICE OF**
- TEMPORARY CARRIERS
- RELEASE FILMS
  WILL BE FOCUSSED
  IN THIS TALK
Warpage during Assembly

Processed Wafer

Background Wafer with chips

Processed through final packaging

Assembled Structure

Primary reason for WARPAGE is CTE mismatch between various materials used in package ~ especially after molding

If FO-WLP assembly process is not carefully designed, then it is likely to result in WARPAGE, causing yield loss

WARPAGE Types

(a) Warpage Mode: CRYING (negative (-) sign)
(b) Warpage Mode: SMILING (positive (+) sign)
(a) + (b) Warpage Mode: TWIST
Need for Carrier Substrate

To Control Warpage

Requirements of Carrier Substrates:
- High Rigidity (*i.e.*, high modulus)
- CTE close to bulk CTE of assembly structure materials
- Good surface flatness

Substrates **MATERIALS** used:
- CTE matched **Borosilicate Glass**
- **Soda-lime Glass**
- **Silicon** (thicker than silicon device)
Need for Release Layer

**PURPOSE**

RELEASE LAYER bonds carrier & grows RDL with the wafer and finally releases assembled wafer before singulation process.

**STRUCTURE**

- Overmolding
- Dies from wafer
- RDLs
- Release Layer
- Rigid Carrier
- RDL on Carrier Substrate

**PREPARATION STEPS**

1. Glass Carrier
2. Wash
3. Release Layer Coating
4. OR
5. Lamination
6. Panel Inspection
7. Sputter Ti/Cu
8. Cure
9. Ready for ASSL’Y
Release Layer Separation

CURRENT SOLUTIONS

ISSUES in DEBONDING using current solutions:

During Preparation (pre-assembly) –
- Contamination
- Surface Roughness
- Flatness /Thickness
- Porosity / Pinholes
- Material loss in spin coating (>60%)

During Assembly Process –
- Adds to preparation time, quality & cost
- Surface Roughness & Planarization of 1st layer RDL patterns \(\Rightarrow\) limiting fine L/S RDL resolution
- Heterogeneous separation during debonding

LIMITATION: Cannot feature < 2/2\(\mu\) L/S pitch RDL for chip last FO-WLPs
New platform carrier solution ➔ HRDP®
(High Resolution Debondable Panel) Technology

☀ Most compatible solution for Fan-Out chip last process
  ➔ Capabilities for ultra-fine RDL structures (<2μm L/S)
  ➔ Lithography can be done directly on copper seed layer of flat HRDP®, thus eliminating seed layer sputter during 1st RDL
  ➔ Smooth sputtered carrier surface, resulting in increased assembly yield.

☀ Wafer Level & Panel Level Packaging Capability in varied dimensions
☀ Release Layer is made of 100% inorganic material,
☀ Stabilizes dimensions and minimizes warpage during assembly work in progress
☀ Easy & low release force at room temperature mechanical debonding of Inorganic releasing material – with low release energy and increased UPH
☀ Simple “Drop-in Solution”, eliminating conventional carrier preparation process steps & issues associated with them.
☀ During processing, this inorganic release layer (IRL) demonstrates higher chemical resistance and heat resistance than alternative technology such as the laser lift-off (LLO) release layer.
About HRDP®

- HRDP® carrier is offered in various dimensions and thicknesses as round wafers and square/rectangular panels with glass or silicon to match customer’s CTE requirements.
- Inorganic Release Layer (IRL) is laid sandwiched between flat sputtered layers.

Product Configuration

Panel format  
(a) Exterior  
Wafer format  
(b) Structure

- L1; Copper layer (0.3um) (SEED LAYER)
- L2; Titanium layer (0.1um)
- L3; Inorganic releasing layer*
- L4; Copper layer
- L5; Titanium layer

Total Function Layers 0.65um thin
## HRDP® Product Offerings by Carrier Material Types

<table>
<thead>
<tr>
<th>Features</th>
<th>Glass</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HRDP-GL</td>
<td>HRDP-GB</td>
</tr>
<tr>
<td>Carrier type</td>
<td>Soda-lime Glass</td>
<td>Borosilicate Glass</td>
</tr>
<tr>
<td>Carrier CTE※1</td>
<td>8.5</td>
<td>3.4~12.1※2</td>
</tr>
<tr>
<td>Carrier Size Format (mm)</td>
<td>Wafer : φ200 &amp; φ300</td>
<td>Wafer ※2 : φ200 &amp; φ300</td>
</tr>
<tr>
<td></td>
<td>Panel : 200 × 200~600 × 600</td>
<td>Panel ※2 : 200 × 200~600 × 600</td>
</tr>
<tr>
<td>Carrier Thickness</td>
<td>0.7mm, 1.1mm, 1.8mm</td>
<td>0.7mm~1.8mm※2</td>
</tr>
<tr>
<td>Total Thickness Variation (TTV)</td>
<td>≤20um</td>
<td>≤5um</td>
</tr>
<tr>
<td>Young's Modulus</td>
<td>$7.5 \times 10^3$ kg/mm$^2$</td>
<td>$7.4 \times 10^3$ kg/mm$^2$</td>
</tr>
</tbody>
</table>

Notes: ※1 CTE is a reference value. ※2 Specific application specific CTE & Rigidity can be customized.
### Physical Properties

<table>
<thead>
<tr>
<th></th>
<th>Soda Lime</th>
<th>Borosilicate</th>
<th>Silicon</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>2.5</td>
<td>2.4</td>
<td>2.5</td>
<td>2.3 $\times 10^3$ kg/m³</td>
</tr>
<tr>
<td>Young's Modulus</td>
<td>7.5</td>
<td>7.4</td>
<td>7.3</td>
<td>19.3 $\times 10^3$ kg/mm²</td>
</tr>
<tr>
<td>Poisson's Ratio</td>
<td>0.22</td>
<td>0.23</td>
<td>0.21</td>
<td>N/A</td>
</tr>
<tr>
<td>Mohs Hardness</td>
<td>6.5</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Thermal Expn. (CTE)</td>
<td>8.5</td>
<td>3.4</td>
<td>9.4</td>
<td>3.6 $\times 10^{-6}$ °C (at 20-350°C)</td>
</tr>
<tr>
<td>Specific Heat</td>
<td>0.19</td>
<td>0.77</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Thermal Conduct.</td>
<td>0.86</td>
<td>N/A</td>
<td>N/A</td>
<td>160 kcal/m·h·°C</td>
</tr>
<tr>
<td>Strain Point</td>
<td>523</td>
<td>669</td>
<td>553</td>
<td>N/A</td>
</tr>
<tr>
<td>Annealing Point</td>
<td>540-560</td>
<td>722</td>
<td>602</td>
<td>N/A</td>
</tr>
<tr>
<td>Softening Point</td>
<td>720-740</td>
<td>971</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Process Flow Comparison

CONVENTIONAL ORGANIC RELEASE LAYER PREPARATION STEPS:

Glass Carrier → Wash → Release Layer Coating On Carrier Wafers / Panels → Cure → Ti/Cu Sputter → Insp.

ASSEMBLY PROCESS STEPS

Inspection → RDL → Chip placement → Compression molding → Trimming → Debonding & Seed etching

HRDP® increases productivity
Fan Out Chip Last process flow using HRDP®
Manufacturing of HRDP®

Glass inspection
- Brush roll
- Alkaline cleaning
- Ultrasonic cleaning

Carrier cleaning
- Particle monitor during sputtering
- Automatic particle inspection
- Film thickness measurement etc.

Function layers sputtering

HRDP® inspection

Packing and shipping
- Panel packing
- Wafer packing

Clean room; Class 100

Sputtered Structure
- L1: Copper layer (0.3μm) (SEED LAYER)
- L2: Titanium layer (0.1μm)
- L3: Inorganic releasing layer
- L4: Copper layer
- L5: Titanium layer

HRDP after sputtering (Wafer format: Φ300mm)

Panel packing
Wafer packing
HRDP® helps lithography process optimize to form L/S of 2/2μm & below

<table>
<thead>
<tr>
<th>Process</th>
<th>Company</th>
<th>Material / Equipment</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier</td>
<td>Mitsui</td>
<td>HRDP-GL (CTE: 8.5)</td>
<td>Wafer: φ300mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HRDP-GB (CTE: 4.6)</td>
<td>Panel: 320mm sq.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HRDP-S (CTE: 3.6)</td>
<td>Thickness: 0.7mm, 1.1mm</td>
</tr>
<tr>
<td>Photo resist</td>
<td>Sumitomo</td>
<td>XI-4920 (Liquid type)</td>
<td>Thickness: 4um</td>
</tr>
<tr>
<td></td>
<td>Chemi.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposure</td>
<td>Canon</td>
<td>Stepper: FPA-5520iV</td>
<td>Photo resist: 1600J/m²</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Expose area 52x68mm)</td>
<td>Photo Via: Dose 4500J/m²</td>
</tr>
<tr>
<td>Pattern plating</td>
<td>UYEMURA</td>
<td>Copper plating</td>
<td>Thickness: 2um</td>
</tr>
<tr>
<td>PID (Photo Imageable</td>
<td>A company</td>
<td>Liquid/Negative-type</td>
<td>Thickness: 5um</td>
</tr>
<tr>
<td>Dielectric)</td>
<td></td>
<td></td>
<td>Via: φ8um, φ10um, φ15um, φ18um</td>
</tr>
<tr>
<td>Molding compound</td>
<td>B company</td>
<td>Granule type</td>
<td>Thickness: 600um</td>
</tr>
<tr>
<td></td>
<td>C company</td>
<td>Granule type</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D company</td>
<td>Liquid type</td>
<td></td>
</tr>
<tr>
<td>Mold equipment</td>
<td>TOWA</td>
<td>Compression mold</td>
<td>Wafer: φ297mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Panel: 300mm sq.</td>
</tr>
</tbody>
</table>

* Molding compound cure condition
  - A: In-mold cure temp. and time: 150°C x 10min , Post-mold curing temp. and time: 175°C x 6hr
  - B: In-mold cure temp. and time: 150°C x 5min , Post-mold curing temp. and time: 150°C x 4hr
  - C: In-mold cure temp. and time: 125°C x 10min , Post-mold curing temp. and time: 150°C x 1hr
**HRDP® helps lithography process optimize to form L/S of 2/2 and finer**

<table>
<thead>
<tr>
<th>Line &amp; Space width</th>
<th>0.8/0.8 μm</th>
<th>1.0/1.0 μm</th>
<th>1.2/1.2 μm</th>
<th>1.5/1.5 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aspect ratio</td>
<td>2.1</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
</tr>
<tr>
<td>After photoresist strip (x 10000)</td>
<td><img src="1" alt="Image" /></td>
<td><img src="2" alt="Image" /></td>
<td><img src="3" alt="Image" /></td>
<td><img src="4" alt="Image" /></td>
</tr>
</tbody>
</table>

- Cu plating thickness: 2.1μm
- Carrier: HRDP-GL (φ300mm wafer format)
Process Optimize to form fine photo via

<table>
<thead>
<tr>
<th>Via diameter</th>
<th>φ8μm</th>
<th>φ10μm</th>
<th>φ15μm</th>
<th>Φ20μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aspect ratio</td>
<td>0.4</td>
<td>0.32</td>
<td>0.21</td>
<td>0.16</td>
</tr>
<tr>
<td>After PID development</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tilt 30° (x 5,000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via diameter (Bottom)</td>
<td>7.5μm (σ: 0.3)</td>
<td>10.7μm (σ: 0.2)</td>
<td>15.2μm (σ: 0.2)</td>
<td>21.3μm (σ: 0.4)</td>
</tr>
</tbody>
</table>

- Carrier: HRDP-GL (CTE: 8.5), φ300mm Wafer format
- PID thickness: 5.3μm

- Δ variation in wafer

<table>
<thead>
<tr>
<th></th>
<th>HRDP-GL</th>
<th>HRDP-GB</th>
<th>HRDP-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.5 (σ:0.1)</td>
<td>3.4 (σ:0.2)</td>
<td>3.7 (σ:0.1)</td>
</tr>
<tr>
<td>B</td>
<td>3.3 (σ:0.1)</td>
<td>3.2 (σ:0.1)</td>
<td>3.6 (σ:0.1)</td>
</tr>
</tbody>
</table>
High chemical resistance during wet processing against variety of chemicals

<table>
<thead>
<tr>
<th>Chemicals</th>
<th>temperature/processing time</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Discoloration</td>
</tr>
<tr>
<td>DI water</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td>5wt% KOH</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Discoloration</td>
</tr>
<tr>
<td>DMSO</td>
<td>RT/10min,30min,6 hours</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 hours:Pass</td>
</tr>
<tr>
<td>NMP</td>
<td>RT/10min,30min,6 hours</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 hours:Pass</td>
</tr>
<tr>
<td>Acetone</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td>EtOH</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td>2wt% H₂SO₄</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
<tr>
<td>TMAH aq. (2.38%)</td>
<td>RT/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Discoloration</td>
</tr>
<tr>
<td>※ PR stripper (ST-120)</td>
<td>50°C/10min,30min</td>
<td>10min:Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30min:Pass</td>
</tr>
</tbody>
</table>

HRDP® has excellent resistance to all processing chemicals customarily used.

※ ST-120; made by TOK Co., It consists of DMSO, TMAH, NMP, Glycol etc.
## WARPAGE after Molding

<table>
<thead>
<tr>
<th>Features</th>
<th>Glass</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HRDP-GL</td>
</tr>
<tr>
<td>Carrier type</td>
<td>Soda-lime Glass</td>
</tr>
<tr>
<td>Molding</td>
<td></td>
</tr>
<tr>
<td>Thermal Expn. (CTE)</td>
<td>8.5 ppm</td>
</tr>
</tbody>
</table>

### Diagram

- **Carrier**
- **Smile**
- **Tensile stress**
- **Cry**
- **Compression stress**

4 Debond: RDL+Mold
### Influence of Carrier type on WARPAGE

<table>
<thead>
<tr>
<th>Features</th>
<th>Glass</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HRDP-GL</td>
<td>HRDP-S</td>
</tr>
<tr>
<td>Carrier type</td>
<td>Soda-lime Glass</td>
<td>Silicon Wafer</td>
</tr>
<tr>
<td>Molding</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thickness:</td>
<td>0.7mm</td>
<td>0.7mm</td>
</tr>
</tbody>
</table>

#### Results & Observation

**Tensile**
- Stress causing elongation

**Smile**
- Induced by internal stresses

**Compression**
- Opposite to tension

![Graph showing tensile stress and compression effects on glass and silicon wafers](image)

- **Glass wafer**
  - Young’s Modulus $\times 10^5$ kg/mm²

- **Si wafer**
  - Young’s Modulus $\times 10^5$ kg/mm²
Mechanical debonding steps of Carrier

Cutting depth from carrier surface: <200um
Mechanical Debonding

Debonding force: 1.69kgf/cm²

HRDP Separation

Easy and quick debond by pushing at the edge of carrier
Mechanical Debonding & Weakest Interface

Cleavage Energy (ΔE) between A and B,

\[
\Delta E = \frac{(E_A + E_B) - E_{AB}}{S}
\]

- First Principles Calculation
- Software: Castep
- Methods: DFT-D
- Task: Geometry optimization
- Functional: GGA-PBE
- Energy cutoff: 580eV
- Pseudopotential: OTFG ultrasoft
- Output: Cleavage Energy (ΔE)

*IRL/Cu separation interface shows the weakest bonding among rest of the interfaces.
**Mechanical debonding & Mechanism**

**Fast & Easy seed layer etching process post-debonding**

After HRDP® de-bonding, the inorganic releasing material remains on RDL surface.

**L1~L3 removal condition**

**L3 : Inorganic Release Layer**
- Process gas: $O_2=100$scccm
- RF power: 100W ($\phi 200$mm)
- Pressure: 5Pa
- Time: 1 min

**L2 : Ti layer**
- Etchant: Ti etch : TI-3991 (Meltex)
- pH: 9 (Hydrogen peroxide)
- Etching temp.: 40 $^\circ$C
- Etching rate: 85 nm/min (90sec)
- Method: Dip

**L1 : Cu seed layer**
- Etchant: QE7300 (MEC)
- Etching temp.: 25 deg. $^\circ$C
- Etching rate: 1.09 um/min (41sec)
- Method: Spray

Expose the embedded L/S=1/1μm RDL and pads.
Releasing strength for IRL/Cu interface after processing temperature excursion

**Test Procedure**

1. **HRDP-GL/HTR**
2. **HRDP + plating**
3. **Plated Cu**
4. **Carrier**
5. **Thermal exposure**
6. **Trimming 10 mm**
7. **Peel test**

**Results**

- **280°C x 2hrs.**
  - Total Ave.: 2.8
  - Total σ: 0.7

- **320°C x 2hrs.**
  - Total Ave.: 3.5
  - Total σ: 1.0

**Notes**

- Releasing force of <30 gf/cm facilitates effective device release during debonding.

---

**Ref:** (JISZ0237)

**Peel direction**

- Ti / releasing layer
- L4 Cu
- Glass sub.
Concluding Remarks

- Selection of Rigid Carrier Substrates & its Release Layer influences quality and productivity of FO-WLP
- Choice of Carrier substrate materials have been established
- There are limitations with currently used ‘polymer release layer’ and their debonding related issues in the industry
- HRDP® is an alternate new Hybrid Carrier for fine pitch chip last Fan-Out solution, where a novel inorganic release layer is integrated with rigid carriers of choice
- Structure and evaluation results suggest HRDP® as promising for fine pitch chip last Fan-Out solution
- HRDP® reduces “total cost of ownership” in assembly
To: the Participants

Thank you

MITSUI KINZOKU

Mitsui Mining and Smelting Co., Ltd.