Mask-less Laser Direct Imaging & Adaptive Patterning for Fan-Out Heterogeneous Integration

Clifford Sandstrom, VP of Technology Development of Deca

Tim Olson, CEO of Deca

Deca Contributing Authors

Cliff Sandstrom – VP of Technology Development

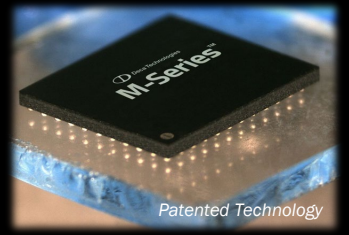
Cliff is VP of Technology for Deca Technologies where he has been since 2010. Previously, Cliff was Director of Research & Development at Cypress Semiconductor. During his tenure at Cypress, Cliff was the Program Manager for the front-end 90 and 65nm technologies from 2005 to 2009 leading groups on 30+ project launches with 25 entering production. He guided teams of 100+ engineers from various disciplines and sites in the development of Cypress Semiconductor products.

Tim Olson – Founder, CEO & Board Member

Tim Olson founded Deca Technologies in 2009 with a mission to transform the way the world creates advanced electronic products. Currently CEO, he has also served as CTO, while continuously serving as a board member. Throughout his career, Tim led multiple breakthrough innovations. As Senior VP of Amkor Technology, he led global research and development, introducing Package-on-Package Through Mold Via (PoP TMV) technology, FusionQuad, and the industry's first high-volume fine pitch Cu pillar flip-chip. As Executive VP of Products and Operations at Micro Component Technology, Tim led development of specialized equipment and software establishing the industry's first high-volume strip-based test. While at Motorola Semiconductor, Tim led creation of the PRISM highly automated and integrated assembly and test factory bringing 2D codes from NASA to semiconductors for tracking and traceability.

Brief Introduction to Deca

- Born of a passion to create breakthrough electronic interconnect solutions
- Based on 10X thinking, inspired by *Greek **déka*** (δέκα)
- 10X order-of-magnitude breakthroughs: M-Series™ & Adaptive Patterning®



M-Series

Chips first, chips up fan-out technology

Adaptive Patterning™

Patented Technology

Adaptive Patterning

Real-time optimized design-during-manufacturing (every device on every wafer)

Deca's Investors

Infineon

Previously CYPRESS

Qualcomm

Deca's current licensees

ASE GROUP 日月光集團

nepes corporation

skywater

maxeon POWERING POSITIVE CHANGE

Previously SUNPOWER

*Deca has become the #1 independent technology development & licensing company in the industry**

**Fan-out WLP & PLP Technologies 2021- Markets & Technology Report, June 2021*

Outline

- Mask-Less Laser Direct Imaging (LDI) Lithography
- LDI Advantages
- LDI Challenges
- Background on Die Shift
- Adaptive Patterning
- Gen 2 RDL and Via Imaging
- Conclusion

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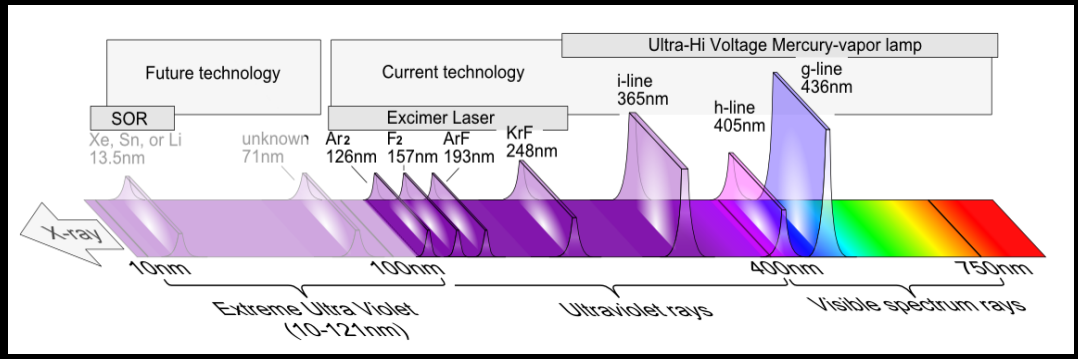
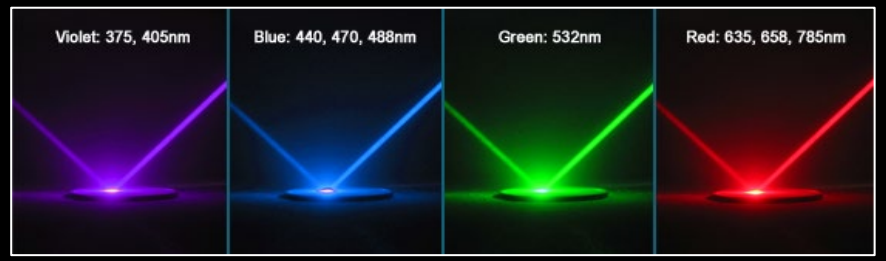
Mask-Less Laser Direct Imaging (LDI) Lithography

Two key mask-less technologies:

1. Electron beam lithography (e-beam)
   - Write field < 1 mm^2
   - Small features, <10 nm
   - Slow, costly and in a vacuum
   - Typical application front-end mask creation
2. Laser Direct Imaging (LDI)
   - Write Field > 500 mm^2
   - Features typically >10 µm
   - Low cost
   - Typical application PCB



https://www.allresist.com/forays-through-the-lithography-of-microelectronics-matthias-schirmer/



https://www.pro-lite.co.uk/File/diode_laser_modules.php

The LDI equipment market includes the following categories of products:

1. Polygon mirrors, typically line scan at 355 nm
2. Grating light valve, free-standing silicon-nitride ribbons on a silicon chip, linear scan
3. Digital Micromirror Device (DMD), area scan at 405 nm

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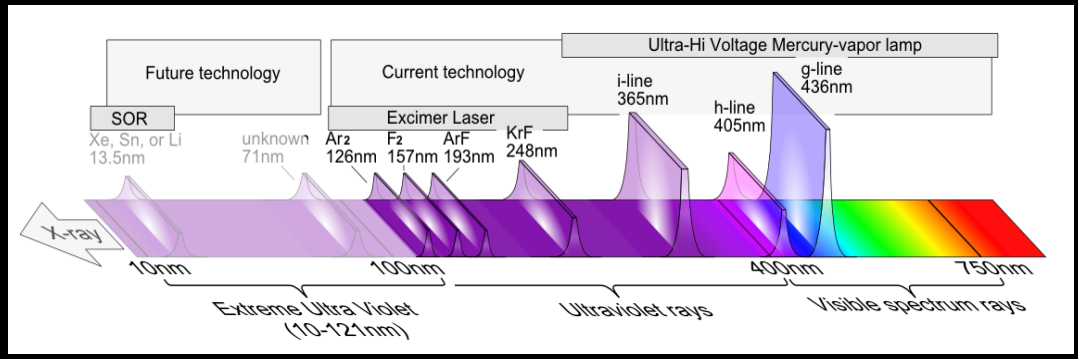
   - Typical application PCB (why not advance packaging?)



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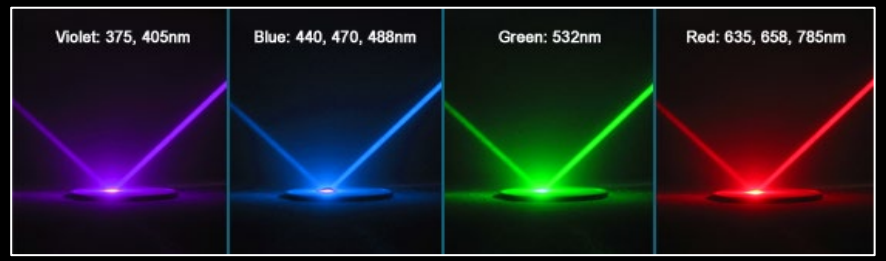

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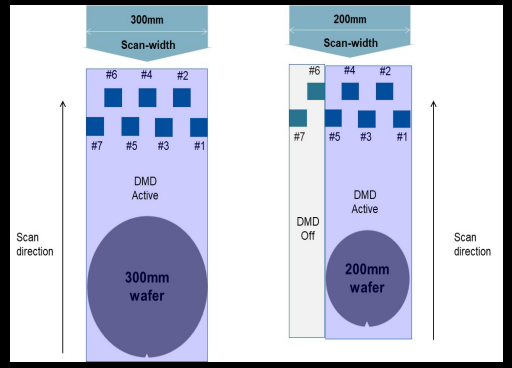
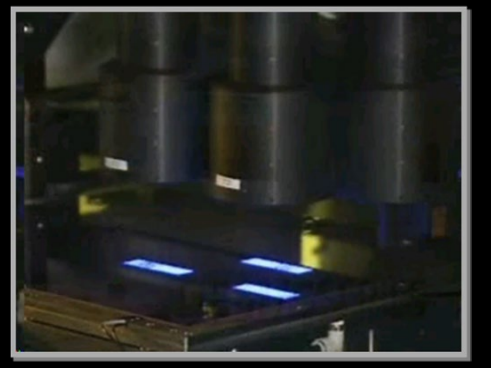
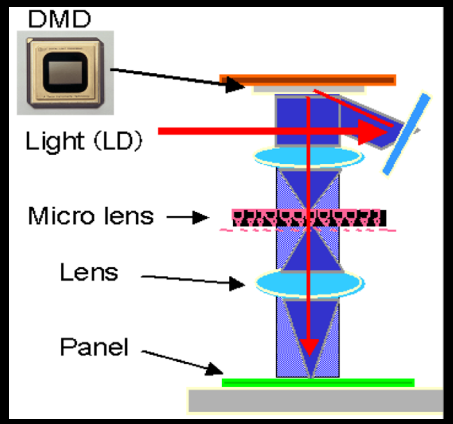
The presentation will focus on DMD LDI applications using 405 nm

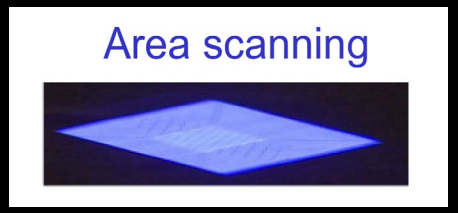
Mask-Less Laser Direct Imaging (LDI) Lithography

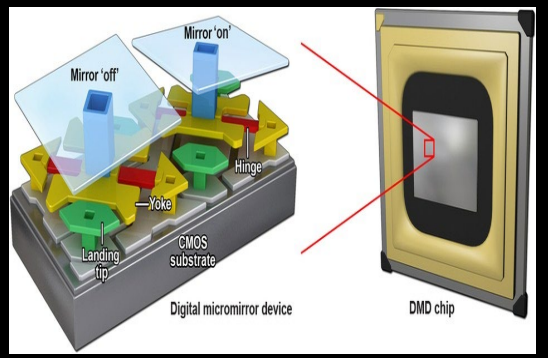
- Tools originally adapted from Hitachi Via Mechanics (now ADTEC Engineering)
- Supports formats of 200 mm, 300 mm and up to 600 mm
- Multiple exposure engines using a solid-state laser (single scan 300 mm, dual 600 mm)
- Laser beam is guided horizontally over the wafer or panel with spot sizes < 3.5 µm and throughput 55 to 110 WPH on 300 mm
- During the scanning movement, the beam is switched on or off in fractions of a second
- DMDs consist of rectangular arrays of microscopic mirrors, deflected between 'on' and 'off' positions separated by an a 12° tilt
- Data resolution currently at 1.0 µm on Gen 1 tool moving to 250 nm on Gen 2

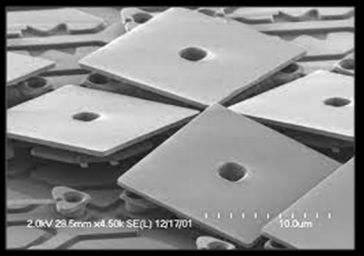












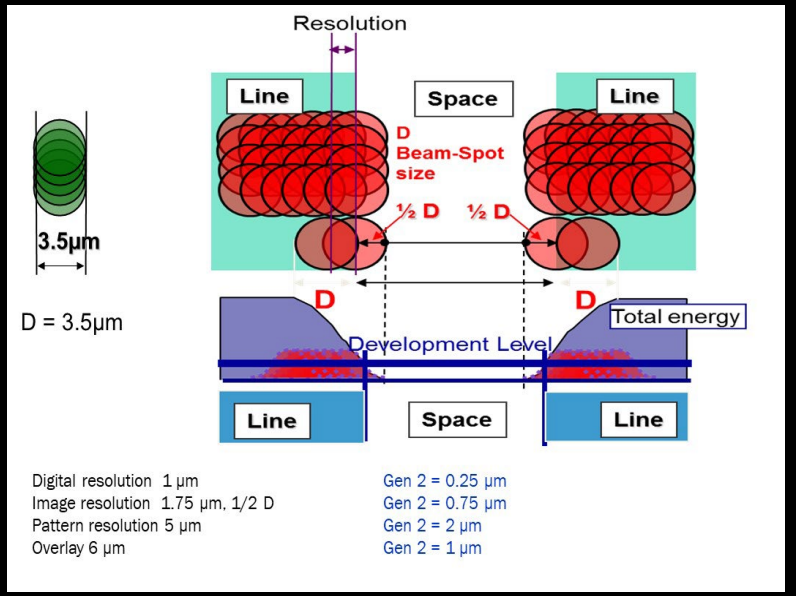
https://people.eecs.berkeley.edu/~pister/147fa16/Lectures/Ming_Wu_Optical_MEMS_2016.pdf

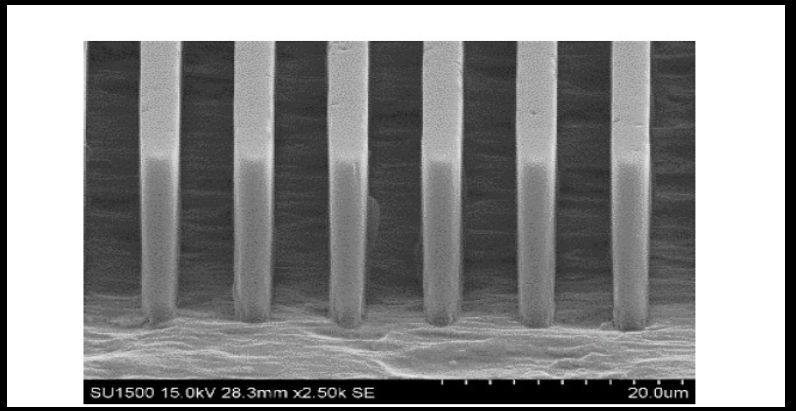
Gen1 Tool Development

Deca drove several custom enhancements to original PCB platform to meet current and future requirements including:

- Enhanced optics, spot size reduction
- Added a sufficient active exposure area to support a 300mm and 600mm formats
- Vision system upgrades (hardware and software, ported from front-end)
- Integrated FOUP wafer handler and pre-aligner
- SECS GEM and SMEMA
- Enhanced temperature control for tighter overlay
- Enhancements to the frame for tighter overlay
- Ceramic chuck for tighter overlay and CD control
- APC integration & algorithms
- Data transfer bandwidth enhancements (fiber optics replaced cabling)
- Software for GDSII data management (vs Gerber)

Next generation includes driving overlay, imaging (mixed wavelengths), and enhanced productivity

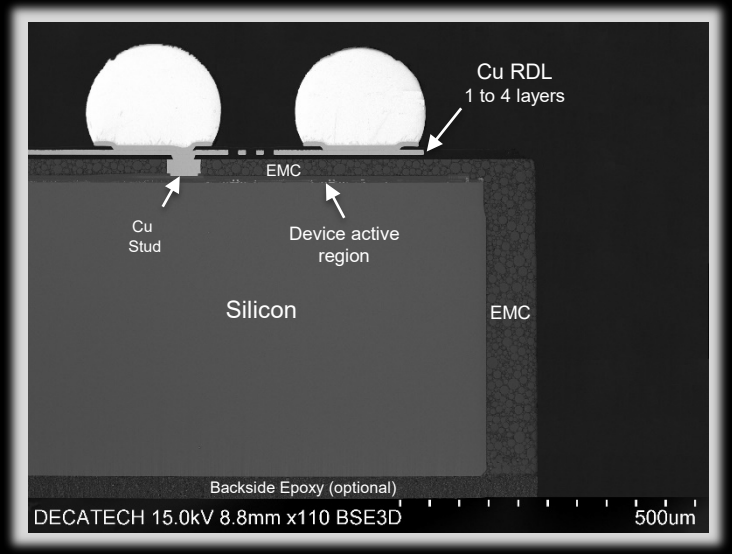




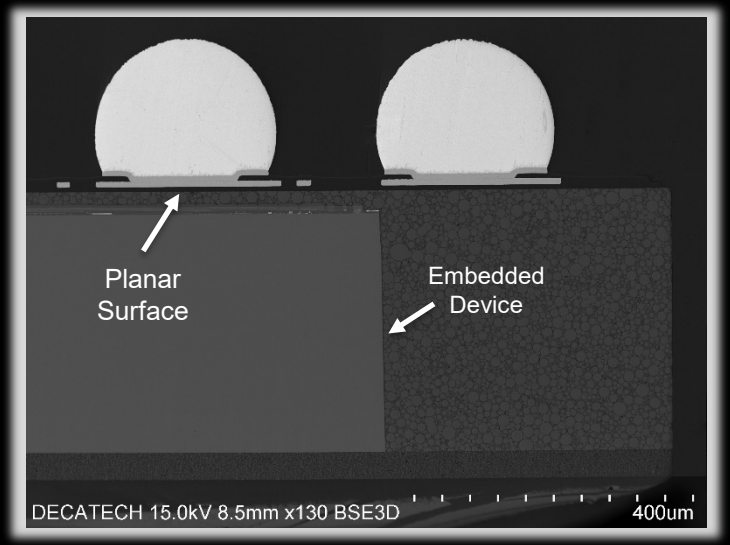
Example of a dry film at 4µm line & space

LDI Success in High Volume Fan-out Production

Over 2.5 billion M-Series fan-out devices shipped using LDI by Deca's licensees



Protected Fan-in



Protected Fan-out

ASE GROUP 日月光集團

&

nepes corporation

M-Series currently the #1 fan-out technology in volume production

... over 3.5 million devices shipping per day

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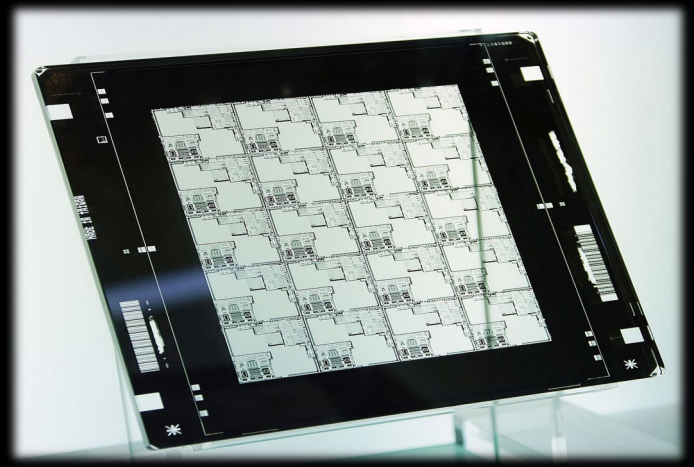
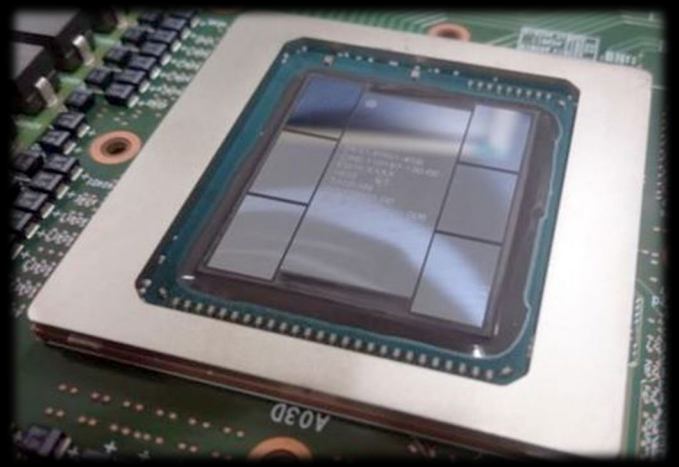
LDI Eliminates Reticle Size Limitations

- Conventional stepper mask-based lithography requires the use of glass reticles
- Complex processor + HBM memory integration exceeding reticle limit, typically around 850mm^2
- Customers asking for 36mm x 36mm (1,296mm^2) to 85mm x 85mm (7,225mm^2)
- Reticle stitching often required resulting in significant stepper throughput loss & reduced resolution



.wikipedia.org/wiki/Photomask

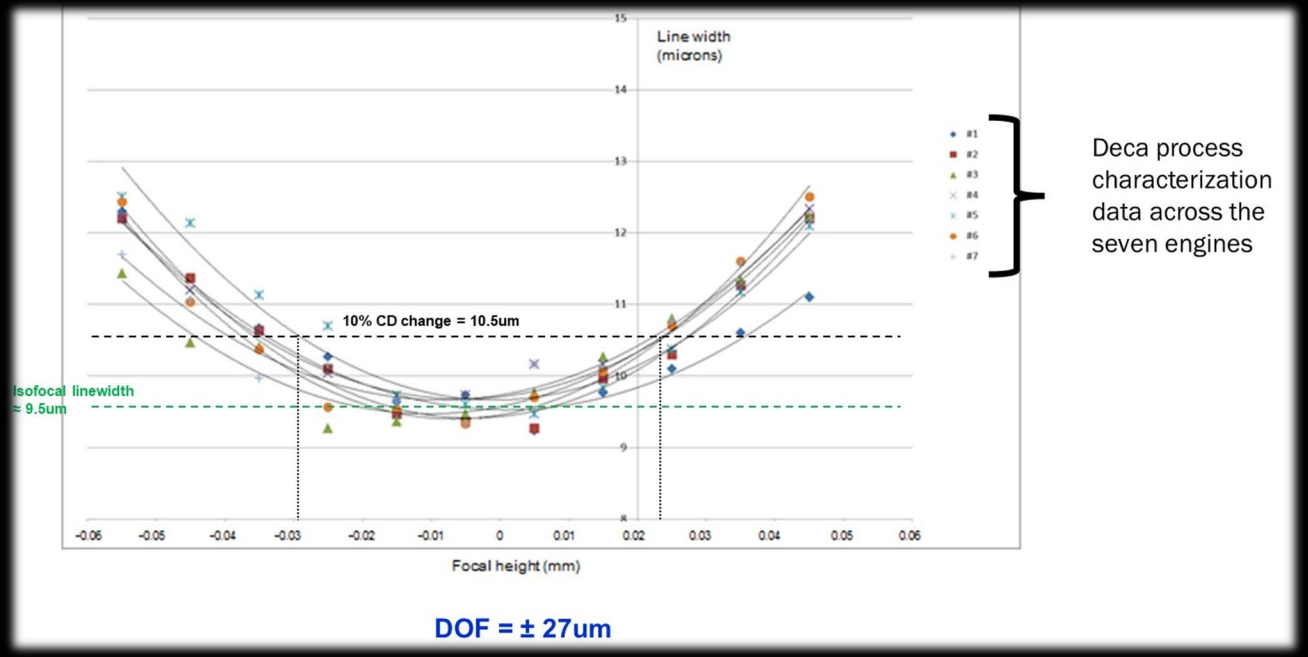


https://www.anandtech.com/show/16036/2023-interposers-tsmc-hints-at-2000mm2-12x-hbm-in-one-package

There is no photo mask with LDI – 100% digital laser light exposure from GDS II file

LDI Provides Larger DOF for Scaling to Finer Features

- LDI offers a high DOF (Depth of Focus) due to its inherent low NA
- Higher DOF becomes critical as linewidths are scaled over the imperfect planarity of organic FOWLP
- Example below is a plot for 10µm RDL lines & spaces across seven engines or heads of the Gen 1 LDI tool
- DOF > +/- 20µm for both RDL and Via



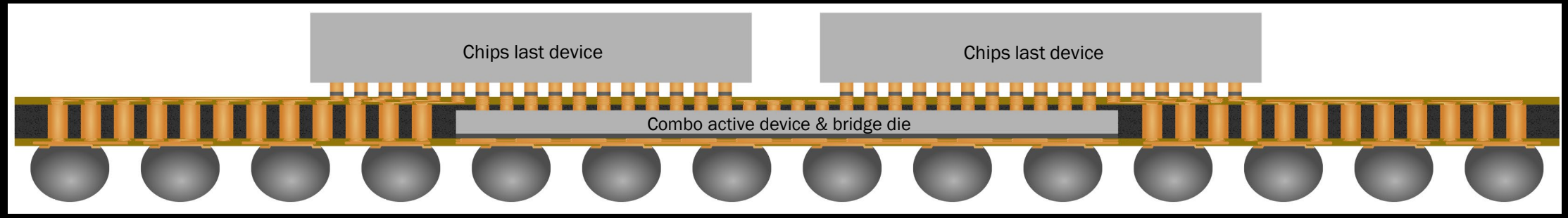
10 µm Lines & Spaces

Focus	Via Formation	With Measurement	Taper Width
Plus 20			5.4um
Plus 10			5.2um
0			4.8um
Minus 10			5.2 um
Minus 20			5.4um

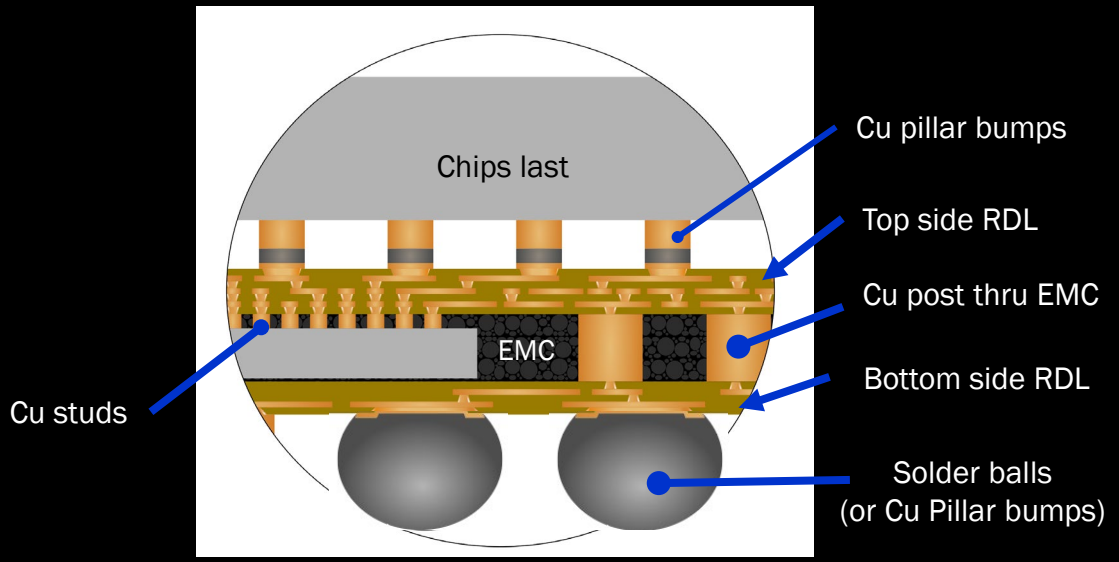
20 µm Via's

M-Series Embedded Active & Bridge Interposer

- Backside & Frontside RDL
- Embedded device & four Chips Last devices
- 150µm pitch Cu posts through EMC



M-Series™ Embedded Die Active Interposer

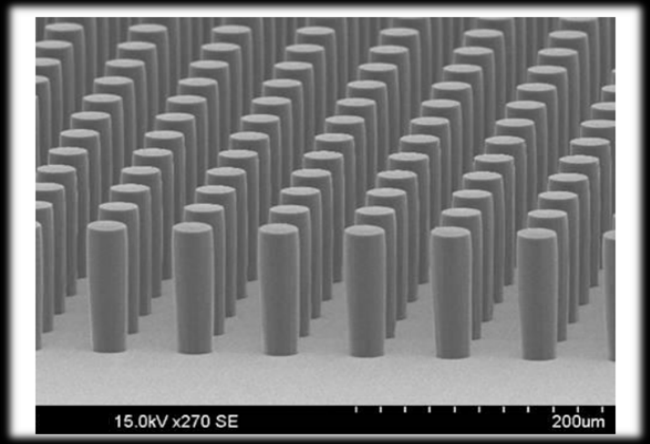


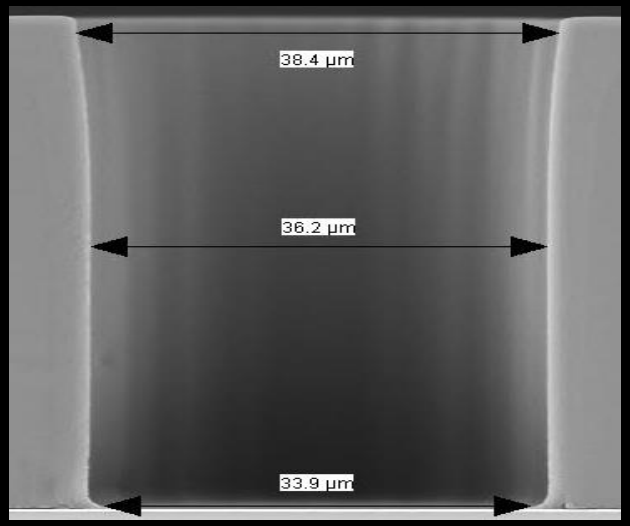
High Aspect Ratio Imaging

1. Cu Studs, 2:1
   25µm CD in 50µm film thickness
2. Cu pillar for bump, 2:1
   60µm CD in 120µm film thickness
3. Through Mold Vias, 4:1
   60µm CD in 240µm film thickness

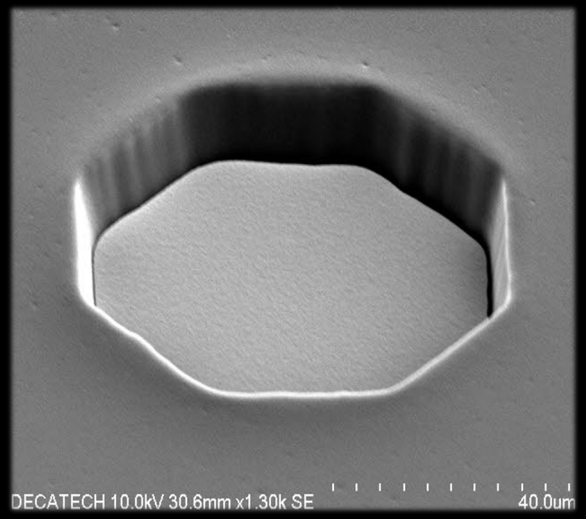
LDI Provides Larger DOF for High Aspect Ratio Dry Films

- Multiple dry film photoresists have shown 4:1 aspect ratio capability
- Ideal for high density Cu post interconnect on 3D fan-out structures
- Beyond 4:1, 30 µm CD demonstrated on a 168 µm dry film
- LDI provides high DOF for high aspect ratio features

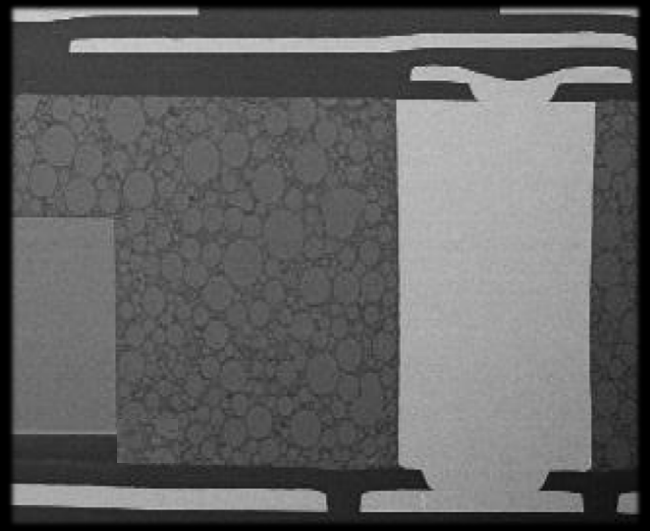




Cu Stud Photo



Cu Stud Post Plate



Cu Post

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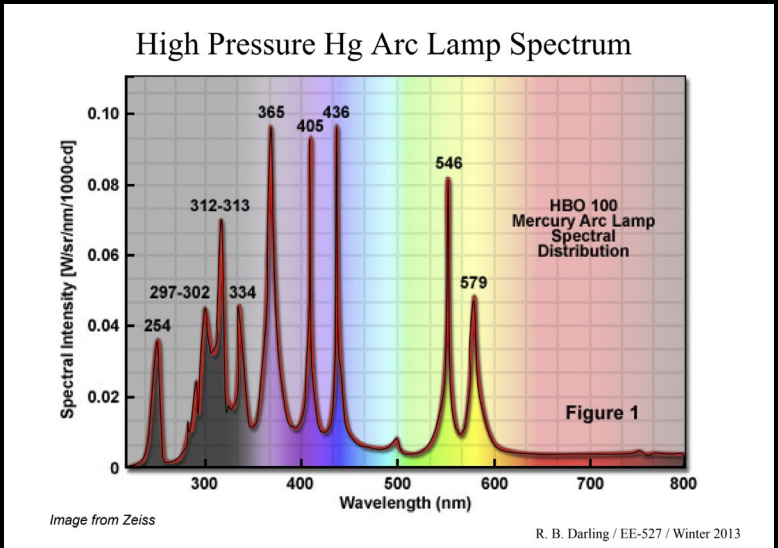
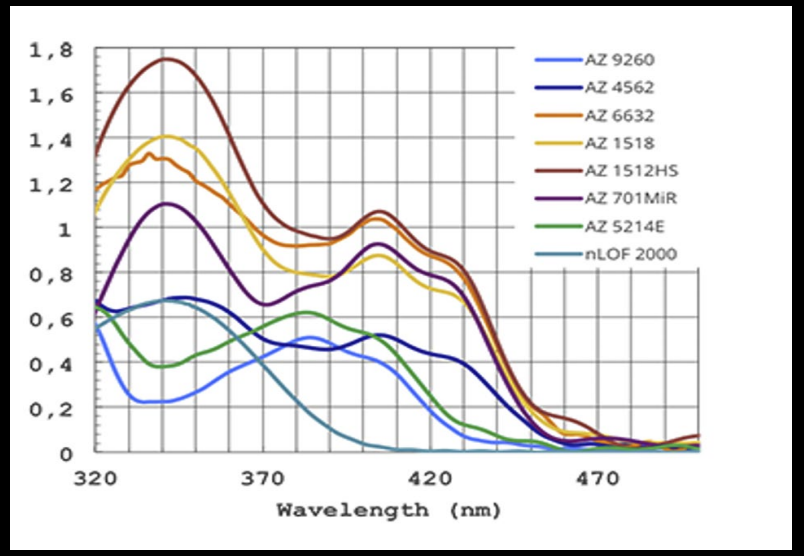
LDI Challenges – 405nm wavelength

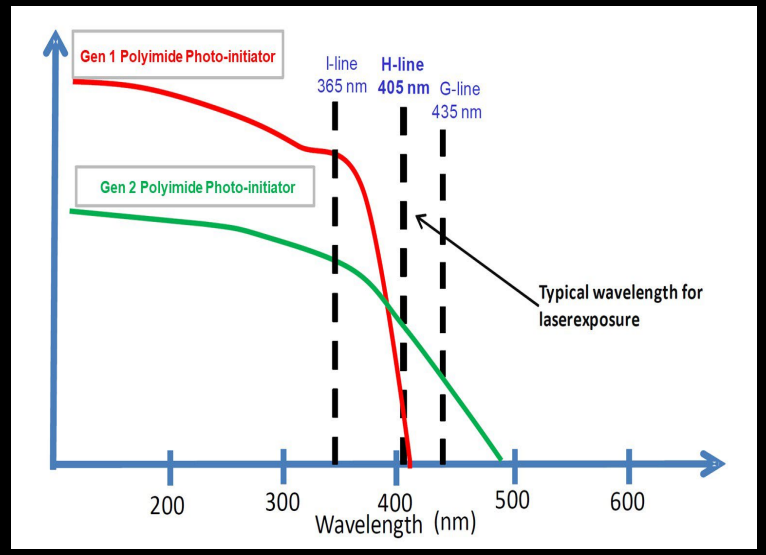
- One of the key challenge when using LDI photolithography was resist and dielectric selection given 405nm output spectra
- Conventional wafer level packaging photoresists and dielectrics have a wide variety of absorbance characteristics
- The most common resist have spectral sensitivity of g-, h-, and i-line ranging from 320 to 470 nm
- The photo-speed is determined by the absorbance efficiency at the wavelength
- i-line resists generally show a negligible sensitivity beyond 400 nm (example AZ nLOF 2000)
- Lower right is a photosensitive wavelength range of the dielectric in production, modified photo-initiator for sensitivity to 405 nm
- PCB industry have a long history of using 405 nm LDI with Dry Film resist



Hg Arc lamp with a wide intensity spectrum

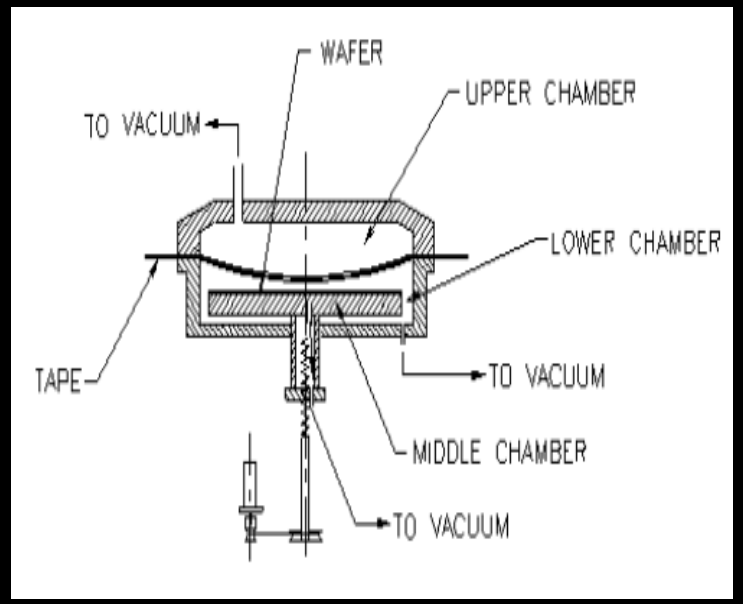


https://www.lithoprotect.com/en/worth-knowing/

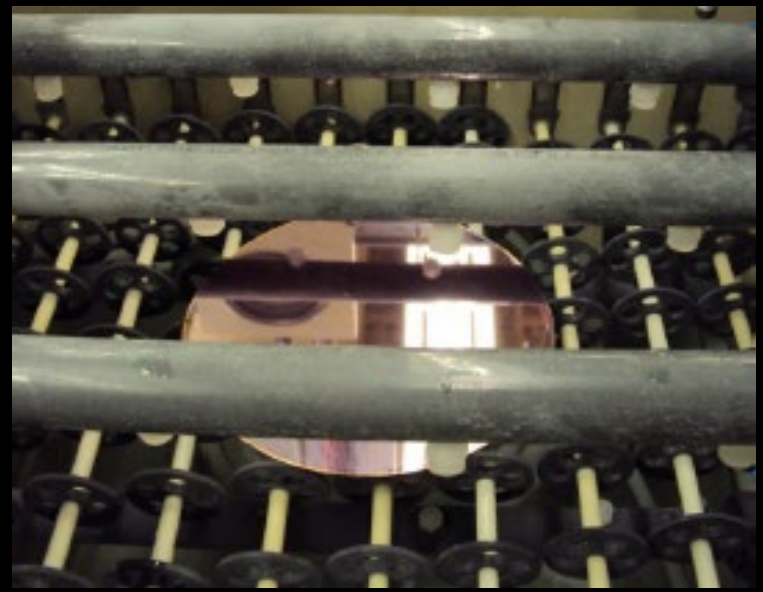


LDI Challenges - Dry Film Application

- Lamination process for dry film resists require robust equipment design and process control to ensure consistent 100% yield free of entrapped air
- Advanced dry films utilize a vacuum method vs. historic roller lamination eliminating potential concern for sensitive device structures
- Conveyor develop is typically utilized for dry film photo resist

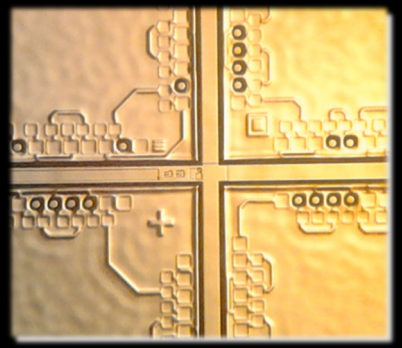


The vacuum below the film is slightly greater than above the film

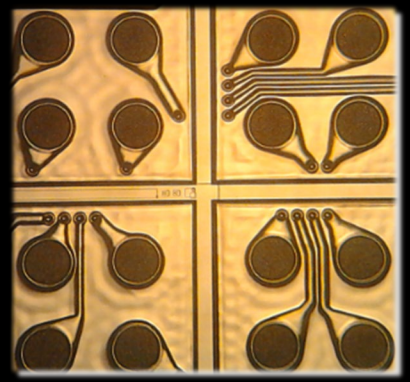


Nozzles continuously sprays solution while the wafer is driven by moving rollers

Lamination after seed at RDL



Lamination after seed at UBM



LDI Challenges – Dry Film vs. Liquid Photo resist

- Alkaline solutions are used as developers which are environmentally friendly vs. typical solvents for liquid resists
- Material waste is cut by > 90% with virtually the entire resist area utilized for large panel processing (600mm x 600mm is SEMI standard introduced by Deca & ASE)
- Comparatively, spin coating results in < 10% of the material being utilized with > 90% wasted in coater drain
- Other advantages of dry film include good conformal characteristics, excellent adhesion on any substrate, high speed LDI photo processing (>100 wph), simple material handling, high aspect ratio vertical profiles and cost

Attribute	Dry Film	Liquid Resist	
		Positve Resist	Negative Resist
Material Cost			
Throughput			
Exposure Cost			
Waste			
Solvent Cost			
Thickness Availability			
Thickness Uniformity			
Application and Develop Cost			
Resolution			
Process Latitude			
Photospeed			
Mask Cost		-	-
Post Exposure Processing			
Electroplating			
Stripping			

Although equipment & processes for dry film are different, there are several inherent advantages

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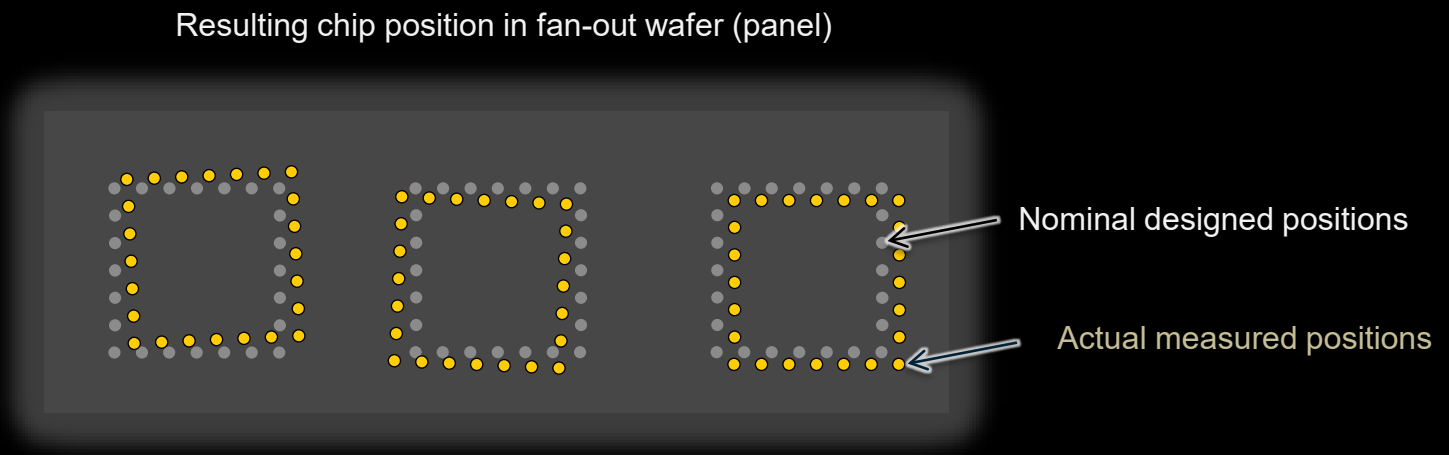
Background – Explaining Die Shift

The #1 Challenge in Fan-Out . Die Shift !

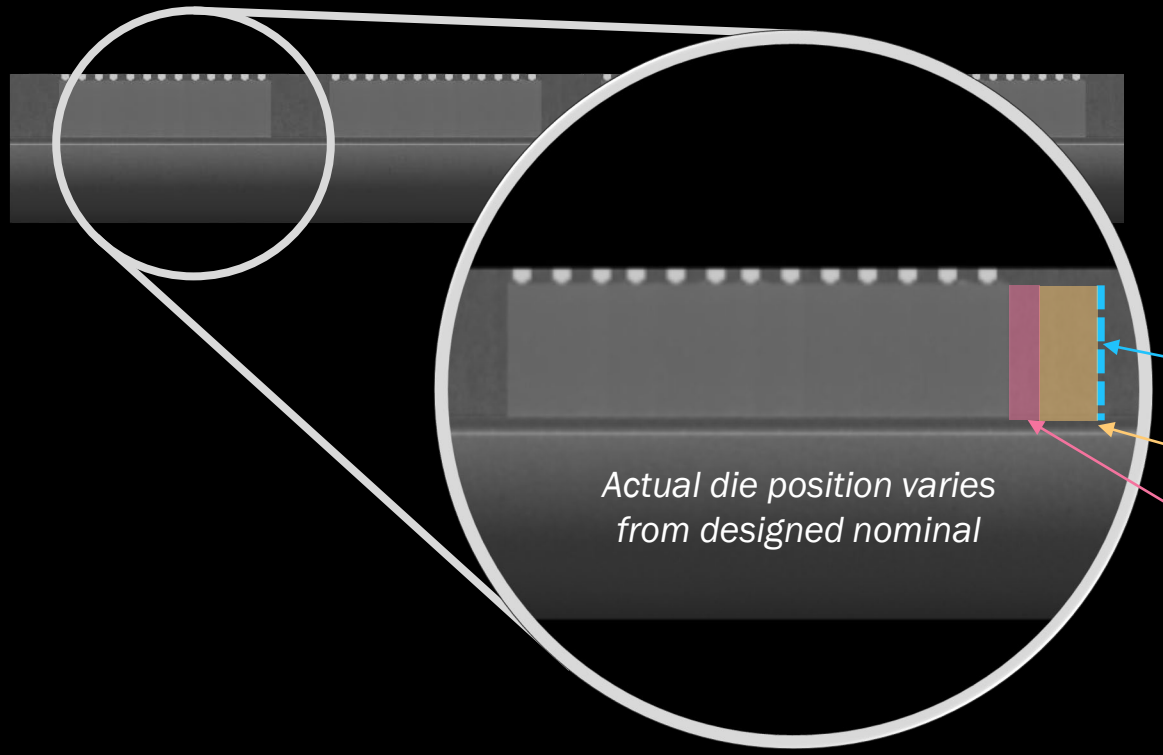
- Precision of monolithic silicon is lost - semiconductor devices are singulated and recombined in plastic 300mm wafer or large panel
- Two major sources of positional variation

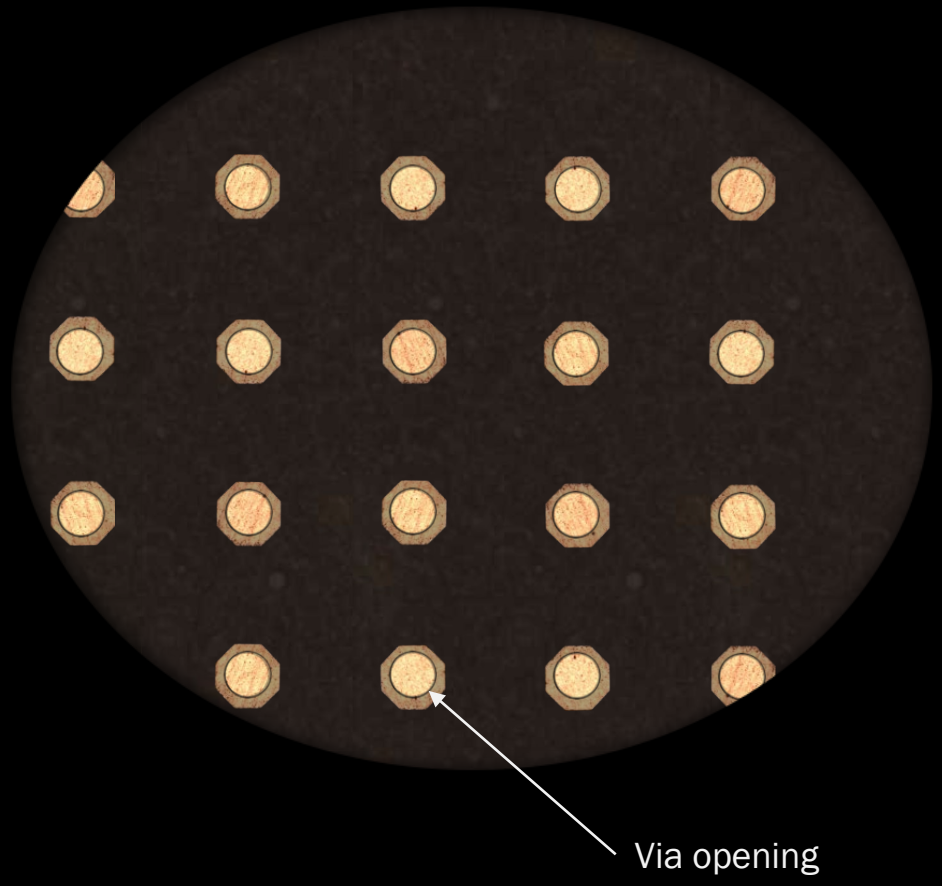


Background – Explaining Die Shift

1. Natural variation in mechanical placement of die

2. Displacement during encapsulation (molding)





Background Continued

- Chips first fan-out using conventional glass mask-based stepper lithography employs several techniques to mitigate die shift

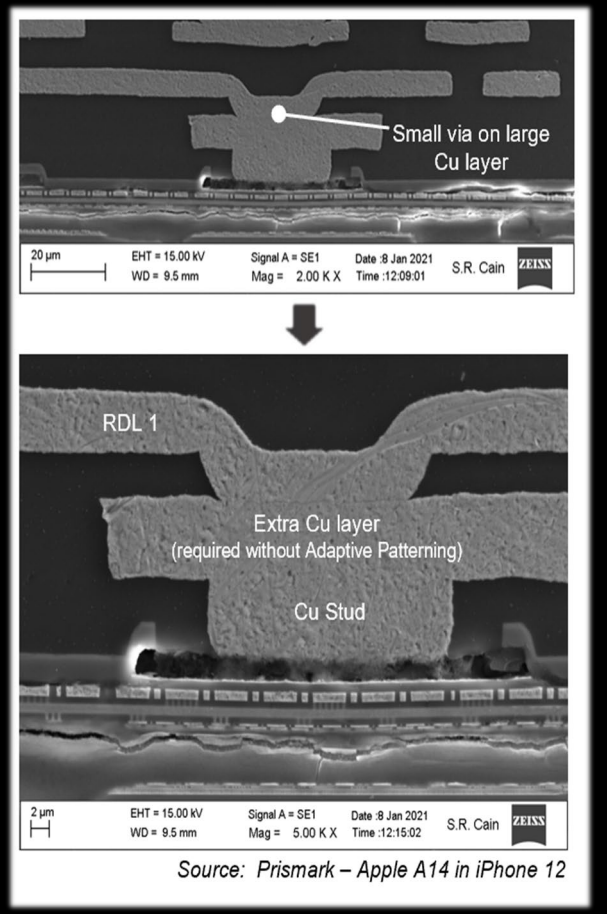
    1. Oversized capture pads – to create sufficient landing pad for remaining die shift

    2. Under sizing vias relative to device bond pad

    3. Chip attach compensation – using as-built measurements to optimize die attach coordinates to compensate for mold cure shrinkage

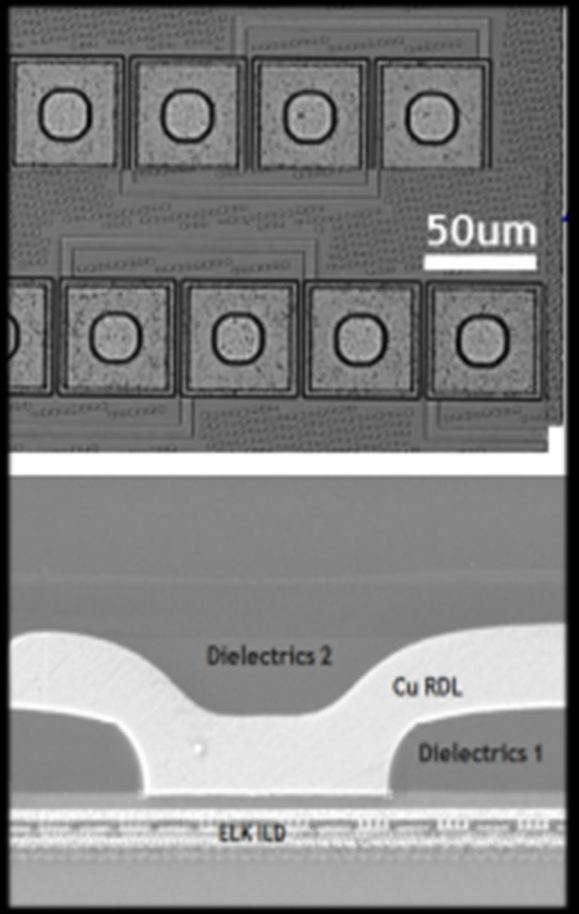
- Scaling to fine bond pad runs out of steam in the 40 to 45µm range

TSMC InFo



Source: Prismark – Apple A14 in iPhone 12

eWLB



http://meptec.org/Resources/June%208%20STATS%20ChipPAC.pdf

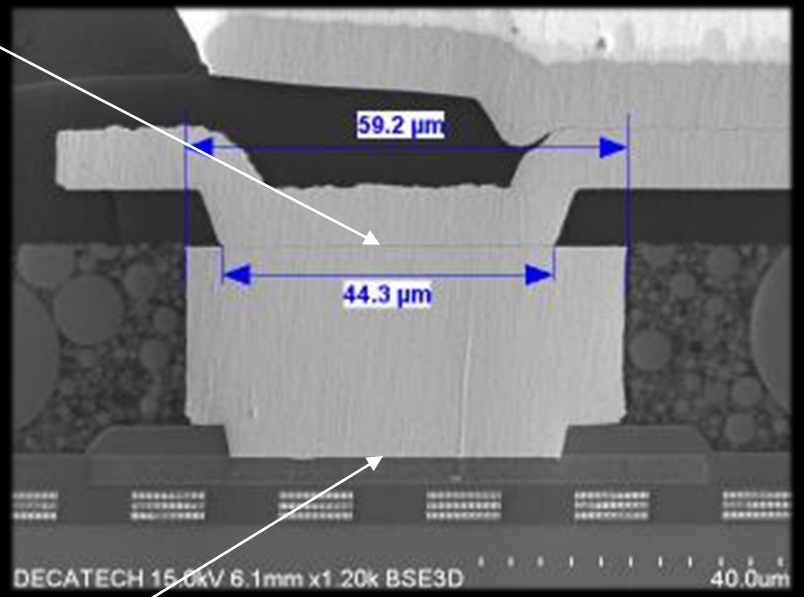
Conventional die shift mitigation techniques don't easily scale to higher density

Device Bond Pad Interface Examples

M-Series

(With Adaptive Patterning)

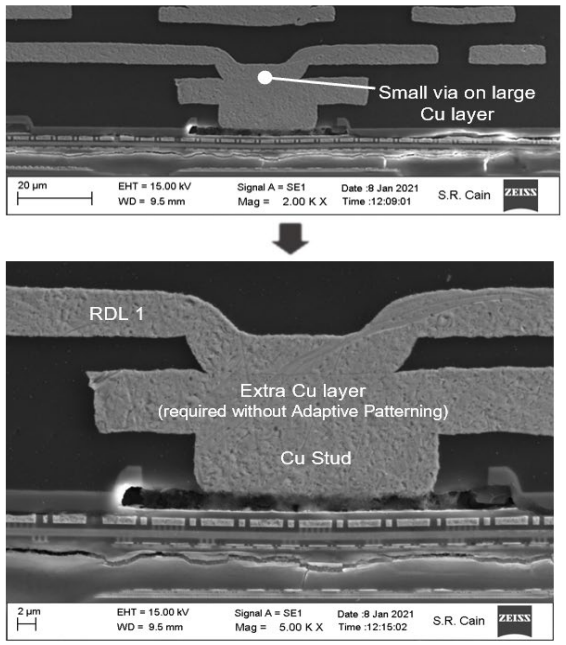
Large via for low RDS_{ON}



100% contact with device bond pad

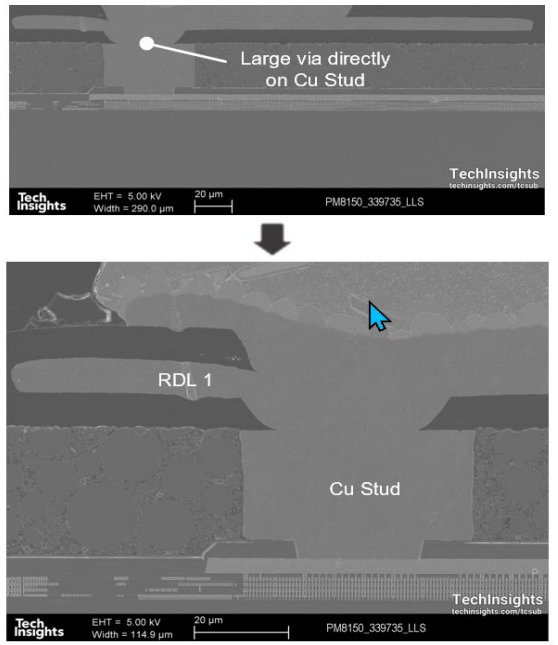
Patents issued & pending

TSMC InFO (in iPhone 12)

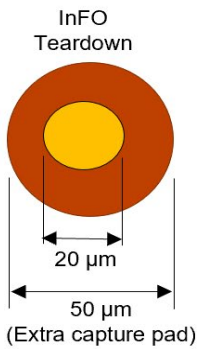


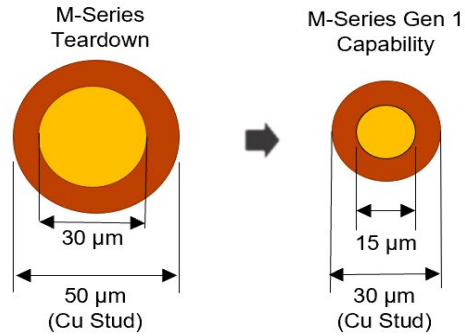
Source: Prismark – Apple A14 in iPhone 12

Deca M-Series (in Xiaomi)



Source: TechInsights – Qualcomm PM 8150 in Xiaomi Mi 9

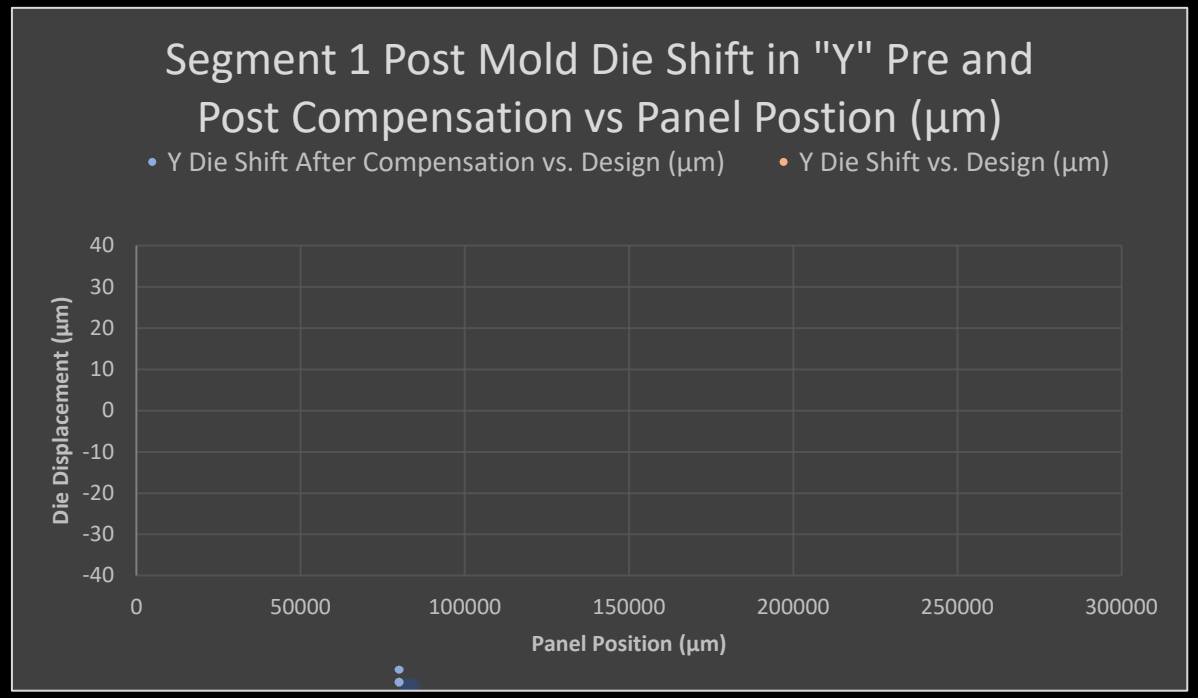




M-Series provides 100% contact with bond pad vs. < 33% with conventional fan-out (eWLB) with no extra Cu landing layer (InFo)

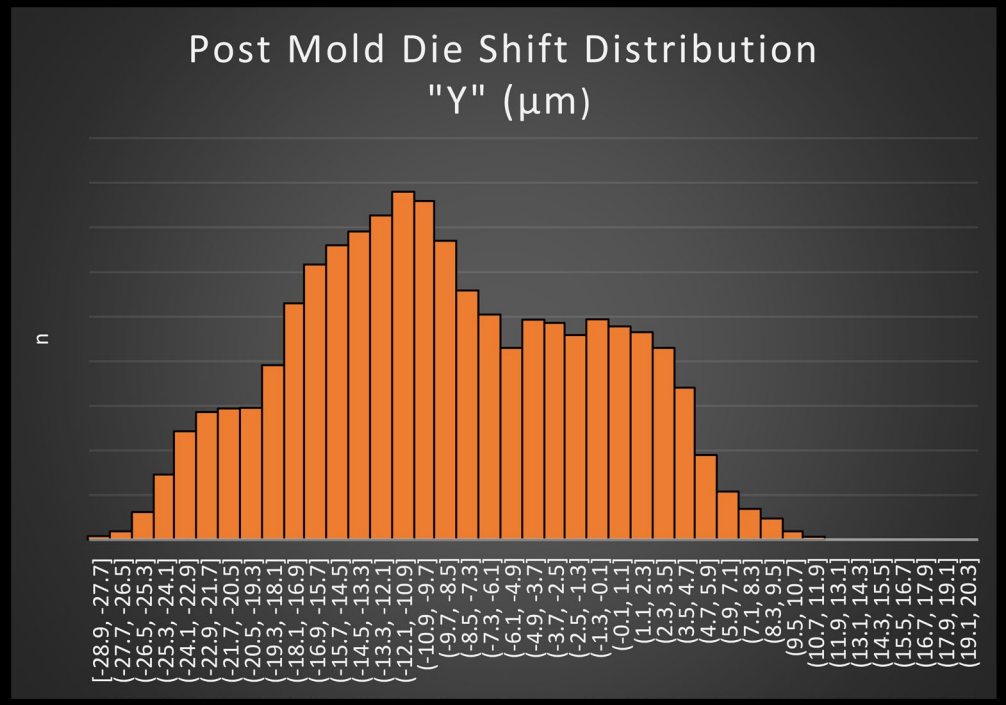
Die Attach Compensation Example – 600mm Panel

- Chip attach compensation – using as-built measurements to optimize die attach coordinates to compensate for mold cure shrinkage
- The slopes and intercepts were calculated for each segment (600mm panel) showing a correlation to panel position
- With this correlation to panel position, the die placements can be compensation using a simple linear fit
- Uncompensated data is shown in orange vs. the compensated data shown in blue

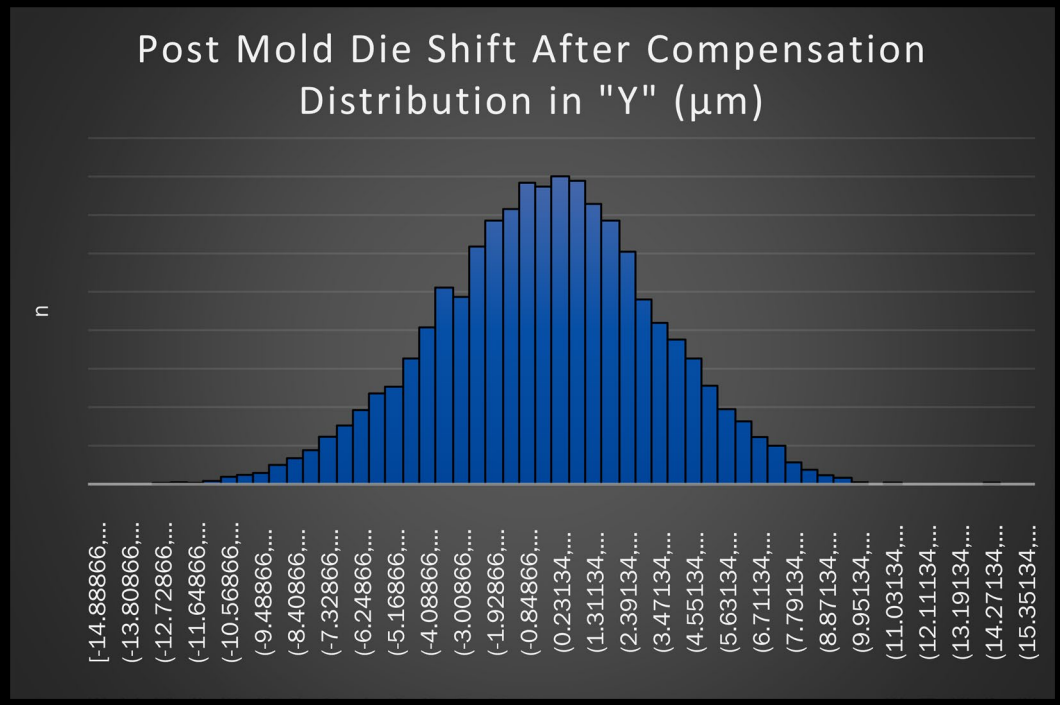


Die Attach Compensation Example – 600mm Panel

Initial “Y” Displacement (µm)



Compensated “Y” Displacement (µm)



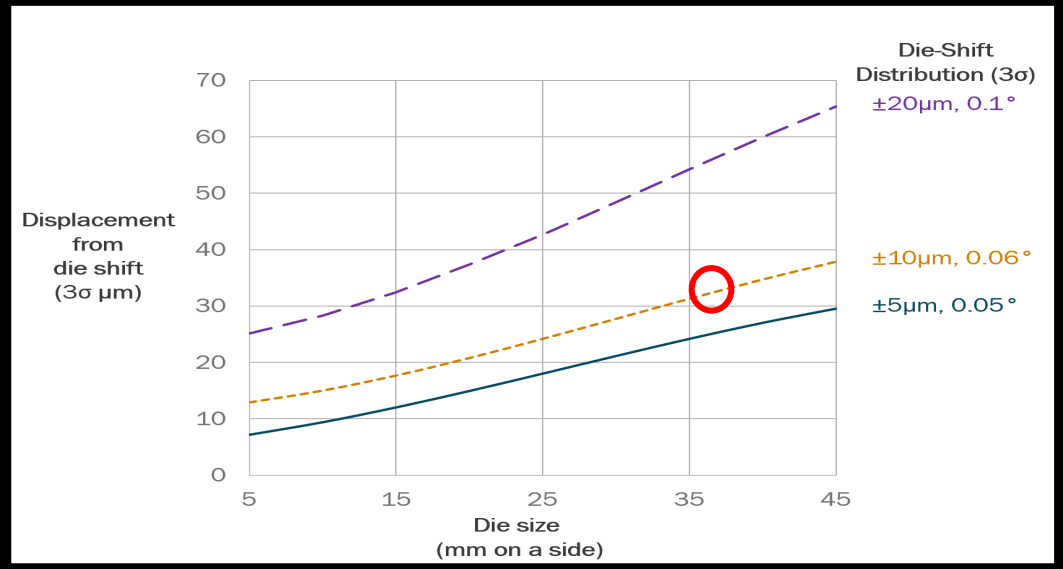
Before chip attach compensation range of -29µm to +10µm centered at -9 µm

After compensation range from -10µm to +10µm centered at 0 (with a normal distribution)

Chip attach compensation improves distribution, however, die shift distribution still significant

Die Shift remains a Significant Concern on Large Die

- With compensated data, we set the post mold die placement specification to +/-10 µm and rotation at 0.06 degrees 3σ for this single die package
- This represents a tuned system (best case manufacturing process for this small package, ~5 mm)
- Impact of package size due to rotation: yellow line represents die displacement vs. package size
- For example, with a 36 mm body size package, we can expect up to a 32 µm die displacement (red circle) with this optimized post mold die placement specification

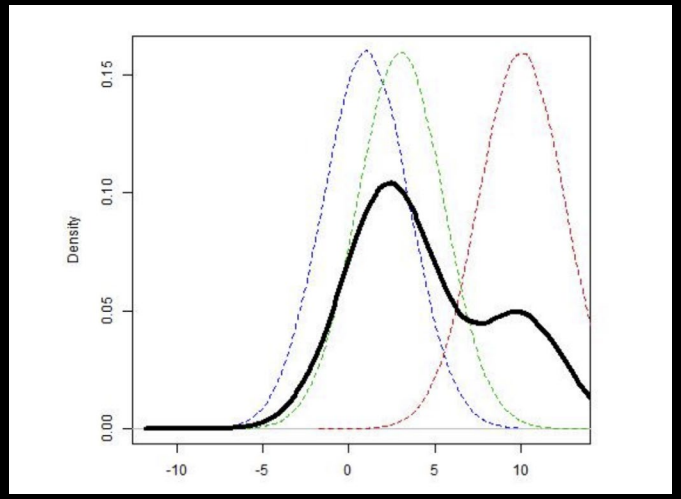


Conventional die shift mitigation techniques fall short on larger devices

Multi-Die Packages and Mixed Gaussian Distributions

- In a multi-die package or chiplet, if we treat each die independently, we can predict the die displacement distribution (based on actual data)
- These multi-die standard deviations can be found buy taking the square root of the combined variances
- Example, a chiplet device consisting of three die will potentially have a 3σ 15 µm post mold displacement (red box)

Multi-Die Sigma(σ) Summary (µm)						
	σ_x	σ_y	σ_R	$3\sigma_x$	$3\sigma_y$	$3\sigma_R$
One Die Package	2.87	3.53	0.04	8.61	10.58	0.13
Two Die Package	4.06	4.99	0.06	12.18	14.96	0.18
Three Die Package	4.97	6.11	0.07	14.92	18.32	0.22
Four Die Package	5.74	7.05	0.08	17.23	21.15	0.25

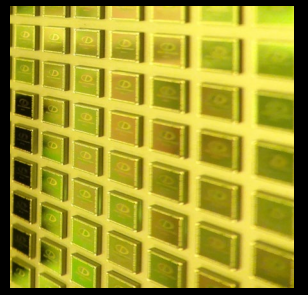


Chiplet integration in multi-die structures very difficult with conventional fan-out techniques

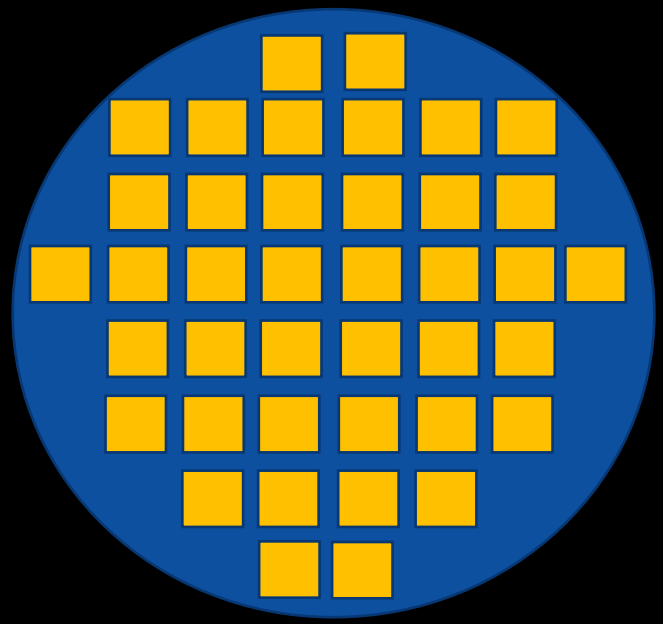
Outline

- Mask-Less Laser Direct Imaging (LDI) Lithography
- LDI Advantages
- LDI Challenges
- Background on Die Shift
- Adaptive Patterning
- Gen 2 RDL and Via Imaging
- Conclusion

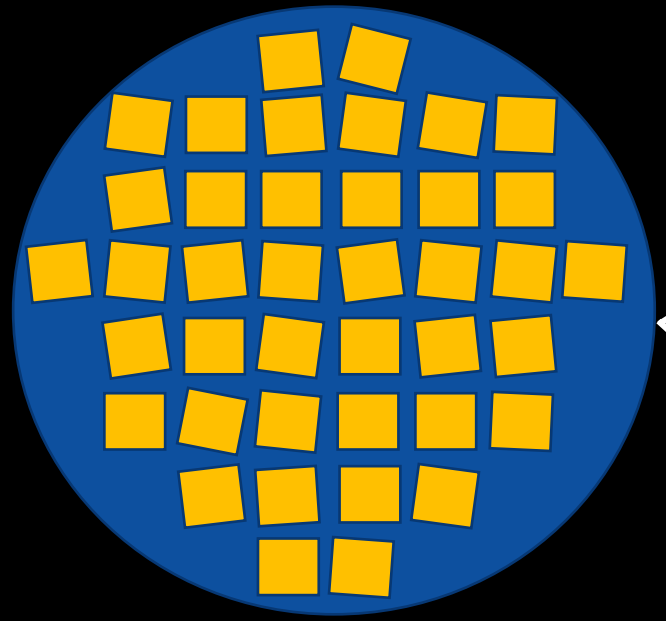
Adaptive Patterning Motivation



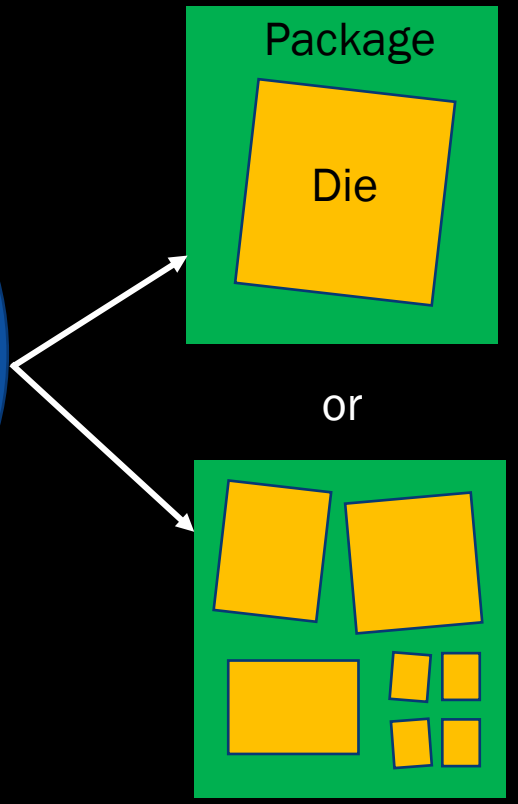
- In a stepper, each chip position is aligned and then exposed
- Die by die alignment decreases through-put and multi-die packages are difficult to manage
- Some systems use area alignment, sacrificing accuracy



Designed die locations
on reconstituted wafer



Actual die locations after
die attach and mold



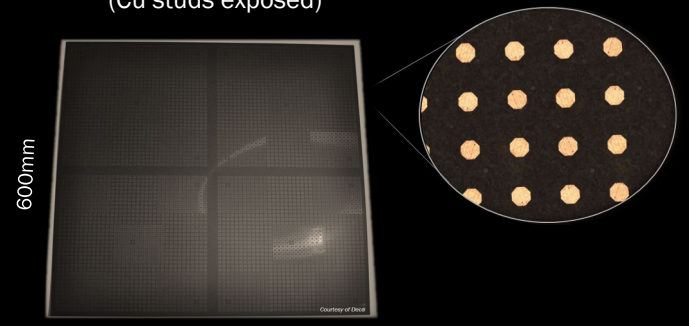
Stepper = each package
is an exposure aligned
to the die offset

Multi-die or chiplets
become difficult to manage

Adaptive Patterning – High level process overview

1. Measure actual die positions using high-speed optical scanner

Planarized molded panel
(Cu studs exposed)



High speed precision optical scanner

100% die measurement results

-112480	4.452	-75300	11.505	-0.07094
-112480	10.433	-60240	-5.664	0.07657
-112480	33.628	-45180	56.964	0.22095
-112480	17.823	-30120	-4.514	-0.06077
-112480	-0.121	-15060	7.748	0.14871
-112480	9.098	0	-2.332	0.15948
-112480	1.766	15060	1.994	0.04271
-112480	7.599	30120	9.588	0.05149
-112480	-2.226	45180	24.771	-0.01267
-112480	-1.291	60240	-13.819	0.04688
-112480	5.439	75300	-0.659	0.13094
-98420	0.127	-90360	7.939	-0.03352
-98420	3.053	-60240	-4.68	-0.01368

2. Generate unique lithography patterns for dielectric & photoresist layers during manufacturing (every device, every panel)

Actual die position
measurements

-112480	4.452	-75300	11.505	-0.07094
-112480	10.433	-60240	-5.664	0.07657
-112480	33.628	-45180	56.964	0.22095
-112480	17.823	-30120	-4.514	-0.06077
-112480	-0.121	-15060	7.748	0.14871
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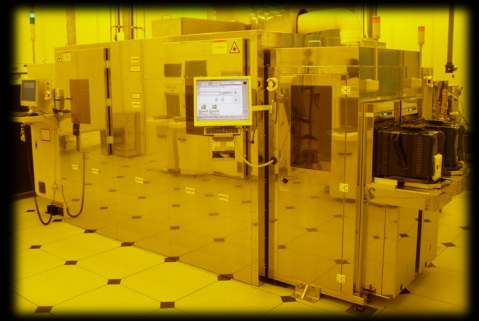
Real-time
Design-during-manufacturing

ENGINE

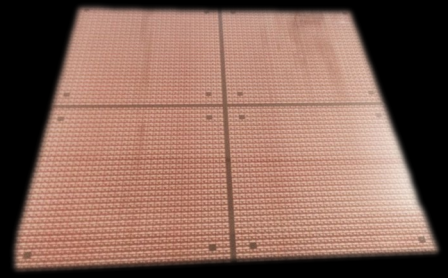
Lithography pattern for the whole panel is dynamically generated

Mask-less LDI lithography system



High throughput scan

Unique lithography
pattern per panel

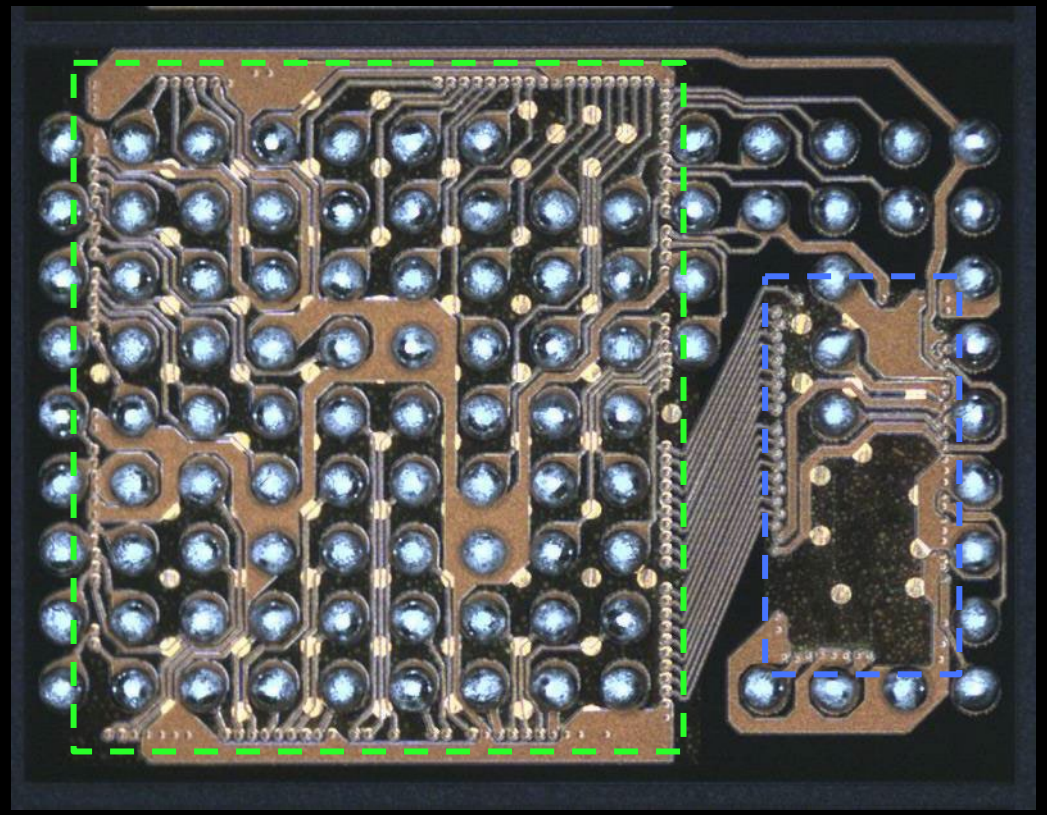


Unique optimized GDSII file for every panel
(no reticle size limitations)

Multi-mode Adaptive Patterning

IoT Module – 2 chips

- High performance MCU – 40nm
- Bluetooth radio – 55nm



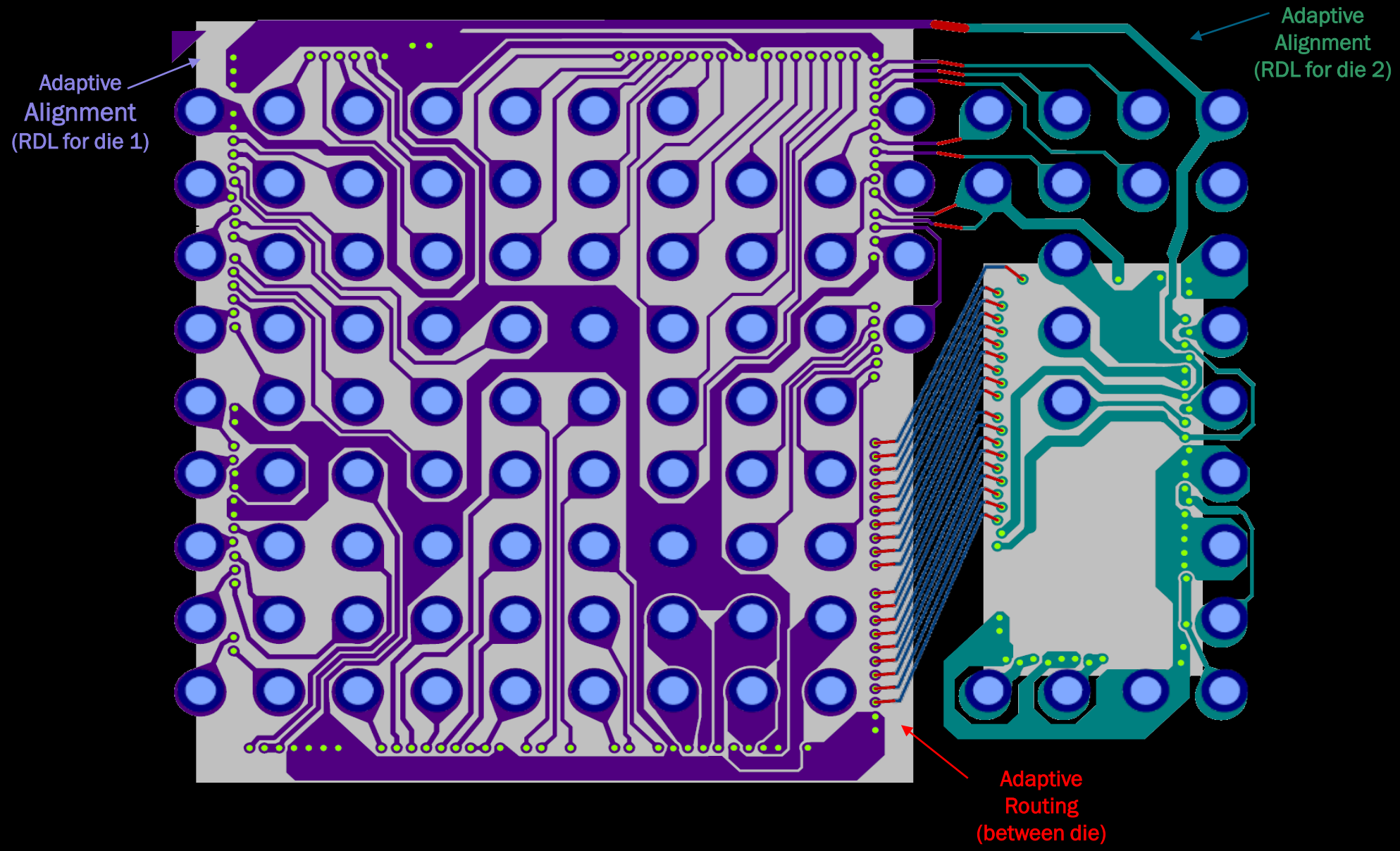
Package 5.0 x 3.8 mm

104 IO, 0.4mm pitch

Die 1: 3.7 x 3.2 mm

Die 2: 1.0 x 2.0 mm

Multi-mode Adaptive Patterning



STUDIO + ENGINE + CONNECT

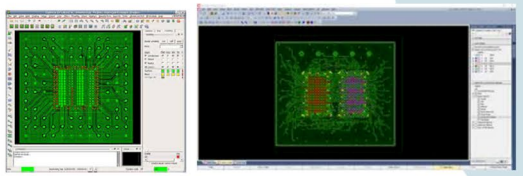
LIVE

by DECA

Electronic Design Automation Software

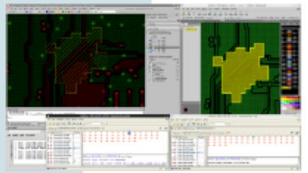
DESIGN KITS

LAYOUT EDA TOOLS (THIRD-PARTY)



STUDIO

VERIFICATION EDA TOOLS (THIRD-PARTY)



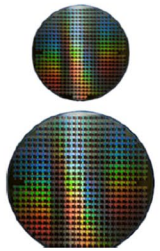
Production Software

ENGINE

Generates a unique design for each package in a wafer or panel with **Design-Thru-Manufacturing (DTM)**

CONNECT

Equipment

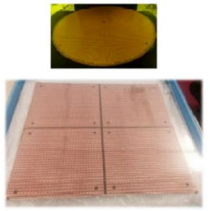


Pick and Place

Die Measurement

Lithography

Automated Optical Inspection



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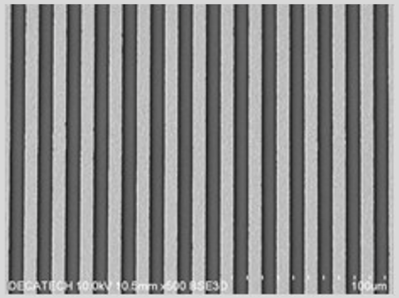
Deca's Scaling to Second Generation

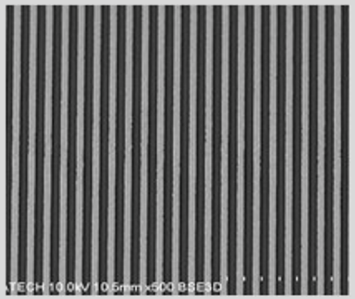
Existing Equipment Set

Gen 1
2018 →



Attribute	Units	Gen 1
RDL lines & spaces	µm	10
RDL layers	#	2
RDL line density	Lines / mm / layer	50
Minimum via*	µm	20
Enclosure	µm	7.5
Bond pad pitch	µm	55
Cu stud diameter	µm	35

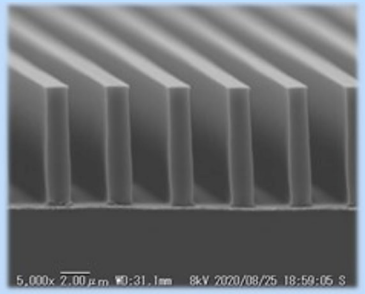
Gen 1.5
2021 →



Gen 1.5
5
3
100
10
7.5
45
30

Gen 2 Lithography & AOI

Gen 2
2022 →



Gen 2	Gen 2.1	Gen 2.2
2		
5		
250		
6		
3		
20		
12		

Gen 3 Litho & AOI

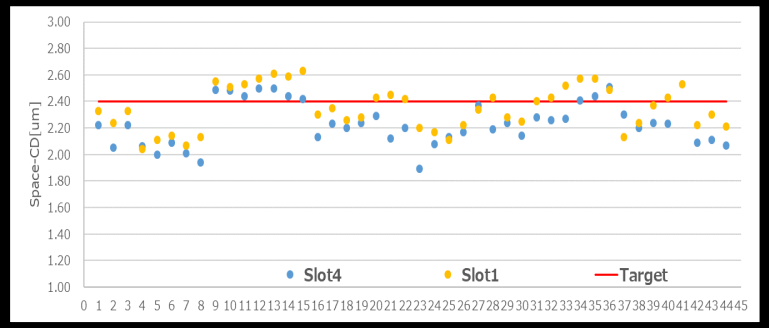
Gen 3
2026 →

**Note: Max via size = Cu stud diameter – 2 x Enclosure*

Delivering Gen 2 Capability with 2µm Line & Space

405nm results using ADTEC's DE-2 LDI equipment with integrated Adaptive Patterning

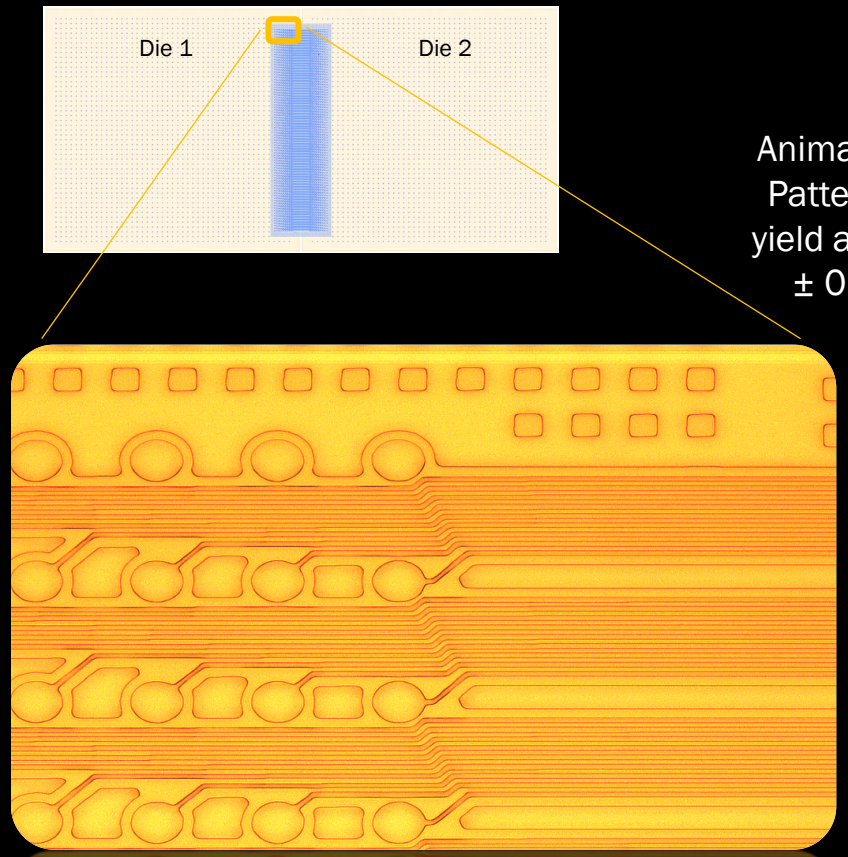
CD measurements @ 460mJ/cm^2



Line CD Measurements on the two wafers

	Ave	Max	Min	Range	σ
Slot1	2.35µm	2.63µm	2.04µm	0.59µm	0.16µm
Slot4	2.23µm	2.51µm	1.89µm	0.62µm	0.16µm
Ave	**2.29µm**	**2.57µm**	**1.97µm**	**0.61µm**	**0.16µm**

RDL intentionally oversized for 2µm to account for Cu dimensional change during strip & etch



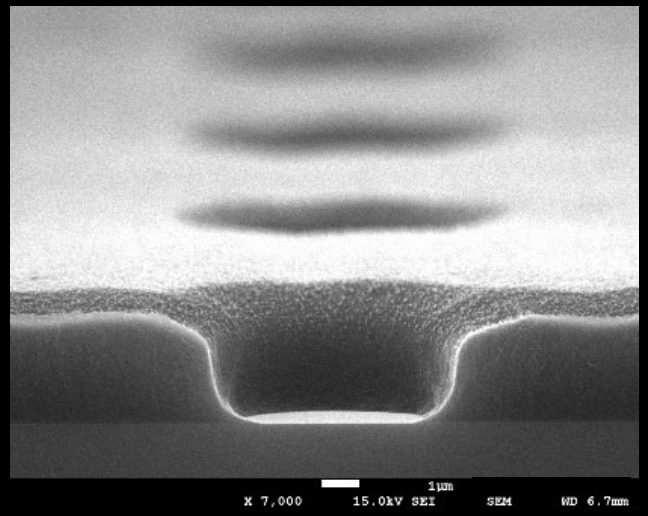
Animation showing Adaptive Patterning to enable 100% yield across ± 15µm X&Y and ± 0.1 deg theta die shift

Integrated Gen 2 Adaptive Patterning provides high yield on multi-chip devices

Delivering Gen 2 Capability with 6µm Polyimide Vias

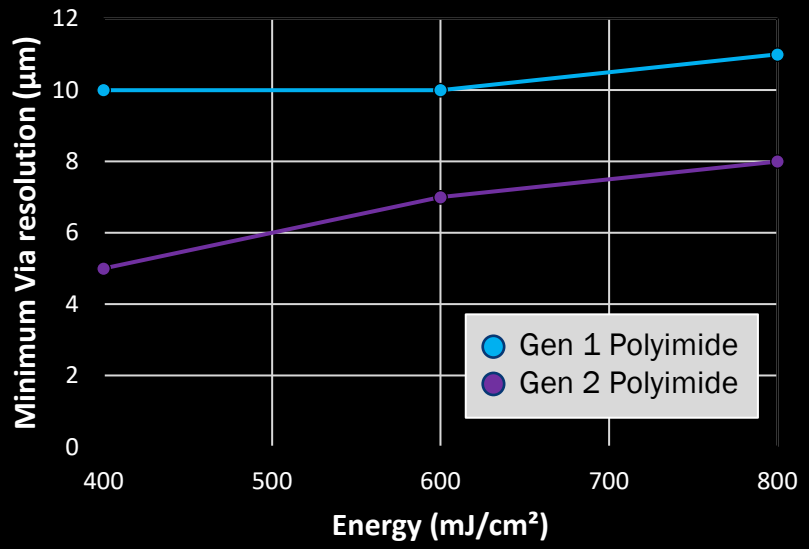
Results using ADTEC's DE-2 LDI equipment with integrated Adaptive Patterning

VIA profile of Gen 2 Polyimide
(400 mJ/cm^2 after develop & cure)



6µm Via using 405nm LDI

VIA resolution vs. exposure dose



Gen 2 polyimide was able to achieve Via CD of 6µm to support M-Series Gen 2 scaling

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Conclusion

- Laser Direct Imaging (LDI) has been in production on wafer level and fan-out packaging for over a decade
- Deca originally worked with Hitachi Via Mechanics to scale LDI to semiconductor requirements on 200mm & 300mm silicon wafers (in preparation for planned Adaptive Patterning implementation on M-Series fan-out)
- Currently LDI is deployed in high volume production on both 300 round and 600mm square panel formats at Deca's licensee partners on M-Series with Adaptive Patterning
- LDI has advantages of higher DOF, no photomasks, no reticle size limitations, large panel processing experience, and real time design optimization through Adaptive Patterning
- Multiple heterogeneous chiplet integration structures are currently in design and qualification utilizing LDI
- LDI technology coupled with Adaptive Patterning provides the industry with breakthrough scaling capability to 20 µm die pad pitch with Gen 2 in 2022

Acknowledgement Benedict San Jose of Deca

Thank you.

For more information contact:

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