

ADDRESSING CHALLENGES IN DUAL SIDED SIP THERMAL BUDGET

Zhang Hanwen
Global Product Manager, Advanced Packaging
Heraeus Electronics

01100



18TH INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
FOUNTAIN HILLS, AZ • WWW.DEVICEPACKAGING.ORG • MARCH 7-10, 2022

AGENDA

1

Introduction

- System In Package for 5G applications
- Thermal Budget Challenge In Dual-sided SiPs

2

Low Temperature Solder Material

- Tin-bismuth-silver (Sn-Bi-Ag) low temperature alloy properties
- Solder bump microstructure and Intermetallic phase development with thermal aging
- Thermal cycling and mechanical drop tests

3

Targeting Ultra-fine Pitch Application

- Paste formulation- powders and flux

4

Q & A

AGENDA

1

Introduction

- System In Package for 5G applications
- Thermal Budget Challenge In Dual-sided SiPs

3

Targeting Ultra-fine Pitch Application

- Paste formulation- powders and flux

2

Low Temperature Solder Material

- Tin-bismuth-silver (Sn-Bi-Ag) low temperature alloy properties
- Solder bump microstructure and Intermetallic phase development with thermal aging
- Thermal cycling and mechanical drop tests

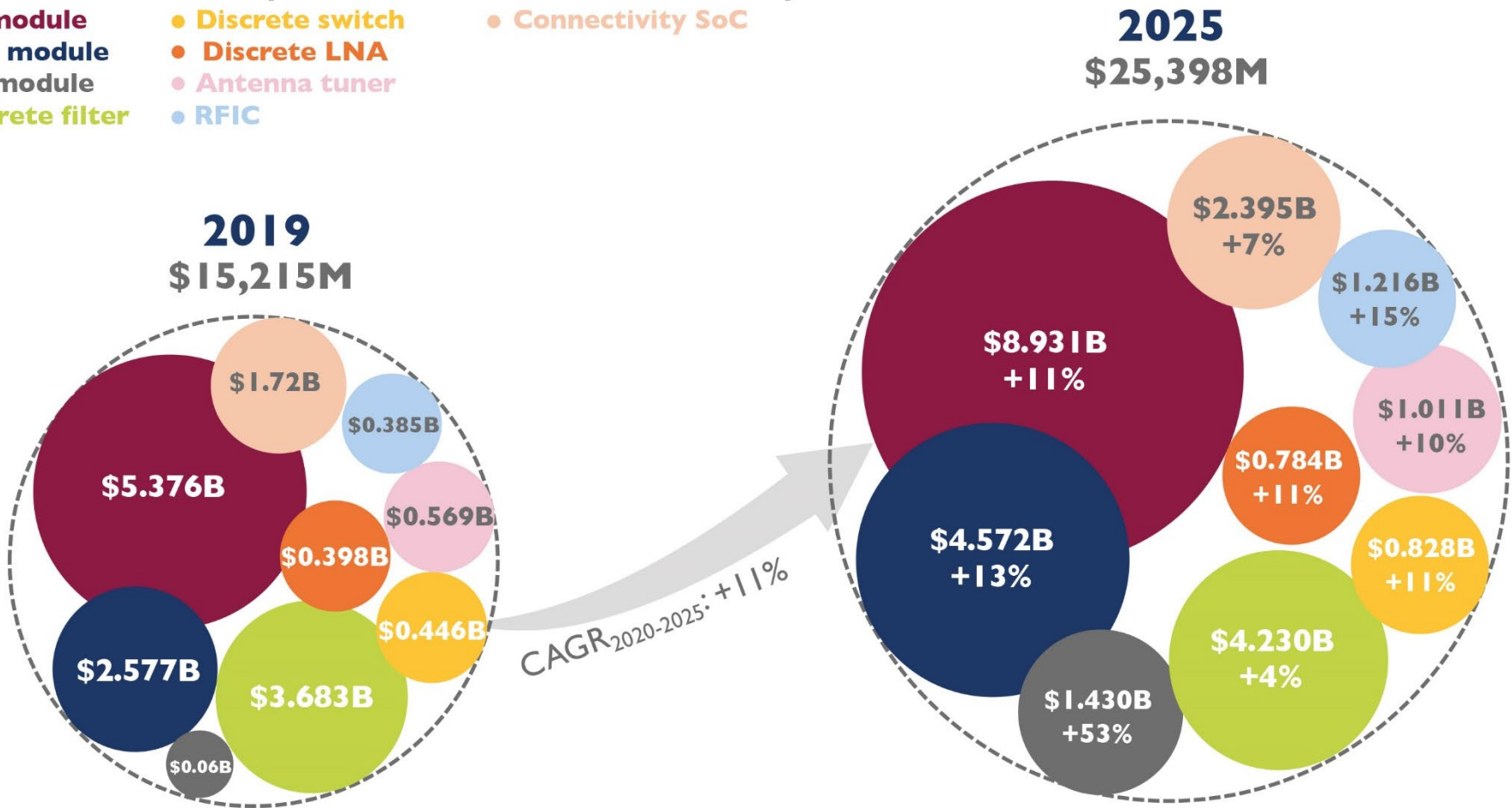
4

Q & A

RF FRONT-END MARKET OPPORTUNITIES

-- TAM Modules & RF components for front-end and connectivity

- PA module
- FEM module
- AiP module
- Discrete filter
- Discrete switch
- Discrete LNA
- Antenna tuner
- RFIC
- Connectivity SoC



Source: Yole Developpement Sept 2020

SYSTEM-IN-PACKAGE (SiP) MODULES FOR 5G APPLICATIONS

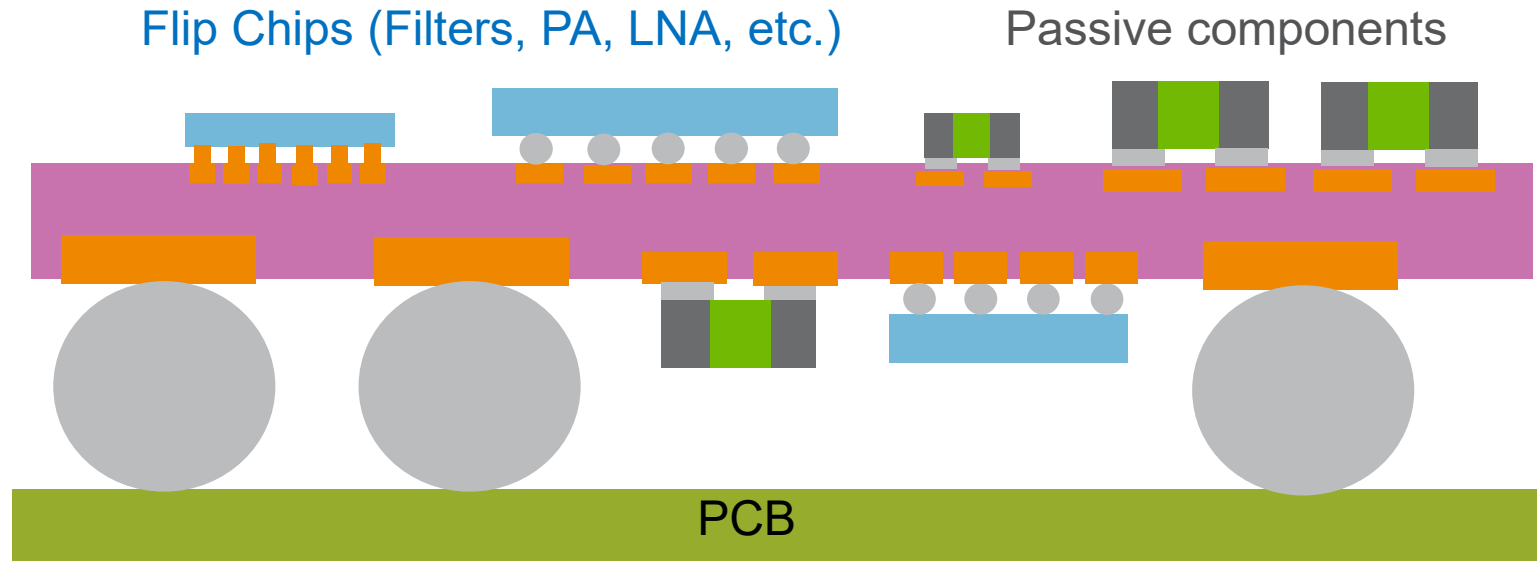
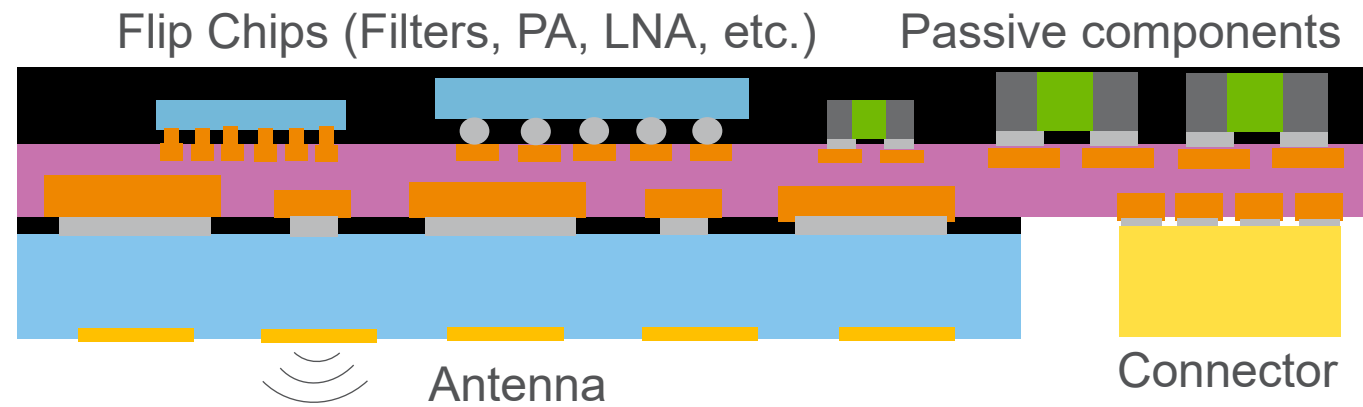


Illustration of RF Front-End SiP module

- System-in-Package technologies' flexibility enables heterogenous integration for functional performance and faster time-to-market
- SiP modules consist of flip chips (filters, PA, LNA, etc.) and passive components of various sizes
- SiP can be dual sided and subjected to multiple reflows

THERMAL BUDGET CHALLENGE IN DUAL-SIDED SIPS

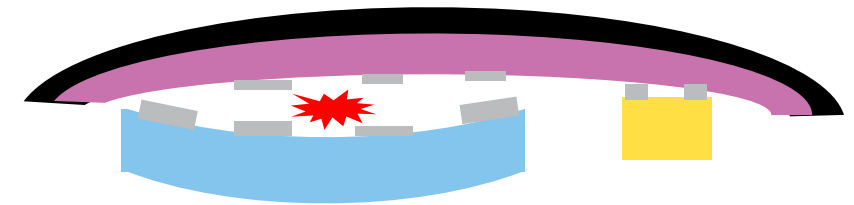
A Case study of dual sided Antenna-in-package (AiP)



1st reflow (260°C for SAC305) and underfill/molding



2nd reflow (260°C for SAC305)



Lower the thermal budget during 2nd reflow by using a low temperature solder material

AGENDA

1

Introduction

- System In Package for 5G applications
- Thermal Budget Challenge In Dual-sided SiPs

2

Low Temperature Solder Material

- Tin-bismuth-silver (Sn-Bi-Ag) low temperature alloy properties
- Solder bump microstructure and Intermetallic phase development with thermal aging
- Thermal cycling and mechanical drop tests

3

Targeting Ultra-fine Pitch Application

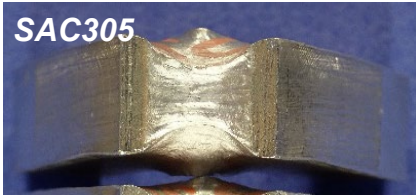
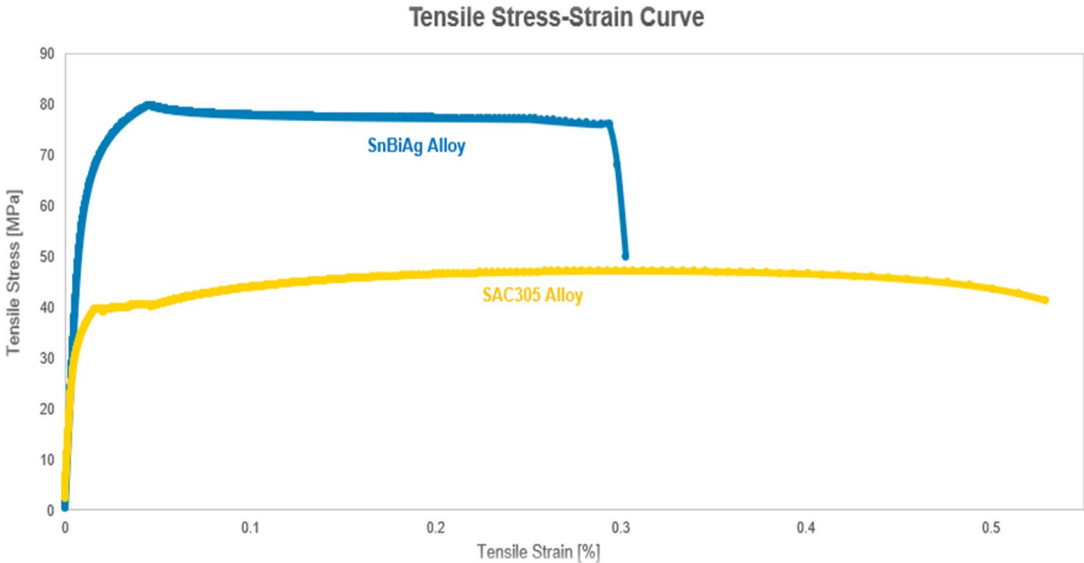
- Paste formulation- powders and flux

4

Q & A

SOLDER ALLOY PROPERTIES

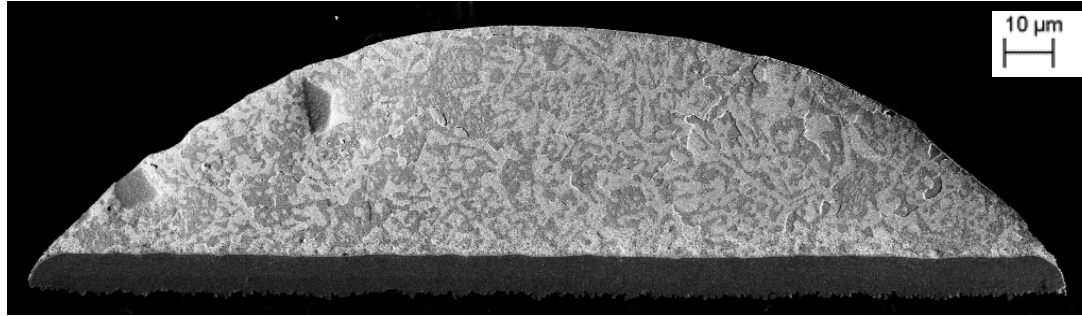
Solder Type	Melting Point, °C	Electrical Resistivity, $\mu\Omega\cdot\text{cm}$ ASTM F84	Young's Modulus, GPa ASTM C597	0.2% Proof Stress, N/mm ²	Tensile Strength, N/mm ²	Elongation, % ASTM A370-17	Impact Energy, J ASTM E23
SAC305	223	10.9	45.6	35.8	46.6	44.6	69
Sn-Bi57-Ag1	138	34.8	41.5	63.0	78.0	22.8	0.88
Sn-Bi48-Ag _x	145	29.0	42.2	60.6	80.6	24.0	0.84



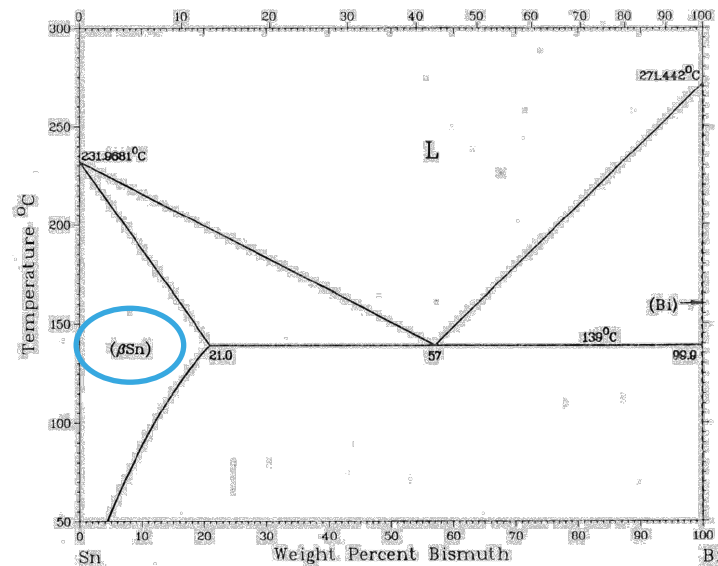
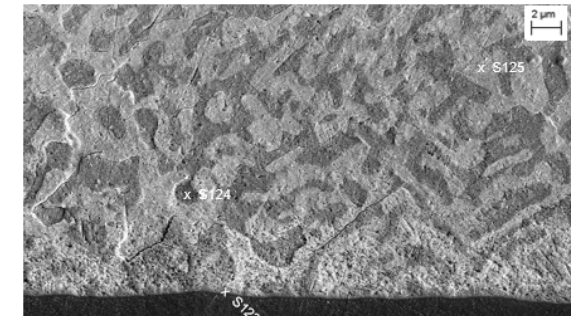
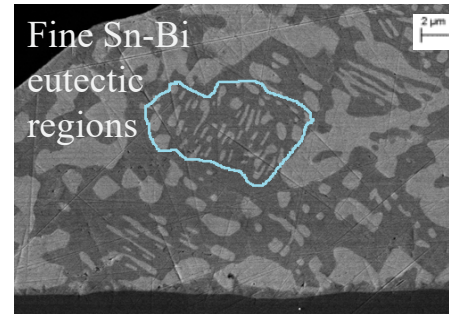
Bi-Sn alloys are known to be more brittle than SAC305

SN-57BI-1AG SOLDER BUMP MICROSTRUCTURE

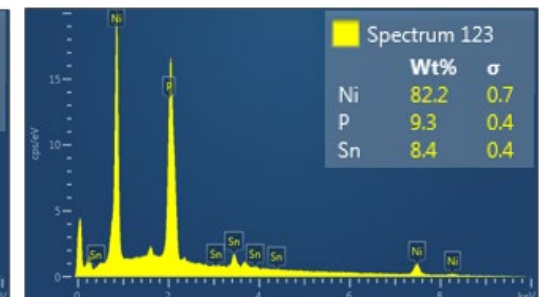
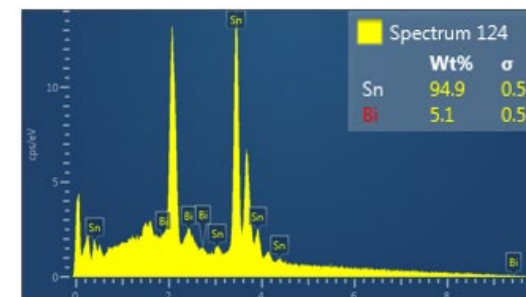
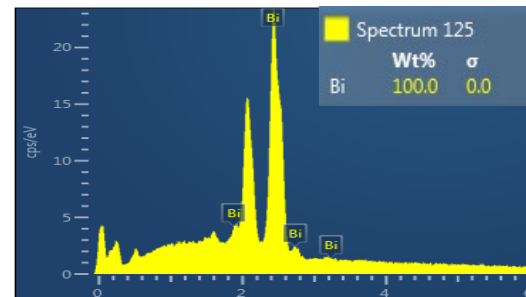
Solder bumps are formed with a Type 6 printing solder paste in a no clean chemistry



Sn-Bi57-Ag1 solder bump printed on ENIG plated surface (Au/Ni)

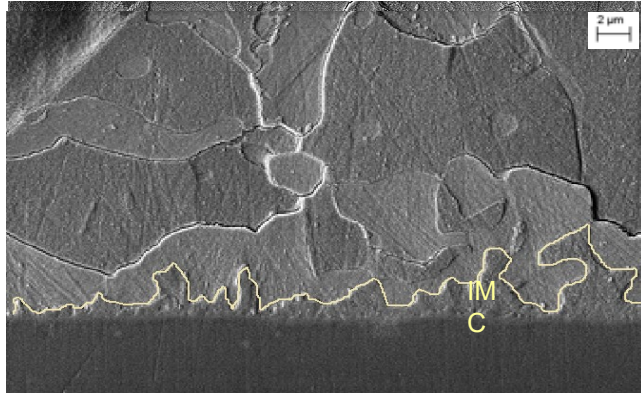


White (S125): pure bismuth phase, 100% Bi
 Grey (S124): primary tin phase (β Sn), Sn-5wt%Bi
 S123: Intermetallic compound (IMC) with ENIG substrate

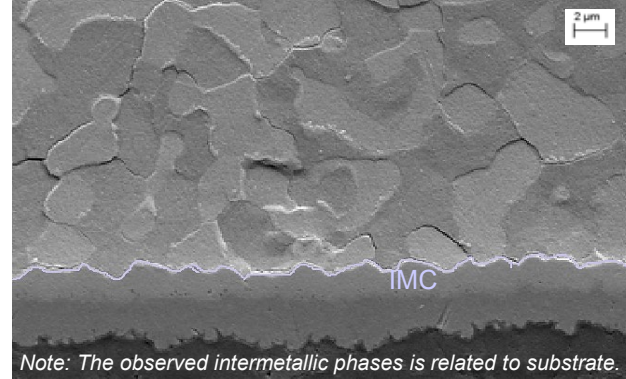


THERMAL AGING TEST AT 75°C- IMC GROWTH ON VARIOUS SUBSTRATES

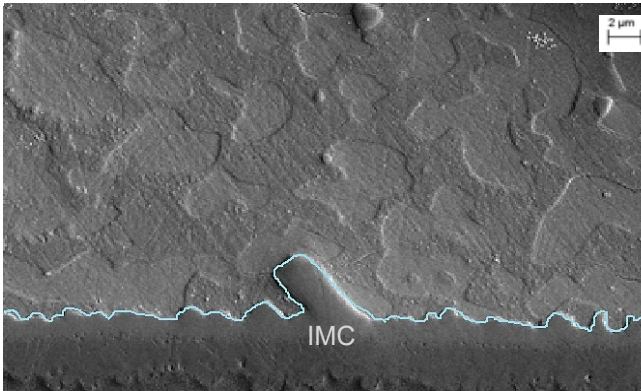
ENIG Plated Surface, 1000H



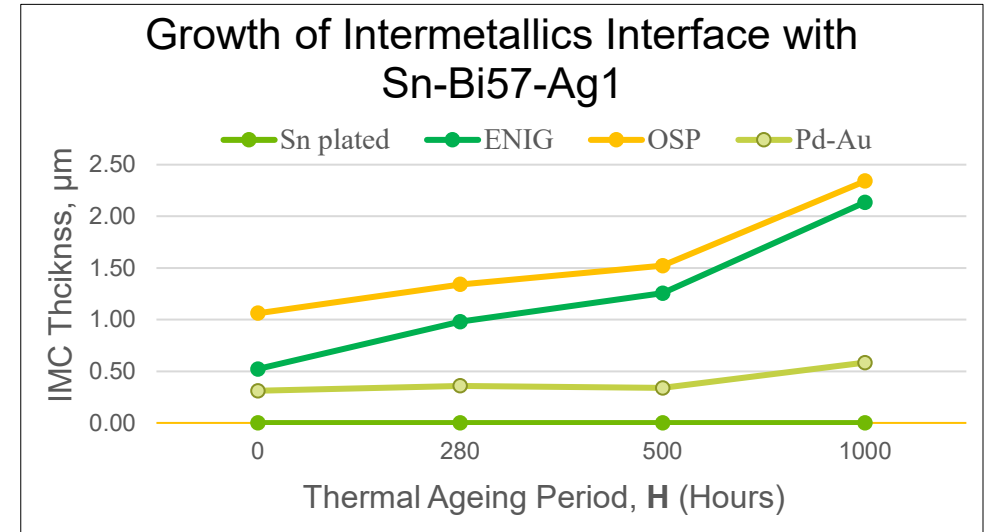
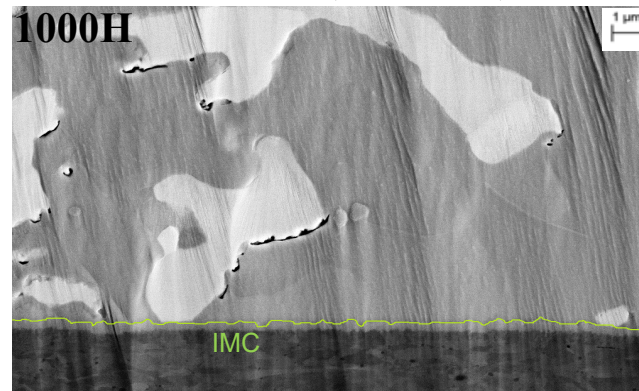
Sn Plated, 1000H



Cu (OSP), 1000H

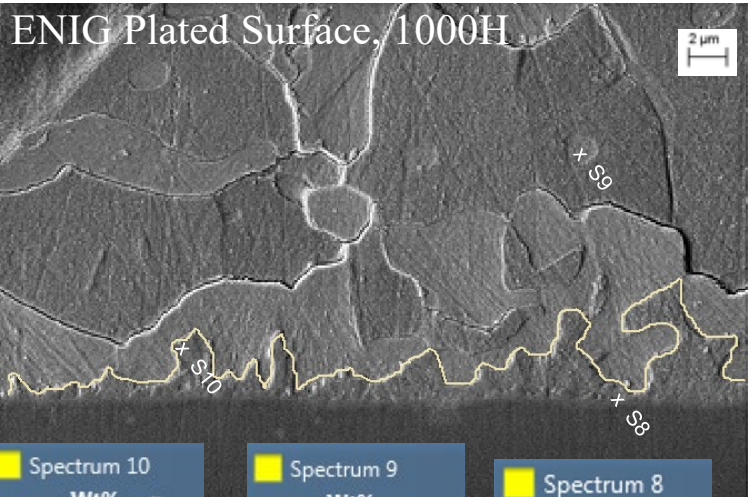


Ni/Pd/Au Plated (ENEPIG), 1000H



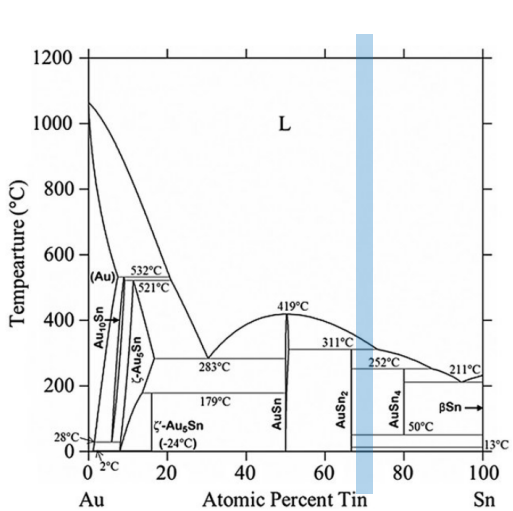
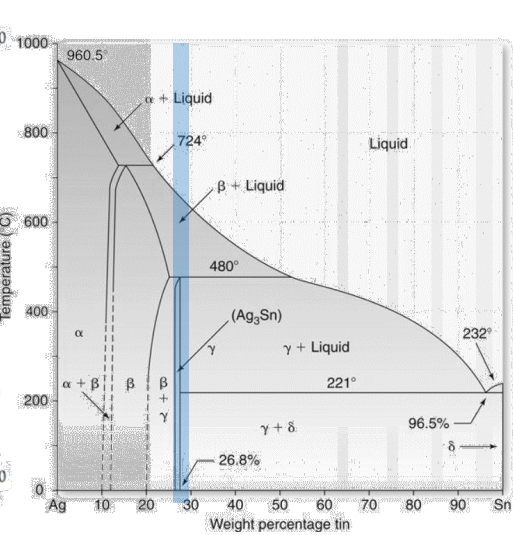
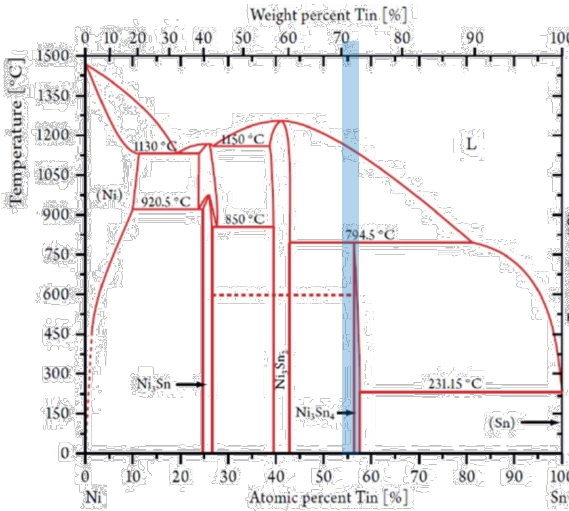
Growth of interface IMC layer thickness over thermal aging at 75°C is more obvious for Cu OSP and ENIG substrate surfaces.

INTERFACE IMC ON ENIG SUBSTRATE SURFACE

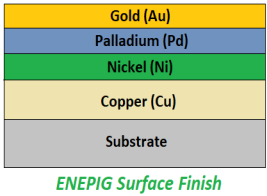
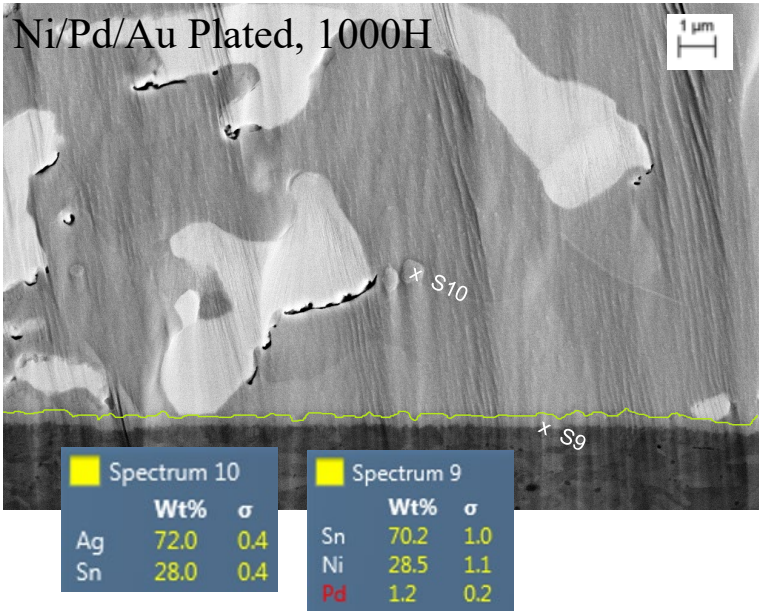
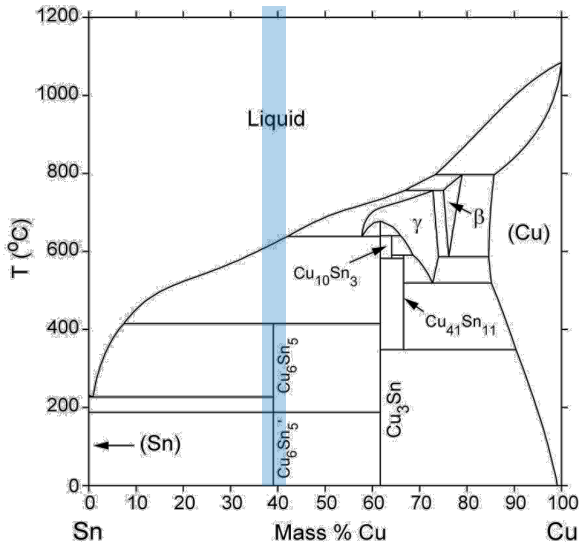
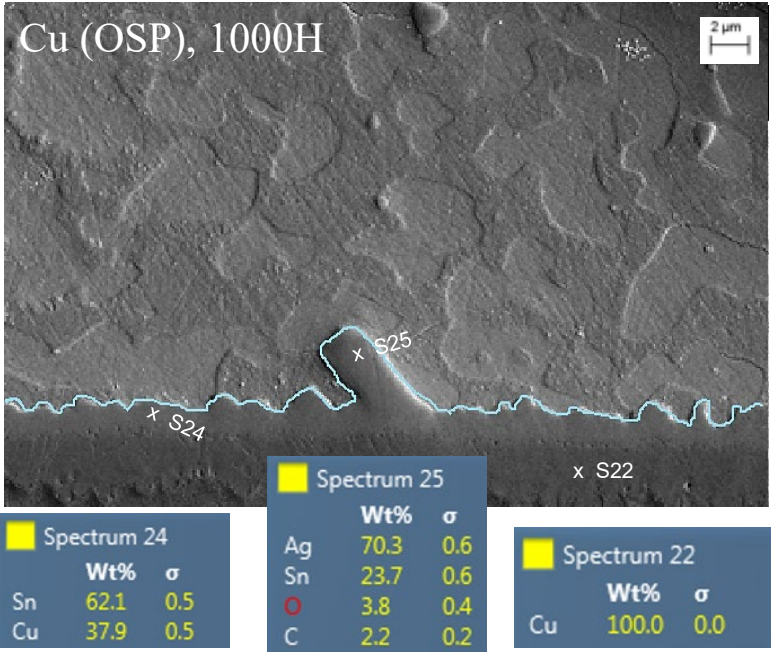


ENIG-SnBi solder interface

Spots	Elements	SEM-EDX, Wt%	Reference-Phase Diagram	Molecular weight, g/mol	Mole fraction	Typical Intermetallics
8	Ni	29.4	Ni ₃ Sn ₄ (Sn 70 – 75 wt%)	191.36	3	Ni ₃ Sn ₄
	Sn	70.6		459.54	4	
9	Ag	68.5	Ag ₃ Sn (Sn 25-30 wt%)	302.95	3	Ag ₃ Sn
	Sn	27.2		120.41	1	
10	Au	37.9	AuSn ₂ (Sn 60-65 wt%)	164.8	1	AuSn ₂
	Sn	62.1		270.02	2	



INTERFACE IMC ON CU OSP & ENEPIG SUBSTRATE SURFACE



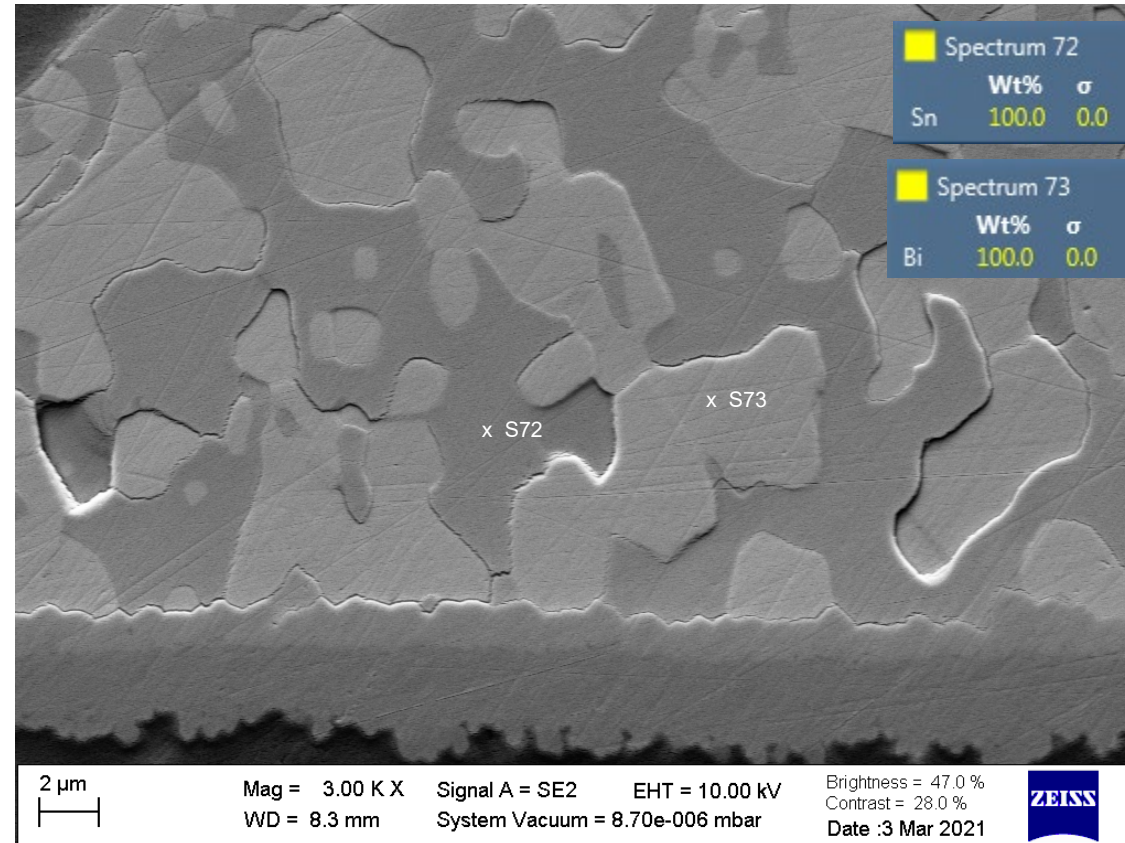
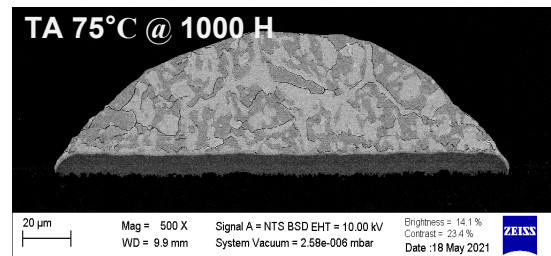
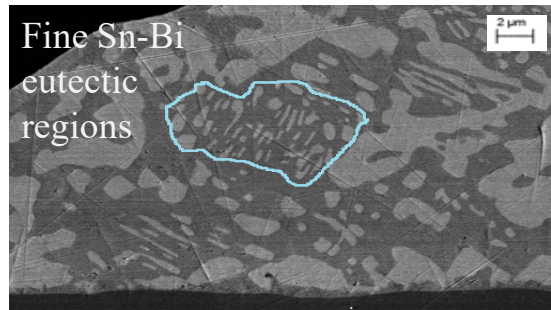
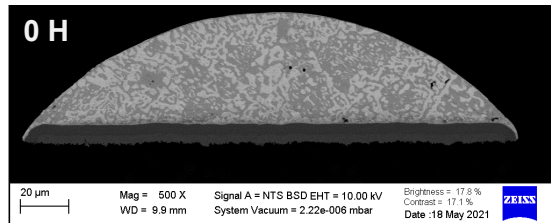
Cu OSP-SnBi solder interface

Spots	elements	Wt%	Typical Intermetallics
24	Cu	37.9%	Cu_6Sn_5
	Sn	62.1%	
25	Ag	70.3%	Ag_3Sn
	Sn	23.7%	

ENEPIG-SnBi solder interface

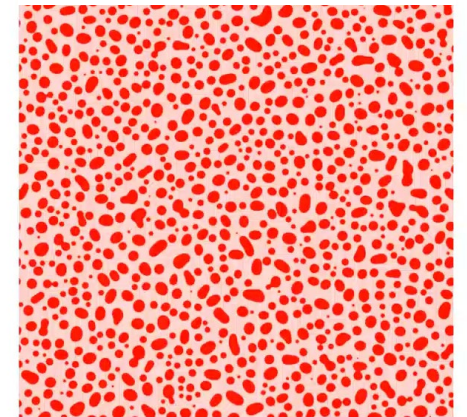
Spots	elements	Wt%	Typical Intermetallics
9	Ni	28.5%	Ni_3Sn_4
	Sn	70.2%	
10	Ag	72.0%	Ag_3Sn
	Sn	28.0%	

THERMAL AGEING (75°C)- SN-BI COARSENING (OSWALT-RIPENING)



- Sn-Bi eutectic phases are evident:
 - S73: pure bismuth phase (100% Bi)
 - S72: primary tin phase (**100% (βSn)**)

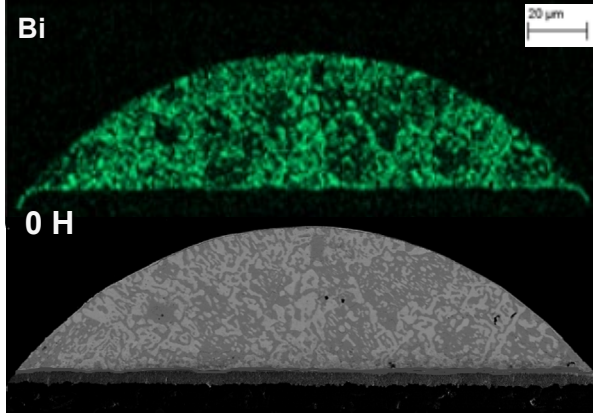
Oswalt Ripening Effect



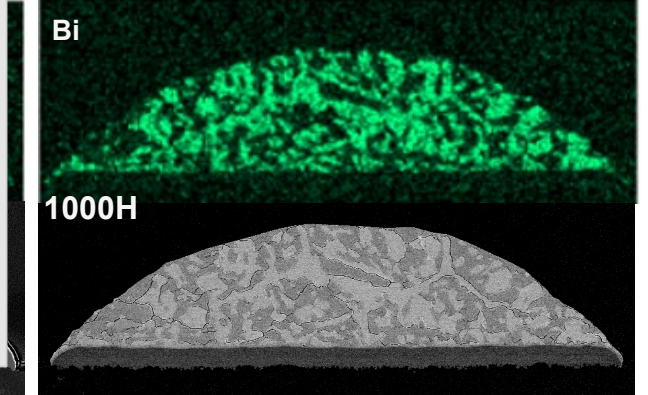
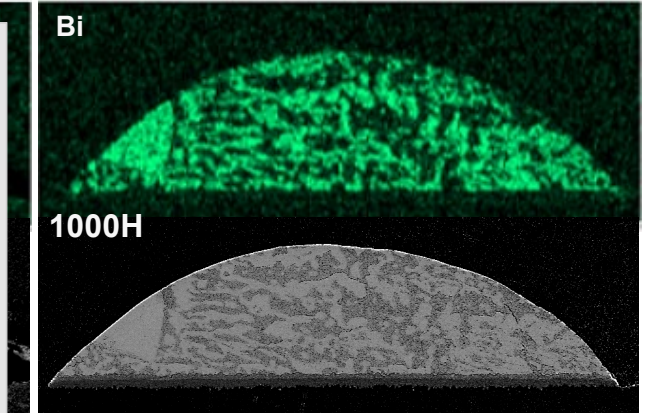
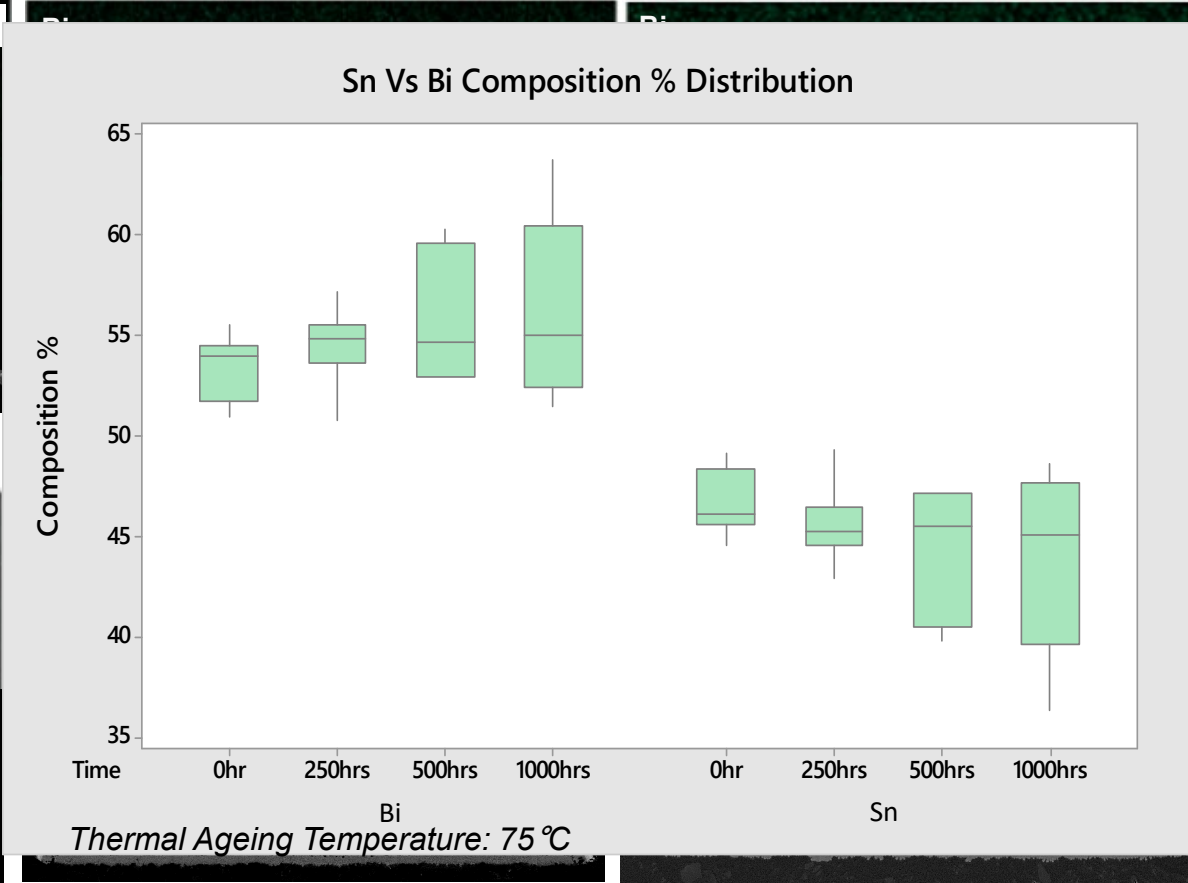
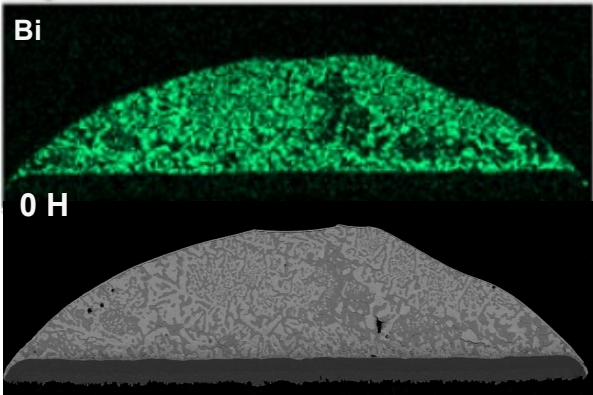
- Oswalt Ripening:** Obvious coarsening of Bi and Sn phases noticed.
- Sn-Bi interface is stable** without any significant changes in microstructure.

SEM / EDX ANALYSIS OF SN-BI COARSENING

Cu-OSP Surface

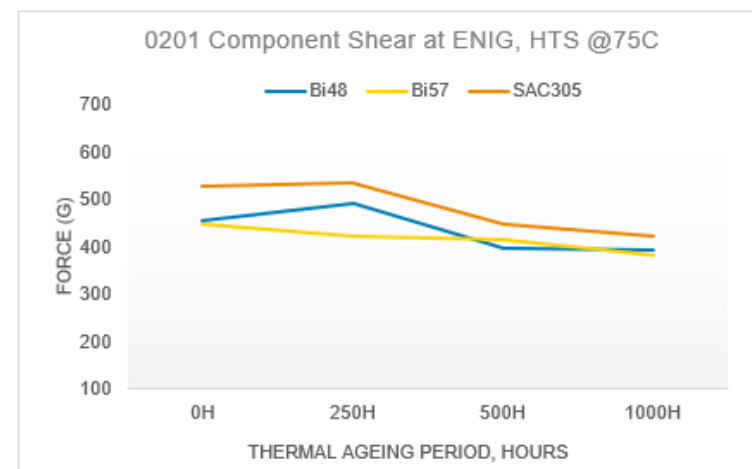
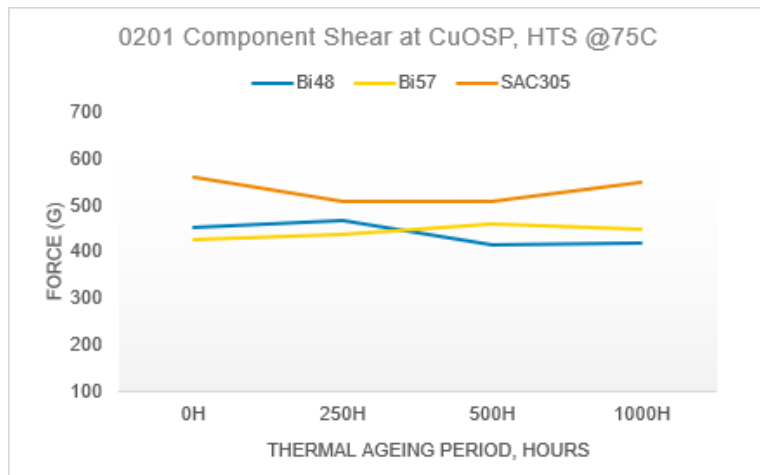
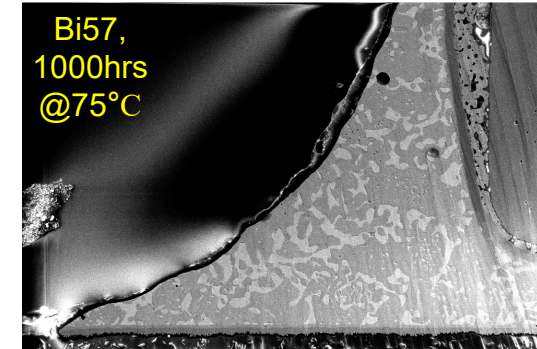
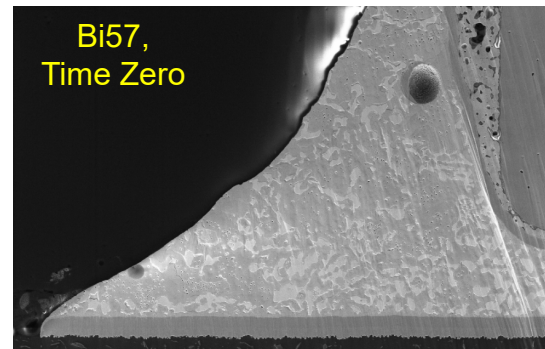
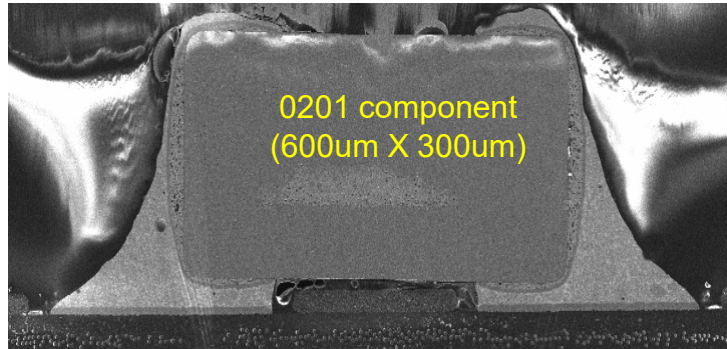


ENIG Surface



Sn and Bi phases become coarser and more inhomogenously distributed over aging time

COMPONENT SHEAR STRENGTH WITH THERMAL AGING (75°C)

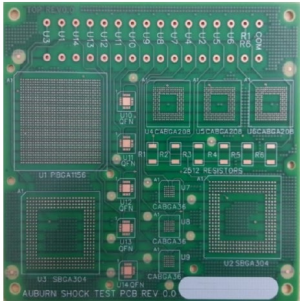


- Shear strength remains high without significant degradation over 1000Hr aging at 75°C
- Effect of interface IMC growth and Sn-Bi coarsening on shear strength is minimal

STUDY 1- THERMAL CYCLING TESTS

Low Temp. Solder Alloys	
Solder A	SnBi57Ag1
Solder B	SnBi48Ag _x
Solder G	SAC305
Solder J	SnBi48Ag _x + dopants

Conditions: **Thermal cycling profile: -40/125C** with 16.5 minutes ramps up and down (10°C per minute) and 15 minutes dwell time at 125°C and 10 minutes dwell time at -40°C. Recorded continuously the electrical connectivity of the solder joints. ENIG plated test boards



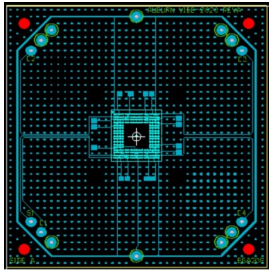
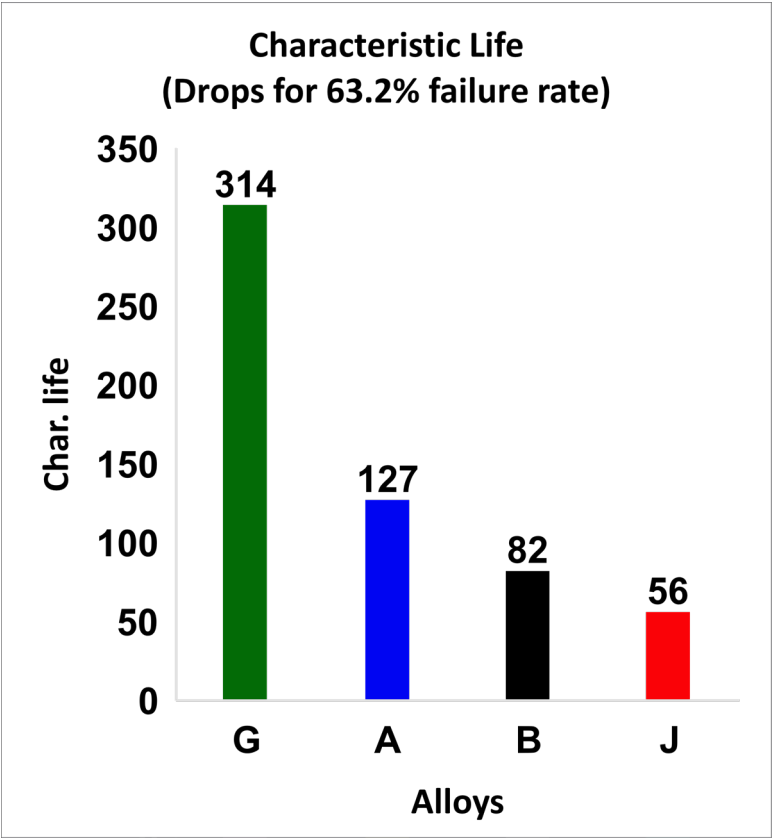
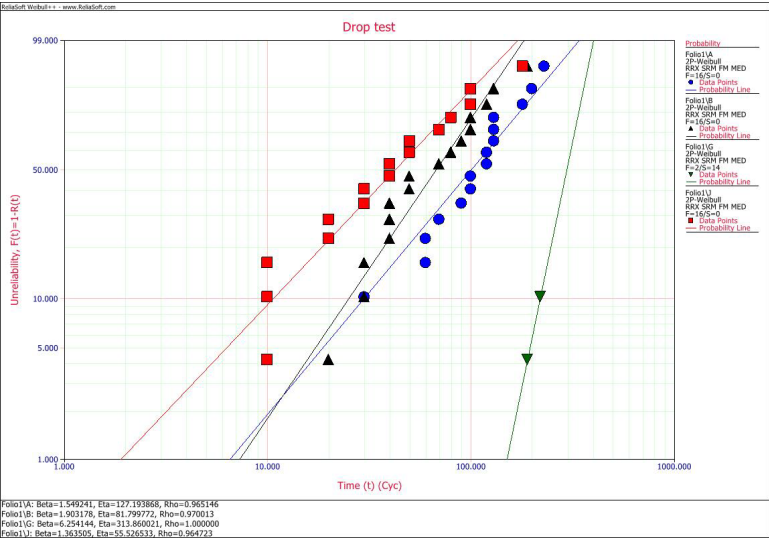
Thermal Cycling PCB

Paste	A (SnBi57Ag1)		B		G (SAC305)		J	
Component	CABGA208	SMR	CABGA208	SMR	CABGA208	SMR	CABGA208	SMR
Total Test Components	18	36	18	36	18	36	18	36
# of failed components until 1500 cycles	1	0	2	0	3	0	9	1
% failure until 1500 cycles	5.56%	0.00%	11.11%	0.00%	16.67%	0.00%	50.00%	16.67%
1st Failure	1240	0	275	0	1180	0	190	970

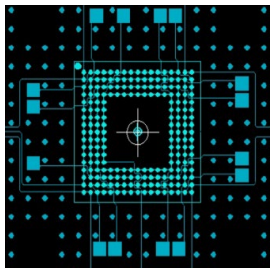
- Sn-Bi57-Ag1 showed comparable TCT performance to SAC305, and best among all low temperature solder pastes tested.

STUDY 2- MECHANICAL DROP TEST

Low Temp. Solder Alloys	
Solder A	SnBi57Ag1
Solder B	SnBi48Ag _x
Solder G	SAC305
Solder J	SnBi48Ag _x + dopants



PCB design top view



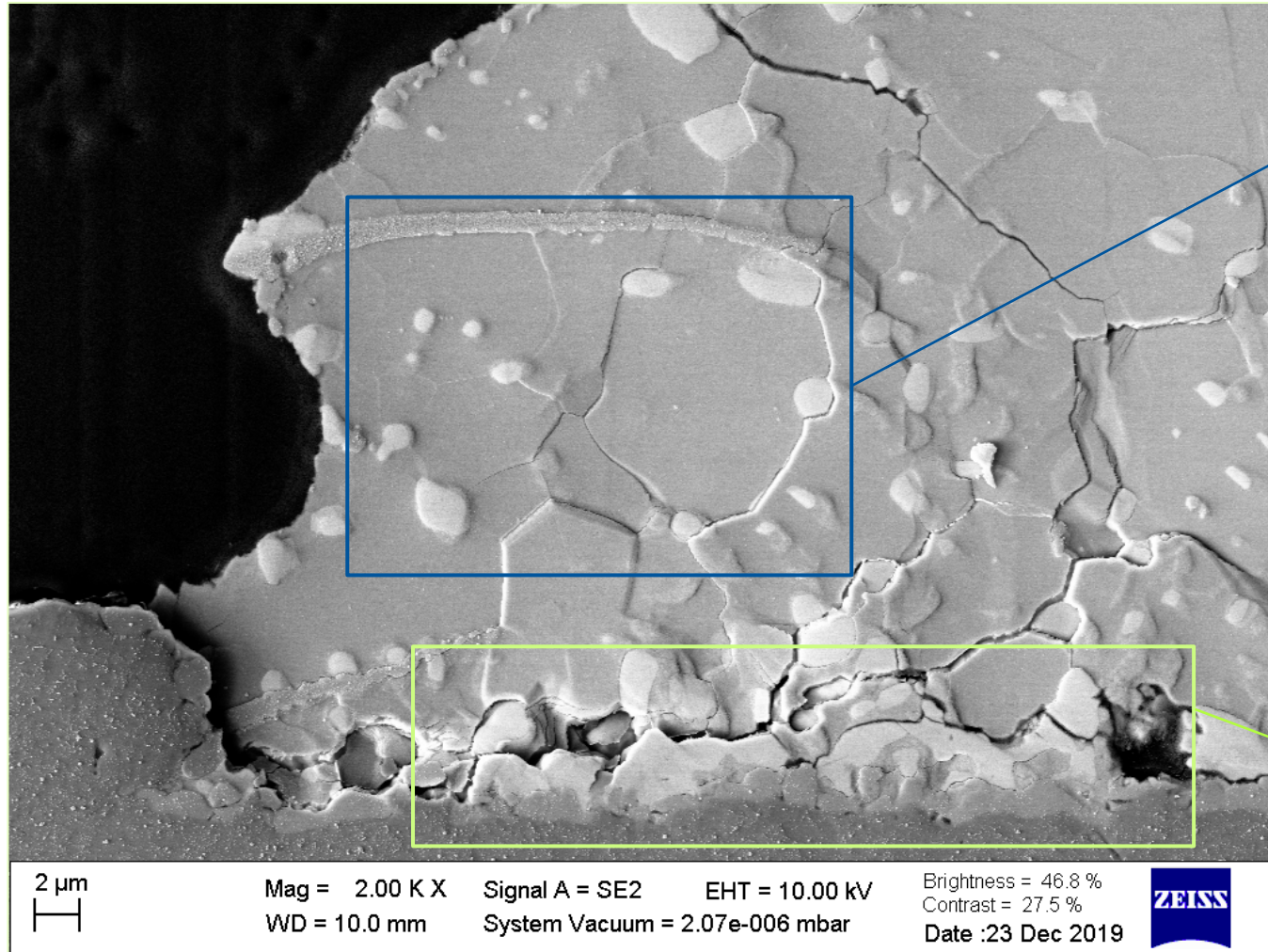
Component footprint with inspection pads

PCB are 76x76mm, 1.0mm total thickness, 6-layer board, 1/2 oz copper all layers, use IT180A for all layers, 3 mil line with 4 mil space, 4 tooling holes on OSP PCB surface finish. 15x15mm CTBGA208-SAC305 component per PCB. 16 boards per sample.

JESD22-B111 specifications to maximum peak acceleration of 1500g and half-sine shock pulse duration of 0.5 milliseconds.

■ Sn-Bi57-Ag1 (Solder A) showed drop characteristic life of >100 drops

MECHANICAL DROP TEST – CRACK ALONG BI PHASE



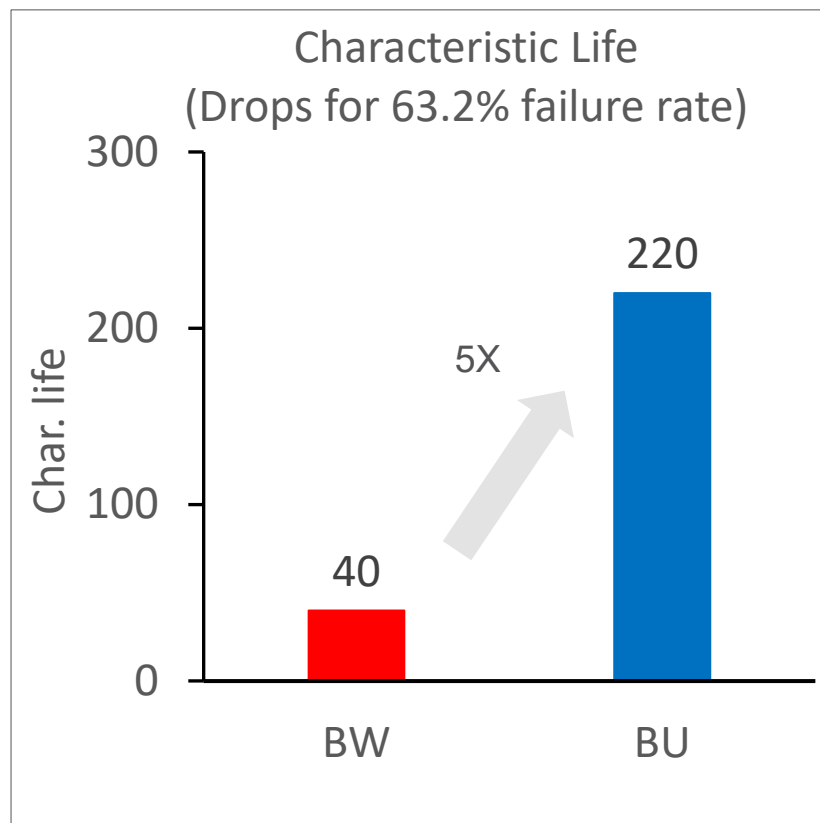
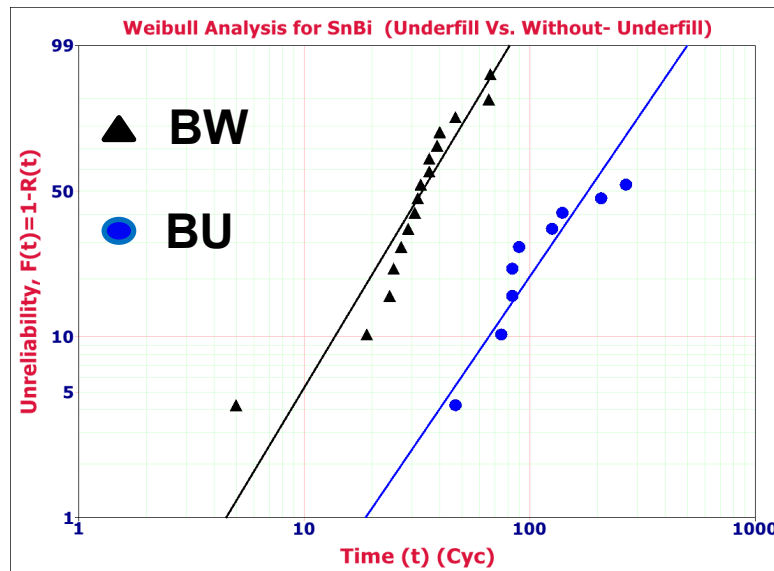
- Scattered fine bismuth phase prolong the crack propagation via Sn eutectic (grain) boundaries.

- Agglomerated large bismuth phase accelerated crack propagation via weak Sn-Bi eutectic interface.

STUDY 3- MECHANICAL DROP TEST WITH UNDERFILL

Low Temp. Solder Alloys

AU	SAC305 with Underfill
AW	SAC305 without Underfill
BU	SnBi57Ag1 with Underfill
BW	SnBi57Ag1 without Underfill



- Deviation in drop test characteristic life as compared to Study 2 without underfill
- Further Investigations in progress on:
 - Substrate condition
 - Reflow profile control
 - Paste volume control
 - Flux formulation control

- With underfill, Sn42-Bi57-Ag1 (BU) showed >5X increase in drop characteristic life
Applicable for SiP modules with underfill and molding

AGENDA

1

Introduction

- System In Package for 5G applications
- Thermal Budget Challenge In Dual-sided SiPs

2

Low Temperature Solder Material

- Tin-bismuth-silver (Sn-Bi-Ag) low temperature alloy properties
- Solder bump microstructure and Intermetallic phase development with thermal aging
- Thermal cycling and mechanical drop tests

3

Targeting Ultra-fine Pitch Application

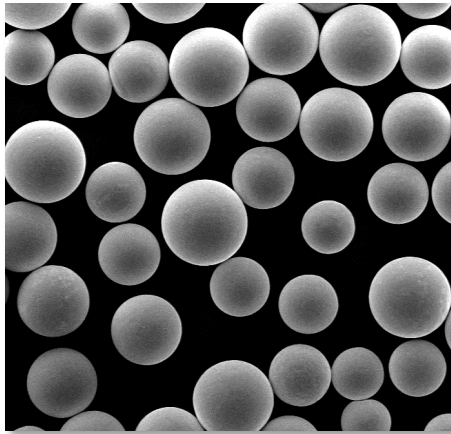
- Paste formulation- powders and flux

4

Q & A

SOLDER PASTE FORMULATION FOR FINE-PITCH SIP APPLICATION

Fine-pitch Solder Paste Formulation:



Fine-pitch Powder

- Type 6, 7, 8 and beyond
- Alloys: SAC305, SnBiAg
- Made with unique Welco™ technology



Flux System

- Designed to work with fine pitch powders for optimal paste performance



Solder Paste for SiP

- Consistent paste release at ultra-fine pitch printing
- Minimal voids & beading
- Long stencil life & staging

SUMMARY

- **Low temperature solder paste material can effectively address thermal budget challenges in dual-sided SiPs for 5G applications (RFFE, AiP, etc.)**
- **Low temperature alloy Sn-Bi57-Ag1 demonstrated best reliability performance for thermal aging (75°C), thermal cycling and drop tests**
- **Key to have the right solder paste formulation for ultra-fine pitch SiP applications**

AGENDA

1

Introduction

- System In Package for 5G applications
- Thermal Budget Challenge In Dual-sided SiPs

2

Low Temperature Solder Material

- Tin-bismuth-silver (Sn-Bi-Ag) low temperature alloy properties
- Solder bump microstructure and Intermetallic phase development with thermal aging
- Thermal cycling and mechanical drop tests

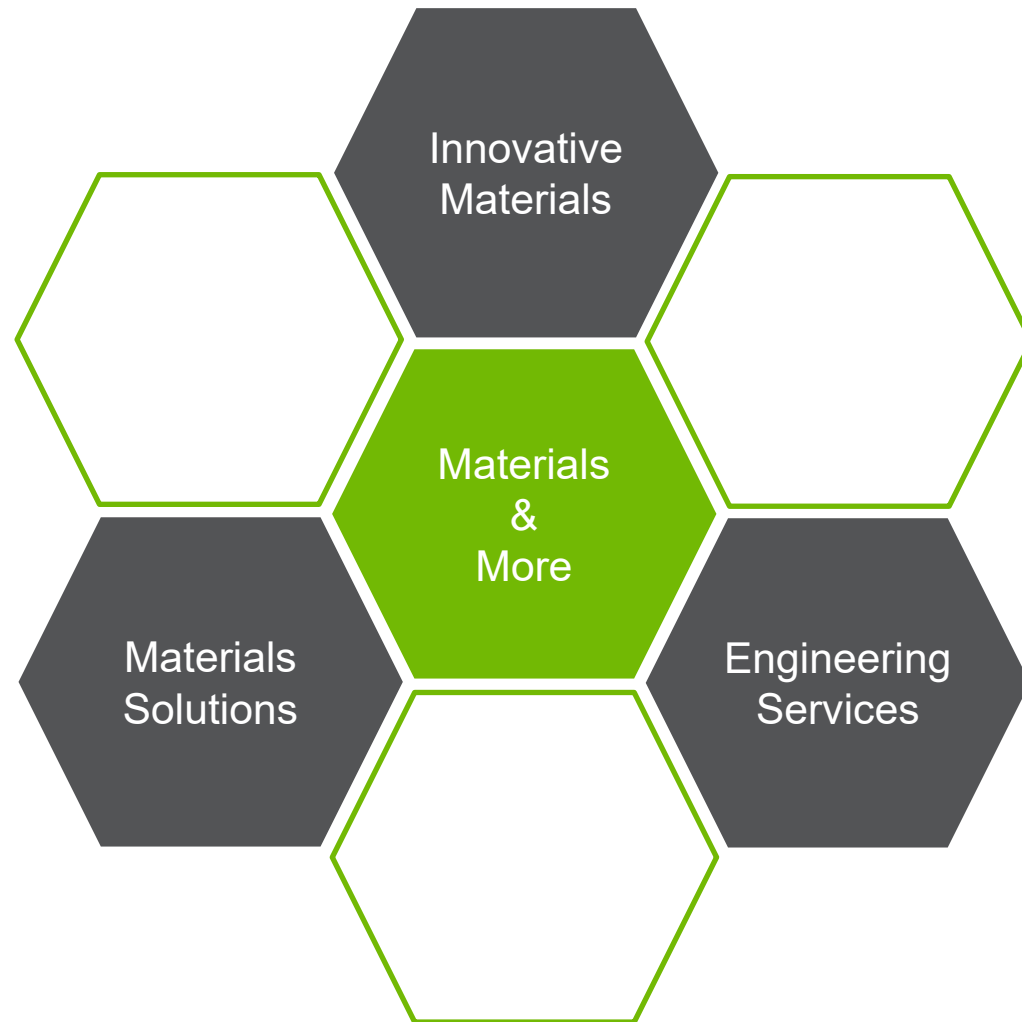
3

Targeting Ultra-fine Pitch Application

- Paste formulation- powders and flux

4

Q & A



Thank you for your attention.
For more information, visit
[Heraeus Electronics](#)