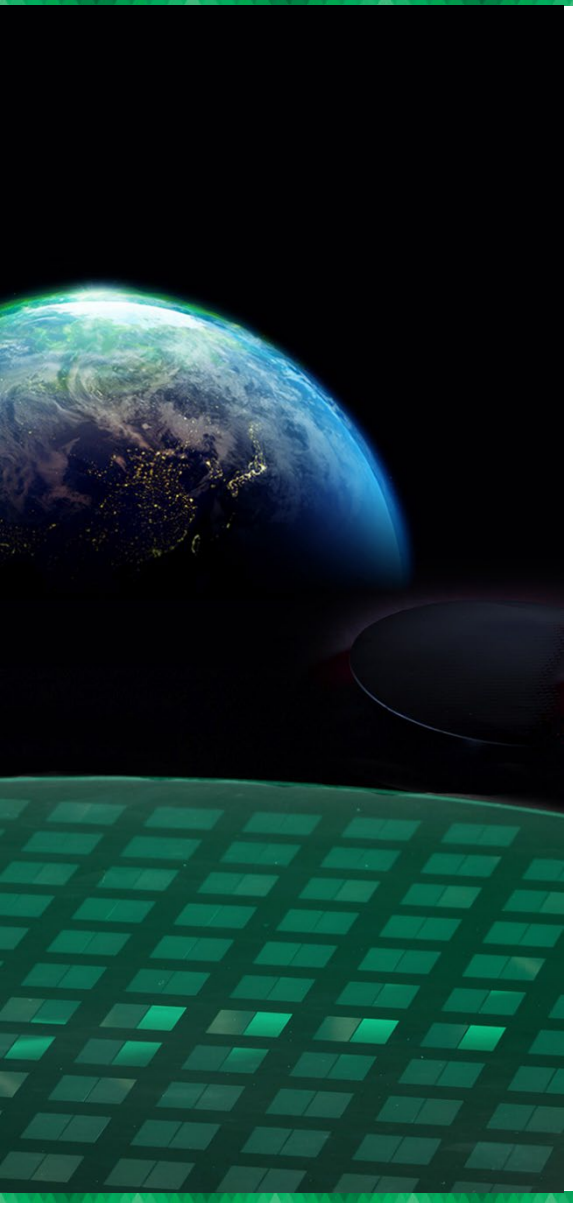

Immersion tin plating enabling reliable wettable flanks on QFN packages

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Lead frame based bottom terminated IC packages

Rapid growth in the automotive industry due to the increase in electronic components in cars and the expanding electric vehicle market*:

- Form Factor
  - Low foot print
  - Low thickness (<1 mm)
- Production cost reduction
  - Low failure rates
- Electrical and thermal performance
  - Heat dissipation to PCB

Electric vehicles	Autonomous vehicles	Connected vehicles	Mobility as a service
New powertrain	Sensors	Vehicle	Ridesharing
Charging infrastructure	HPC	Infrastructure	Car sharing
Better technology	Big data / Analytics	Cloud	Flexible bus
Modularization	AI/ Deep learning	Wearables and personal devices	Micro mobility
	Navigation and guidance		Delivery

*M. A. Mangrum, “Side Wettable Flanks for Leadless Automotive Packaging”, Semiconductor Engineering Whitepaper, October 10, 2020,

*U. Welzel, et.al,, “Wettable-Flanks: Enabler for the use of bottom-termination components in mass production of high-reliability electronic control units”, SMTnet Technical Library, May 23, 2018.

Leadframe assembly processing flow

Etch / stamped lead frame

Selective silver plating

Die attach

Flux + Oxide Cleaning

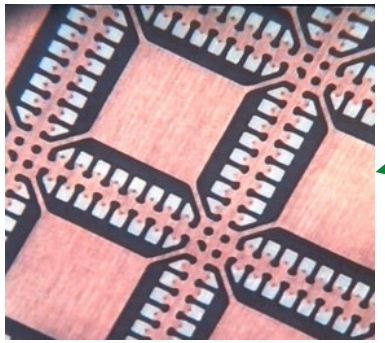
Mold adhesion improvement

Molding

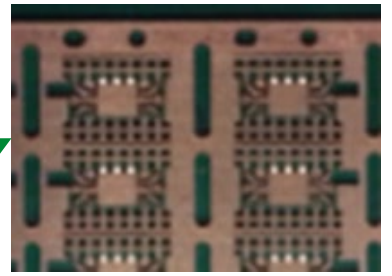
Deflashing

Solder Plating

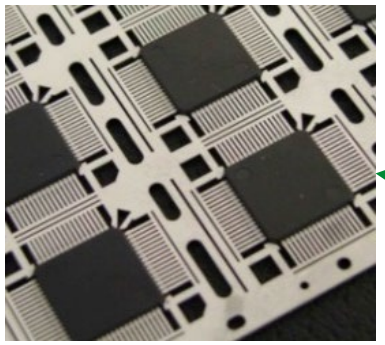
Singulation



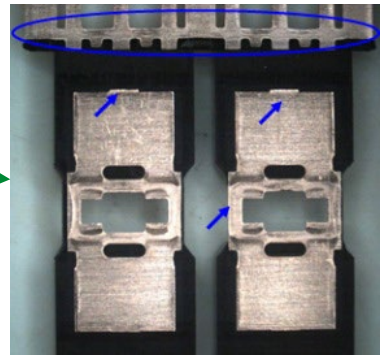
Selective silver plating



Surface roughening

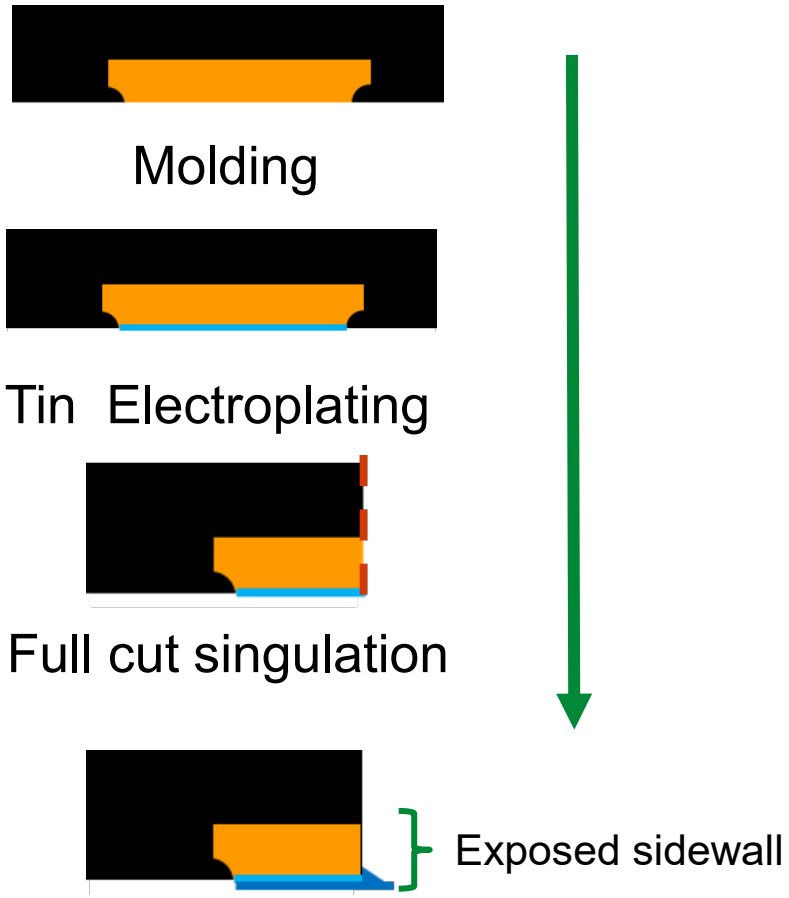


8 – 12 μm tin plating



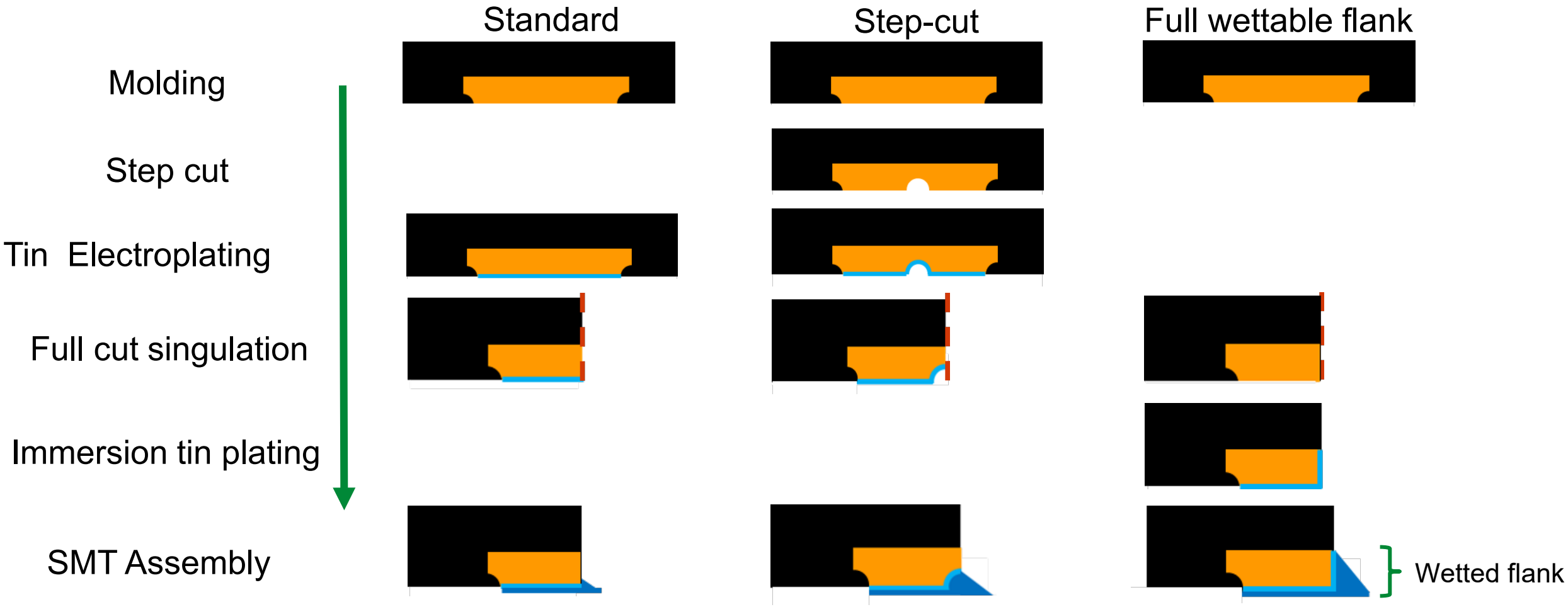
Electrodeflash

High reliability requirements



- Underside solder joints are not visible on mounted packages in automatic optical inspection (AOI).
- On the optically visible sidewalls a solder fillet does not form.
- Automatic X-ray inspection imposes package lay-out restrictions.
- Solder filler on the flanks of the package leads improves the reliability of solder joints.

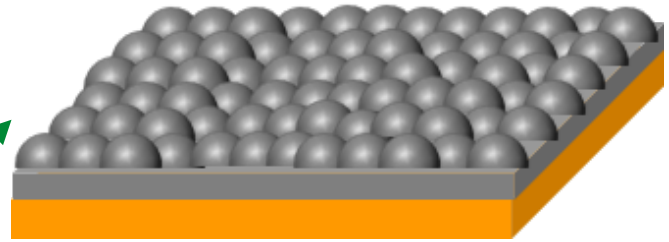
QFN lead frame assembly processing flow



Immersion tin plating

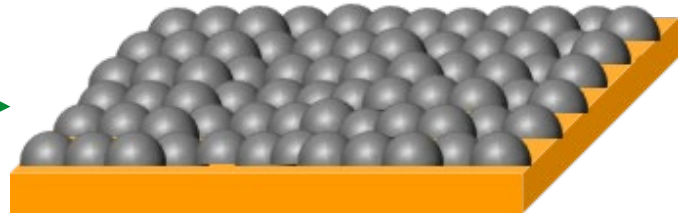
Immersion tin solder finishes:

+ Planar flat surface
+ Very good solderability
- Exposed tin oxidation risk
- Tin whiskering risk



> 2 μm thickness

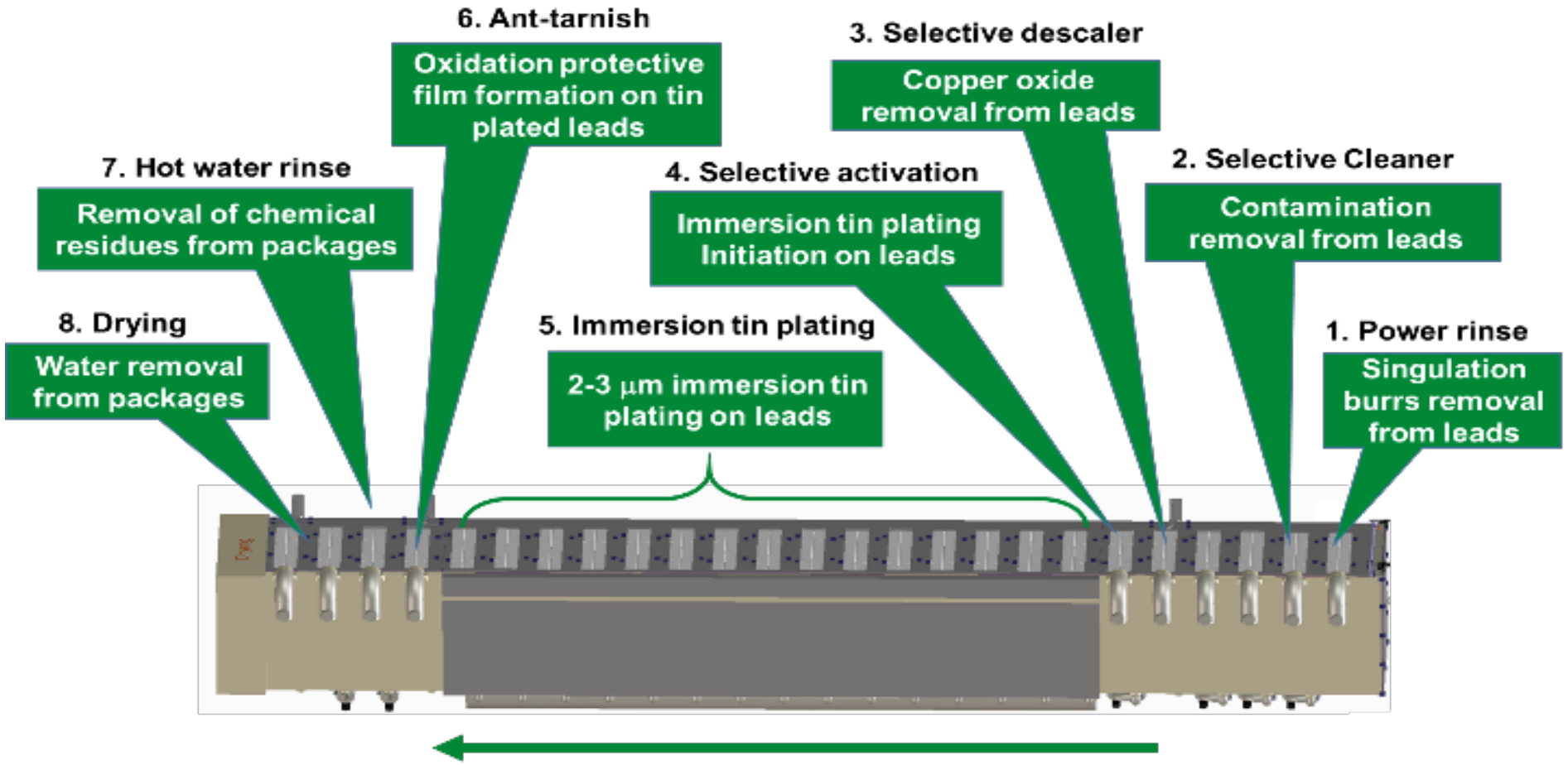
$Sn^{2+} + 2e^- \rightarrow Sn$



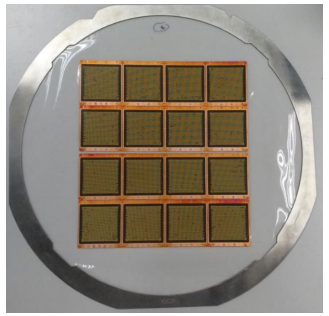
Self limiting at < 1.5 μm thickness

$Cu \rightarrow Cu^{2+} + 2e^-$

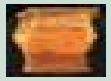
Immersion Tin process flow

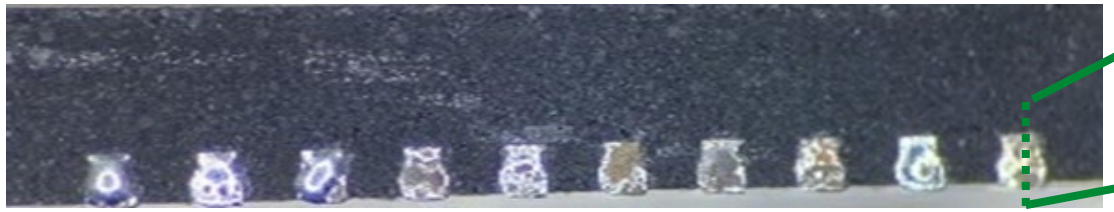


Process flow

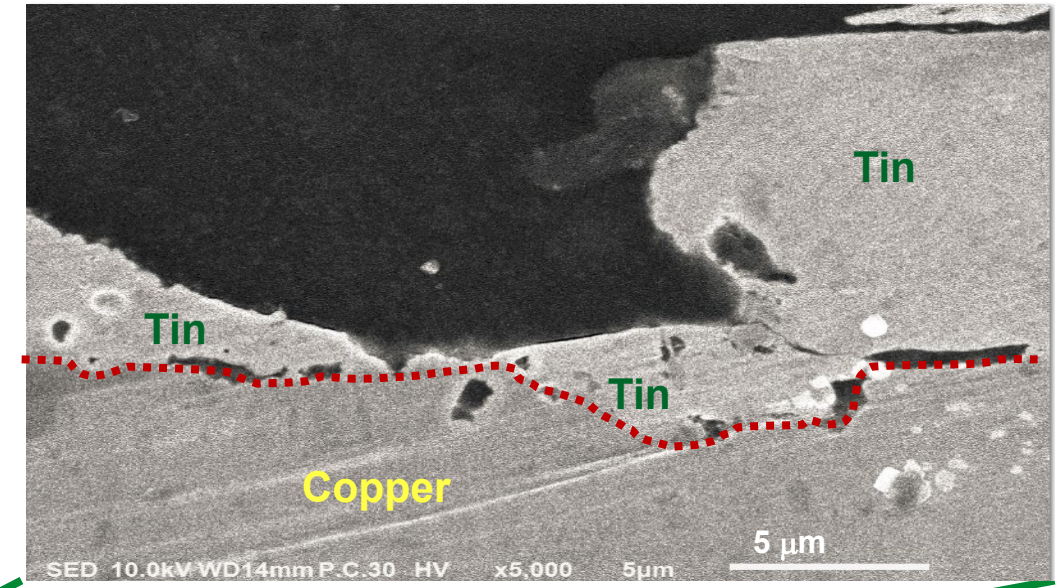


Sidewall surface roughness

Company	Sidewall	Surface Roughness [Sdr]*	Solderability test
A		0.04	Pass
B		0.02	Pass
C		0.03	Pass
D		0.05	Pass
E		0.04	Pass
		**0.07**	**Fail**



Lead side-wall cross-section



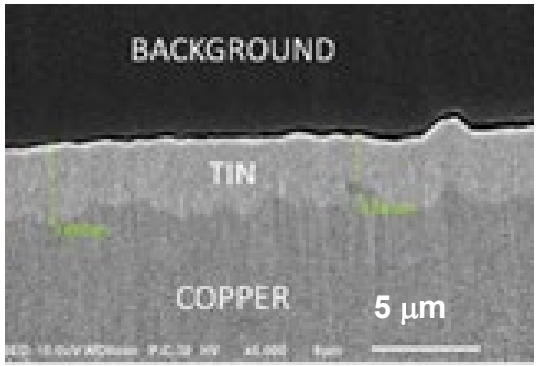
*Sdr = Developed interfacial area ratio

Selective cleaner mechanism

Surface oxidation / contamination

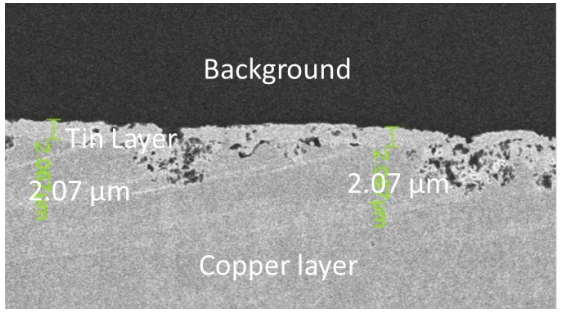
Selective cleaner

Contamination residues in surface roughness valleys removed



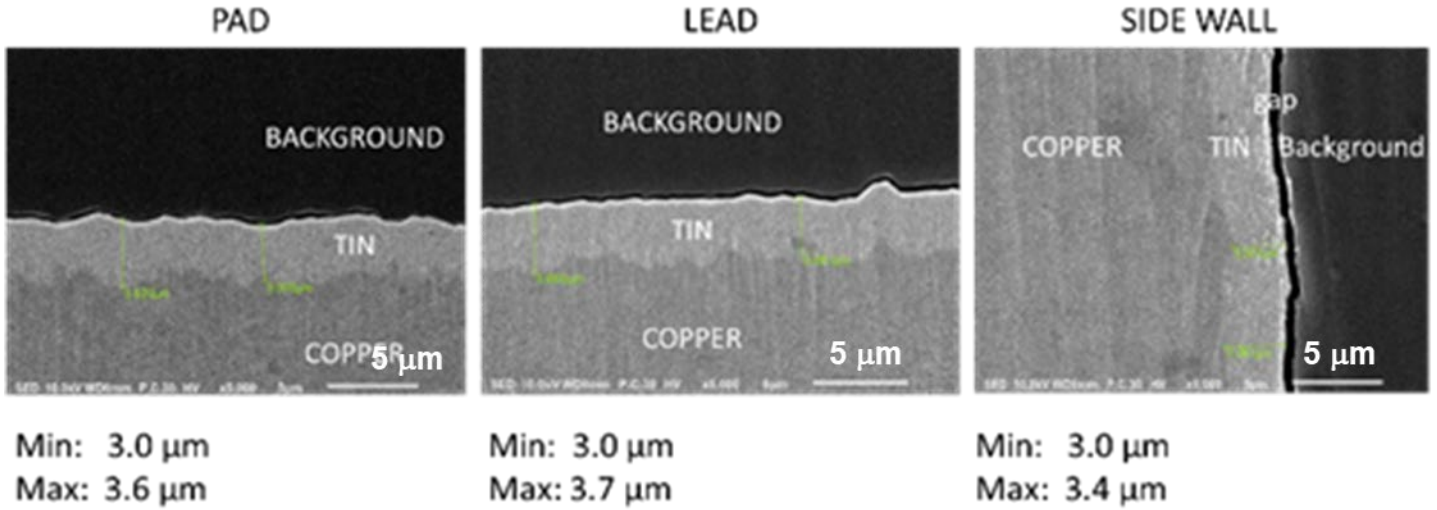
Cleaner

Contamination residues in surface roughness valley's



Immersion tin plating process

1. Fine-grained tin crystal structure
- Smooth and uniform tin layer
- Reduces tin whiskering*
- More uniform copper-tin intermetallic layer

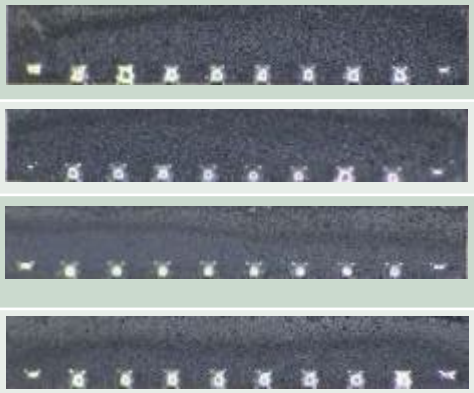
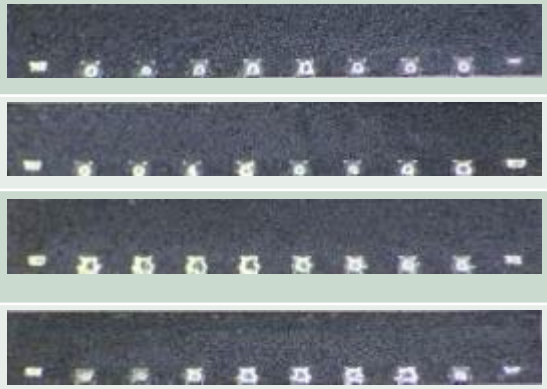
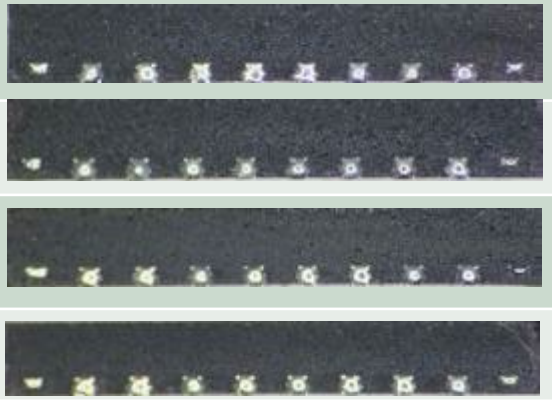


2. The autocatalytic immersion tin process
- Thickness 2 – 4 µm
- Reaction kinetics are purely heat driven: 70-75°C

Immersion time [min]	30	45	120
Thickness [µm]	1.5-2.0	1.9-2.7	3.2-4.9
	1.5-1.9	1.9-2.4	3.0-4.8
	1.6-1.9	1.9-2.2	2.9-3.4

*K. Whitlaw, et.al, “A new fine-grained matte pure tin for semiconductor lead-frame applications”, Circuit World, vol. 32/1, 2006, pp. 23–30.
*M. Tsujimoto, at.al“The Elimination of Whiskers from Electroplated Tin”, NASF Surface Technology White Papers, vol. 78(12), 2014, pp. 9 – 18.

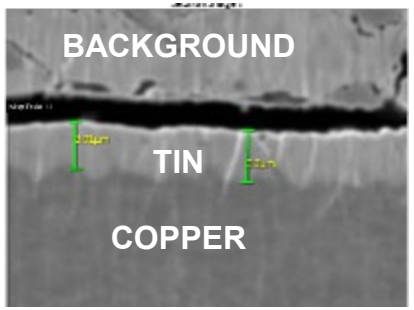
Solderability (JEDEC J-STD-002E)

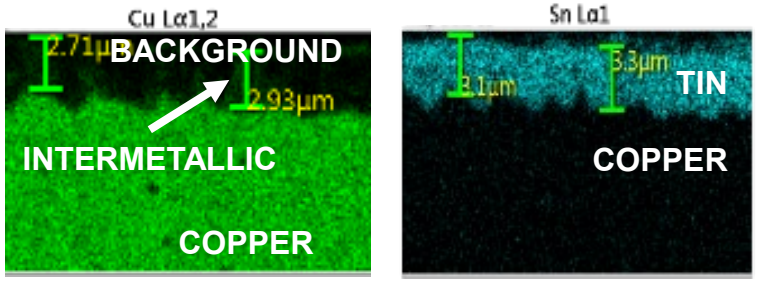
	Zero Hour	8h steam aging at 93°C/80-90%RH	16h dry bake at 150°C
QFN 5x5 –32L			
Sidewall	100% solder coverage (6/6)	100% solder coverage (6/6)	100% solder coverage (6/6)
Lead	100% solder coverage (6/6)	100% solder coverage (6/6)	100% solder coverage (6/6)
Pad	100% solder coverage (6/6)	100% solder coverage (6/6)	100% solder coverage (6/6)

Intermetallic formation after steam aging

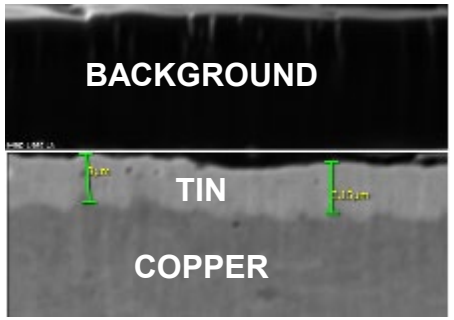
Besi

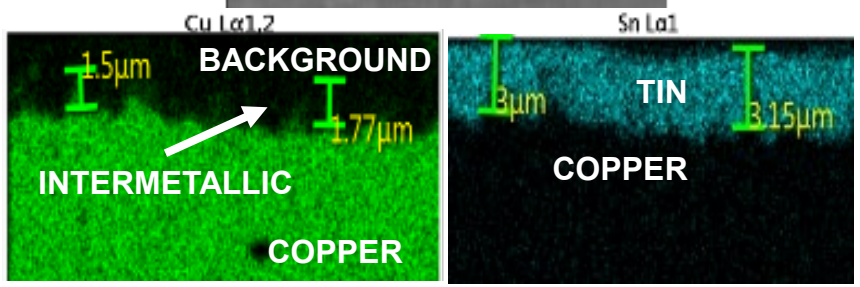
PAD



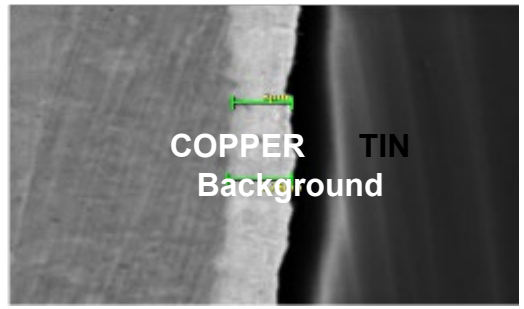


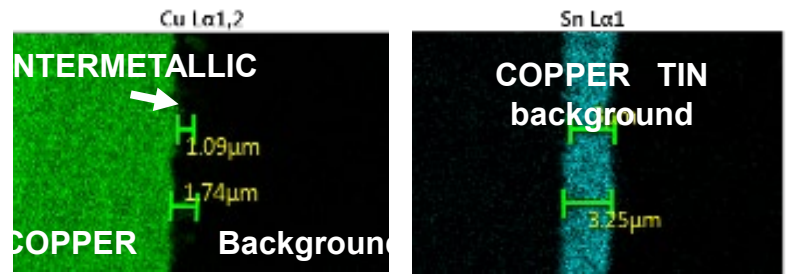
LEAD





SIDE WALL





Total Thickness	Intermetallic layer	Remaining Tin layer	Total Thickness	Intermetallic layer	Remaining Tin layer	Total Thickness	Intermetallic layer	Remaining Tin layer
3.1 µm	2.7 µm	**0.4 µm**	3.0 µm	1.5 µm	**1.5 µm**	3.0 µm	1.1 µm	**1.9 µm**
3.3 µm	2.9 µm	**0.4 µm**	3.2 µm	1.8 µm	**1.6 µm**	3.3 µm	1.7 µm	**1.6 µm**

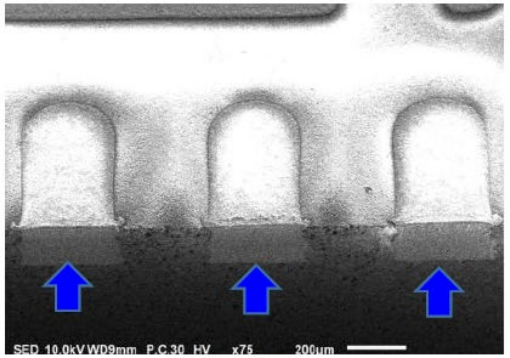
8h steam aging at 93°C/80-90%RH

Tin whisker test

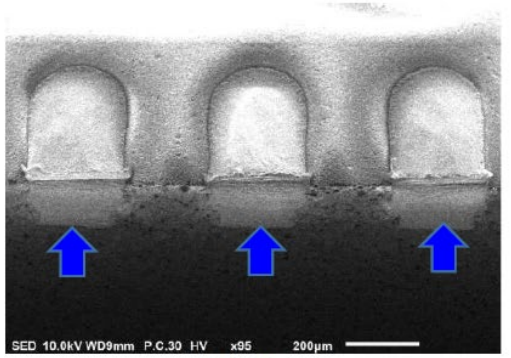
No whiskers observed on lead flanks after (JESD22-A121)

1. 4000h storage @ 30 ± 2°C and 60±3% RH
2. 4 week storage + tin reflow pre-condition and
   1. 4000h storage @ 55 ± 3°C and 85±3% RH
   2. 1500 cycles: -55°C(+0°/-10°) ; 85°C (+0°/-10°)

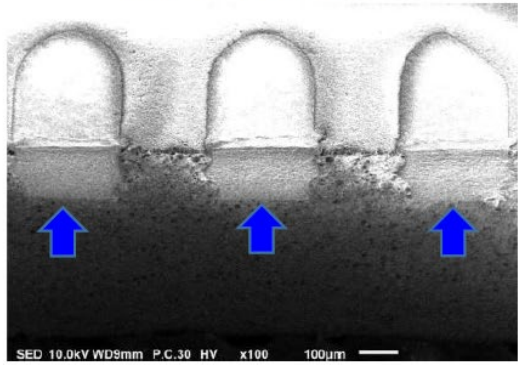
Package type	Tin thickness [µm]	
	Minimum	Maximum
20L QFN 5x5	2.1	2.8
24L QFN 4x4	2.1	2.6
26L QFN 4x6	2.0	2.6
32L QFN 5x5	2.0	2.9



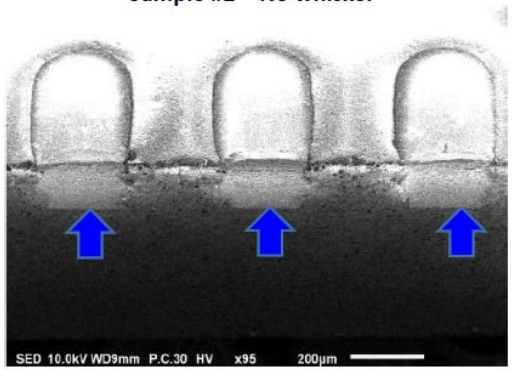
20 VQFN 5x5
Sample #1 – No whisker



24 VQFN 4x4
Sample #2 – No whisker

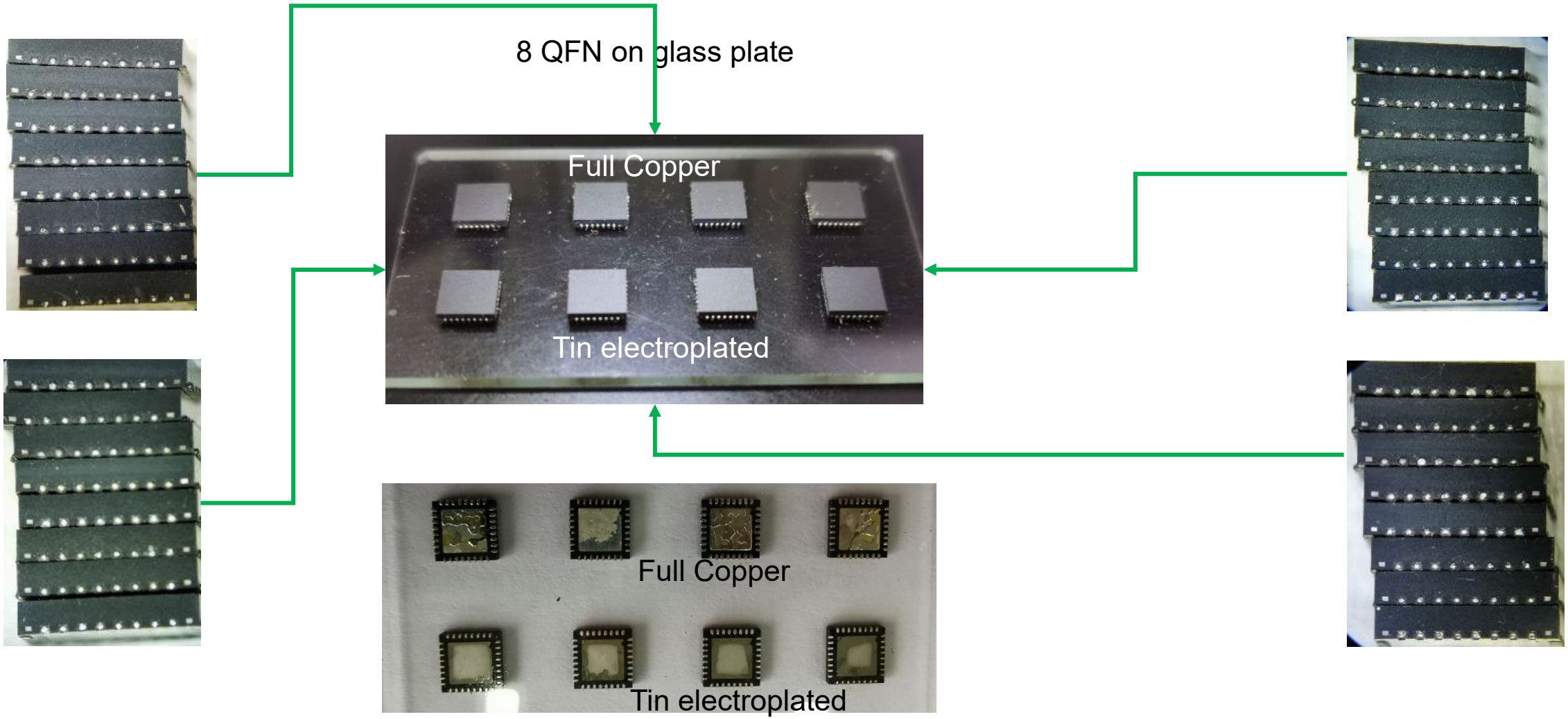


26 VQFN 4x6
Sample #3 – No whisker



32 VQFN 5x5 – Sample #4
No whisker

Glass ceramic test



Sidewall fully soldered after zero hour, 16 hours dry bake and 8 hours steam aging

Summary

The presented immersion tin process produce good quality tin wettable flanks on exposed copper side-walls of singulated QFN packages mounted on singulation tape.

- 2 - 4 μm fine-grained, uniform and smooth tin layers.
- 0.5-1.5 μm of unreacted tin left after aging yields full side-wall, lead and pad solder wetting according to JEDEC J-STD-002E standard solderability tests for component lead durability.
- No whiskering observed after standard aging test for tin whiskering (JESD22-A121).
- Further qualification tests at leadless package and automotive electronics suppliers are on-going.

THANK YOU !

FOR MORE INFORMATION

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