High-throughput Printing of Micro and Nanoscale Interconnects, and Passive and Active Electronics Elements for Heterogeneous Integration and Advanced Packaging Applications

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Outline

- Introduction
- How does it work?
- Nanoscale Directed Assembly-based Processes
- Electrophoretic Assembly
- Fast fluidic Assembly
- Crystalline and single crystal printing of metals and semiconductors
- Applications (Interconnects, Transistors, Diodes, display, Sensors)
- Scalable and fully automated Fab-in-a-Tool
- Summary

Only Large Companies Can Make Nanoscale Electronics

- Can you input your design and materials on one end and have your electronics come out the other end on the same day using one machine?
- Can the cost be 10-100 times less than conventional fabrication?
- Can any small or mid size company can make their own chips on the same day?

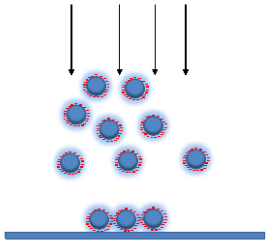
Yes!

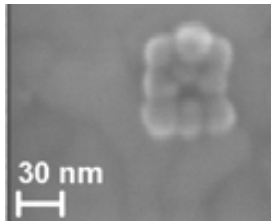
How does it work

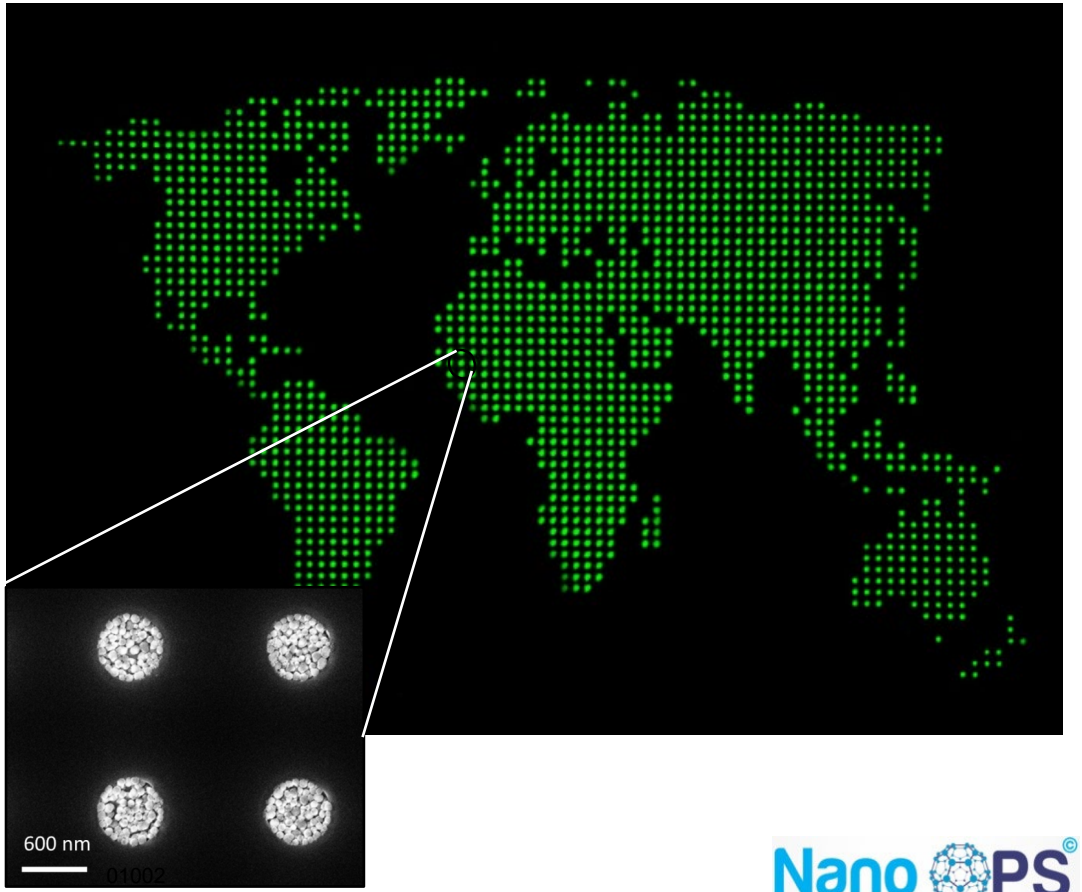
Nature uses bottom-up self-assembly, molecule by molecule, cell by cell.

We directly assemble each nanoparticle to print a circuit pattern.

Directed assembly-based printing







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The New Future of Electronics Manufacturing is Here

- Feature size down to 25nm
- 10 – 100 times reduction in cost;
- 10 – 100 times faster;
- 1000 times reduction in materials use;
- Eliminates 100s of process steps;
- 1000 times faster than inkjet or 3D printing;
- Prints crystalline metal and semiconducting structures

Print electronics using any material on any surface

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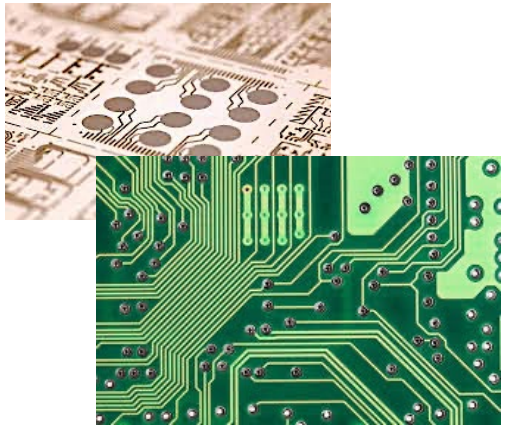
The Big Chasm in Manufacturing of Electronics

Microscale, low cost, and low throughput

Nanoscale, low cost and high throughput

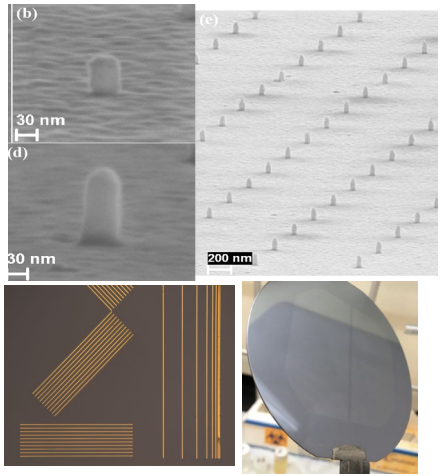
Nanoscale, high cost, and high throughput

Additive Manufacturing of Electronics (Conventional Printed Electronics)



Inkjet and screen printing industry

Nanoscale Additive Manufacturing of electronics



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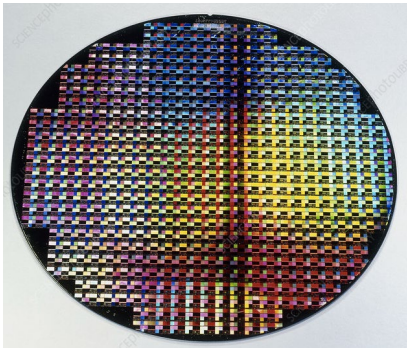
Nanoscale Conventional Semiconductor Fabrication

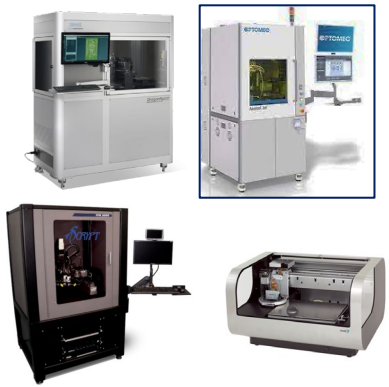


Semiconductor Equipment industry

Electronics Manufacturing Landscape

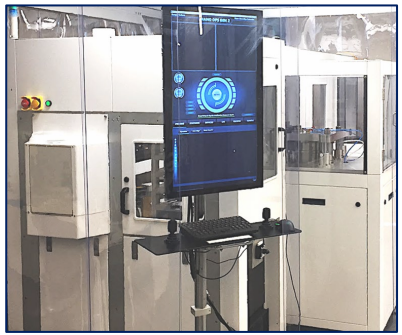
Microscale

- ✓ Low end & low throughput
- ✓ Low cost



Micro & Nanoscale

- ✓ High end & high throughput
- ✓ Low cost



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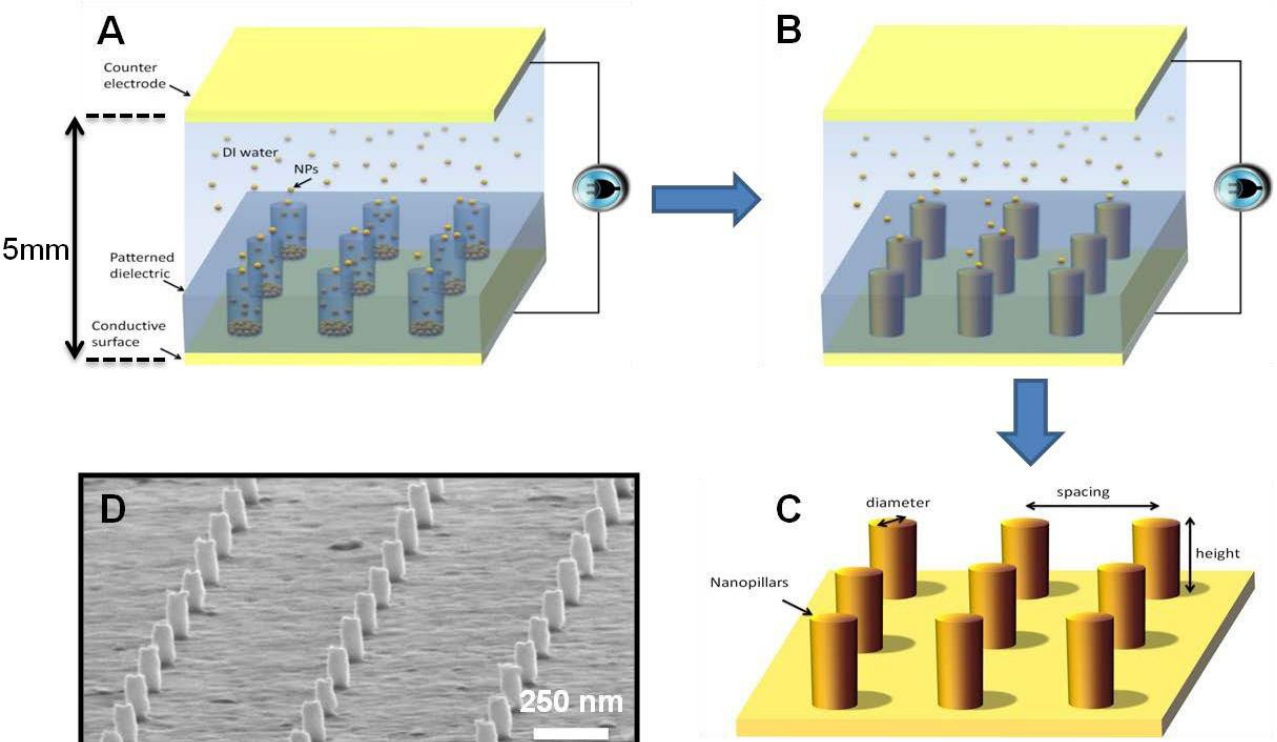
Micro & Nanoscale

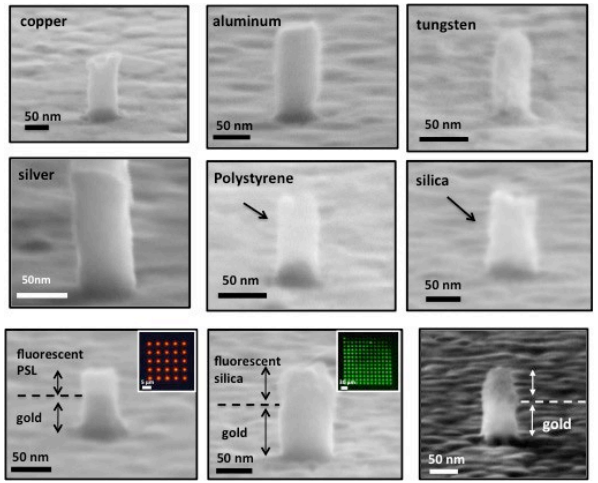
- ✓ high-end & high throughput
- ✓ High cost

Process and Printed Circuit Structures

Electrophoretic Directed Assembly Printing Process – EPx Platform

Printed Interconnects

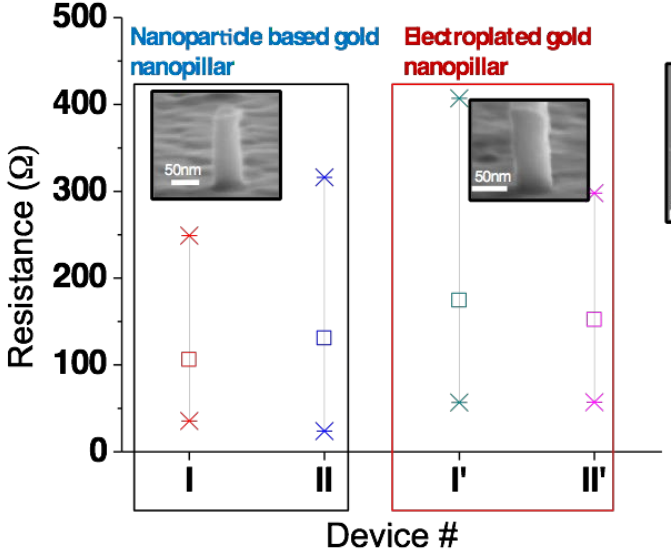


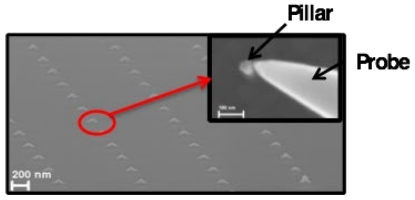


All assembled Nanoparticles are completely fused insitu.

ACS Nano, 8 (5), 2014.

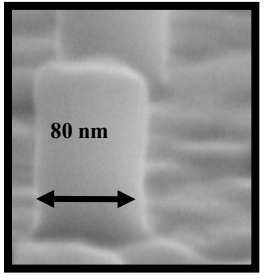
Interconnects Properties

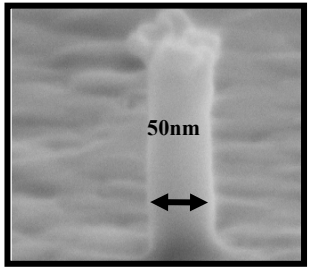


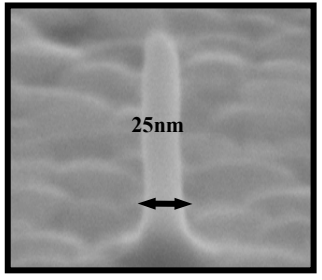


Resistance of assembled interconnects is the same as bulk (electroplated interconnects).

Crystalline Au Pillars



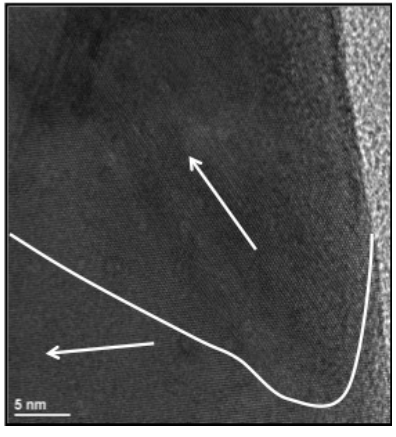




Directly assembled structures properties are equivalent to electroplating, CVD and PVD fabrication.

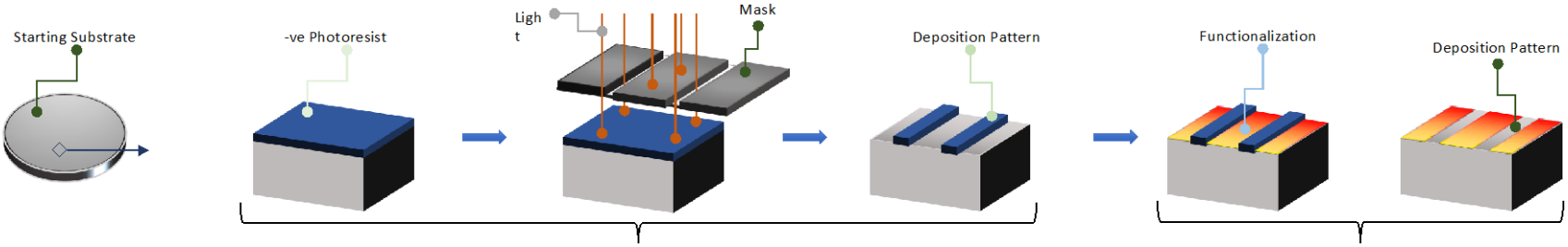
Directly assembled metallic structures (Cu, Ag, Al, Au, and W, etc.) in addition to semiconductors and dielectrics were demonstrated.

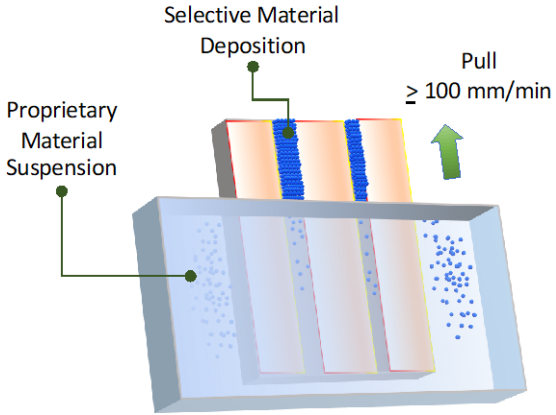
- TEM shows that NPs completely fuse without any voids.
- Nanopillars have polycrystalline nature.



ACS Nano, 8 (5), 2014.

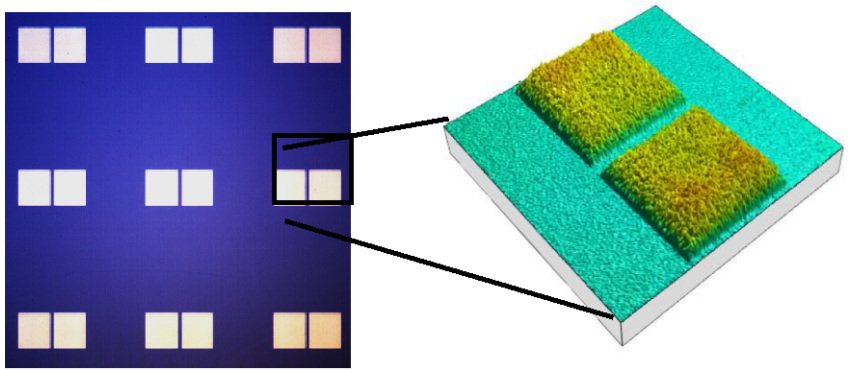
Fast Fluidic Assembly Process – FFx Platform





Fast Fluidic Process

SiO_2 substrate – 10 µm spacing



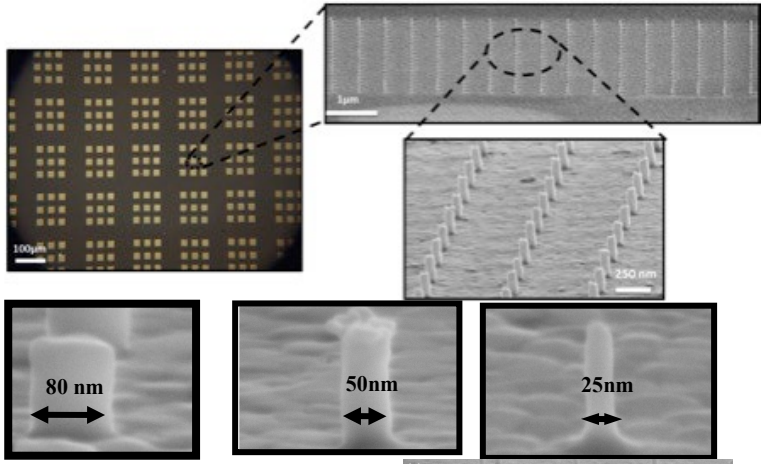
Versatile Process

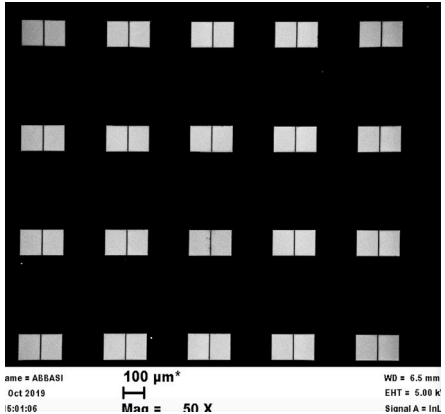
Print any Material at the Nano or Micro Scale on any Substrate

5 µm silver lines variable spacing

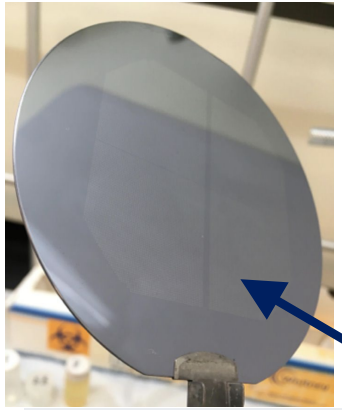
Printed Copper interconnects

Printed Crystalline Au & Ag

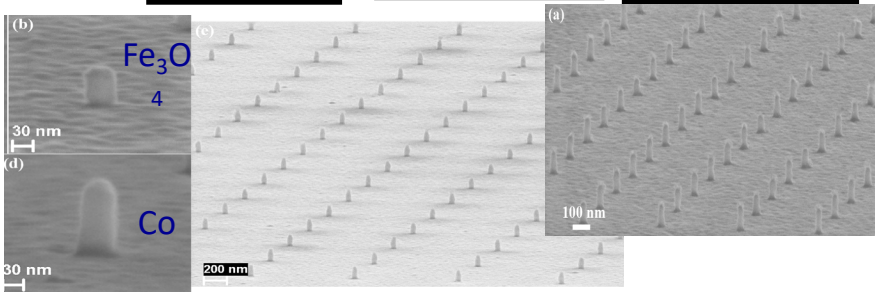




- Metals pads Silver



- 4 inch wafer



Magnetic memory (MRAM) applications

Prints one layer per wafer in one minute

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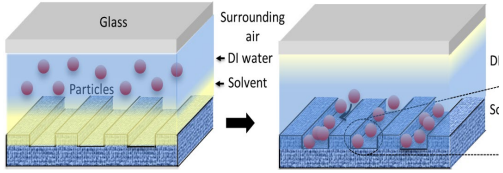
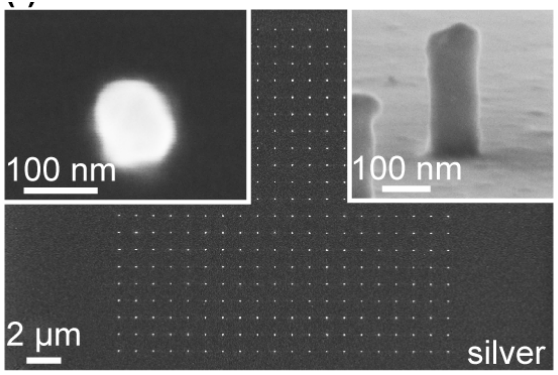
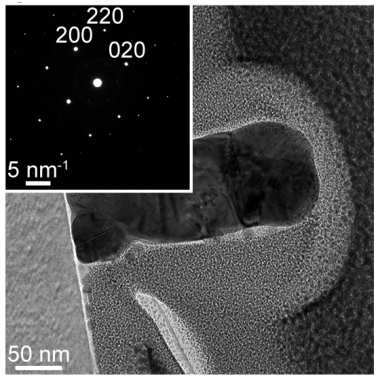
Printing of Single Crystal Semiconductor and Metal Micro and Nano Structures

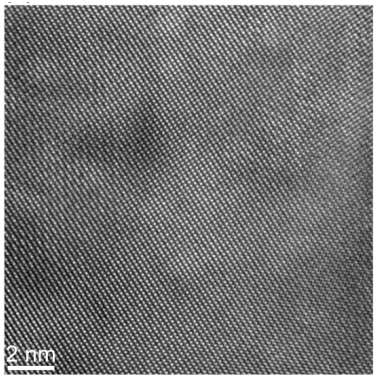
Convective Interfacial Assembly



Advanced Materials, 2020.

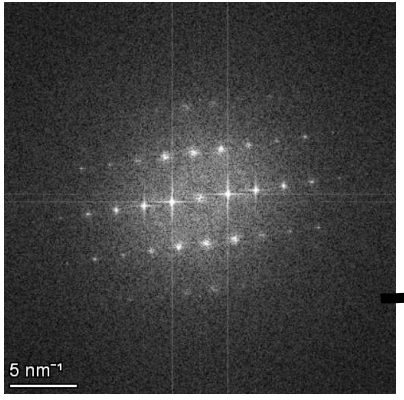


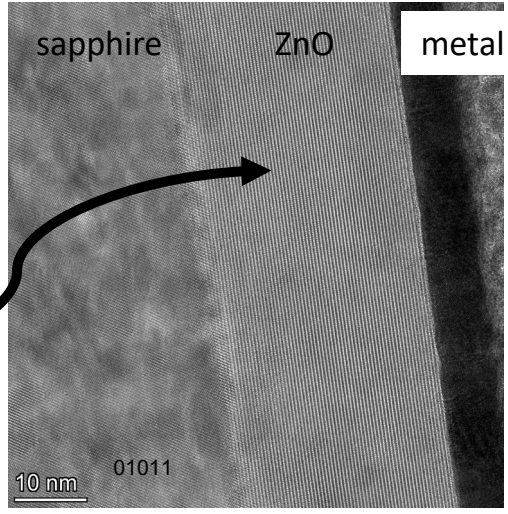




Room temperature annealing to make single crystal metal (Ag) nano structures

TEM of annealed printed ZnO nanoparticles





RTP annealing of II-VI nanoparticles on sapphire gives a single crystal structure throughout.

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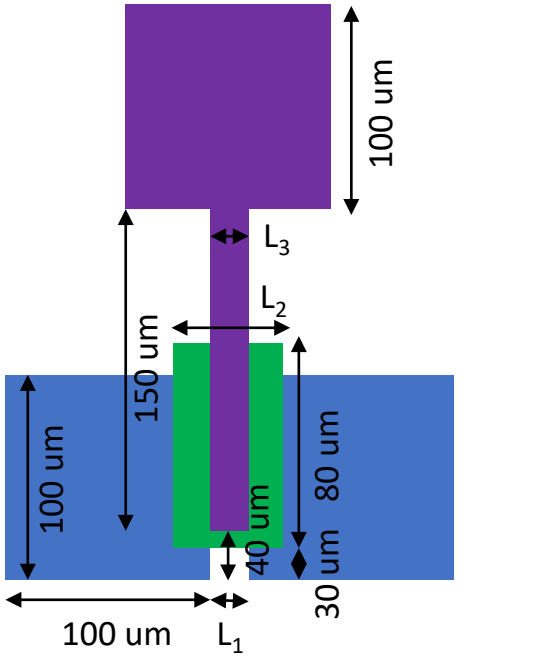
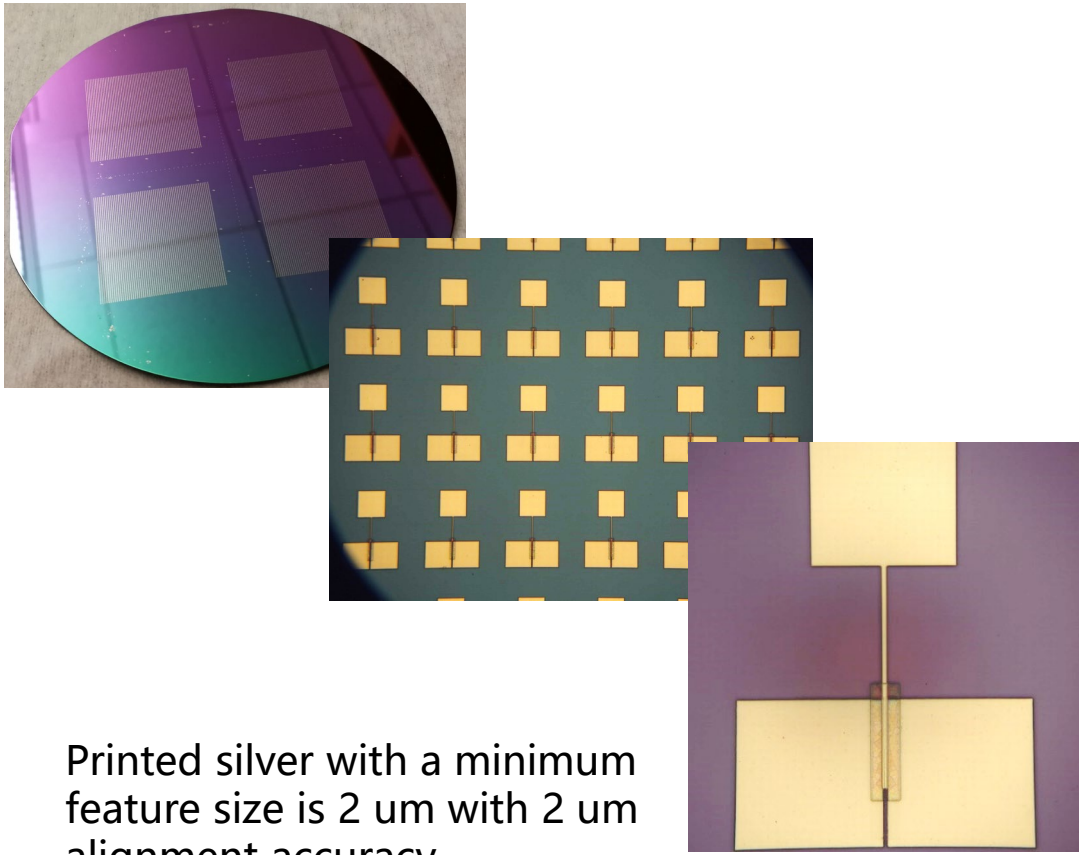
Printed Three Aligned Layers on Silicon Wafers



Source/drain electrodes, silver

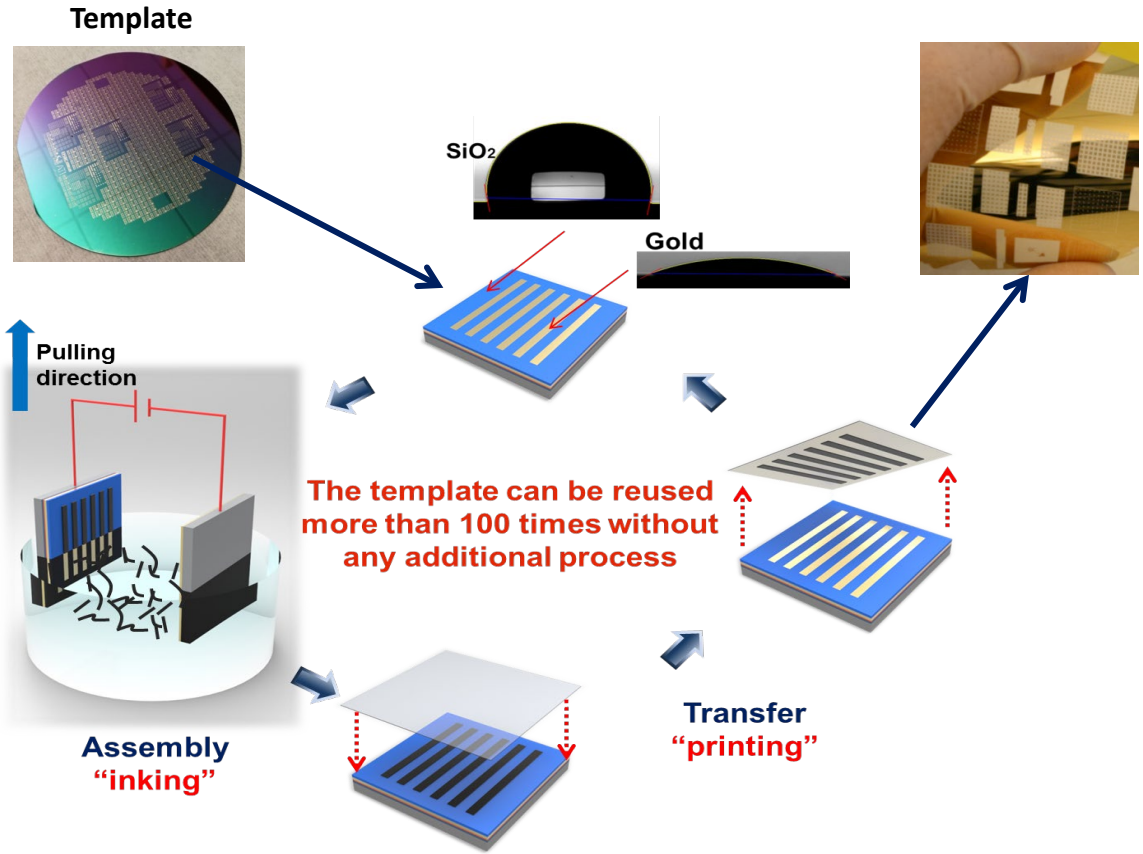
Dielectric, silicon dioxide

Gate electrode, silver



Printed silver with a minimum feature size is 2 um with 2 um alignment accuracy

Electrophoretic Assembly (EPx Platform) for Flexible Electronics



- Additive
- High throughput
- Prints down to 20nm
- Room temperature and pressure
- Prints on flexible or hard substrates
- Multi-scale; nano to macro
- Material independent
- Very low energy consumption
- Very low capital investment

Advanced Materials, 2015, 27, pp. 1759–1766.

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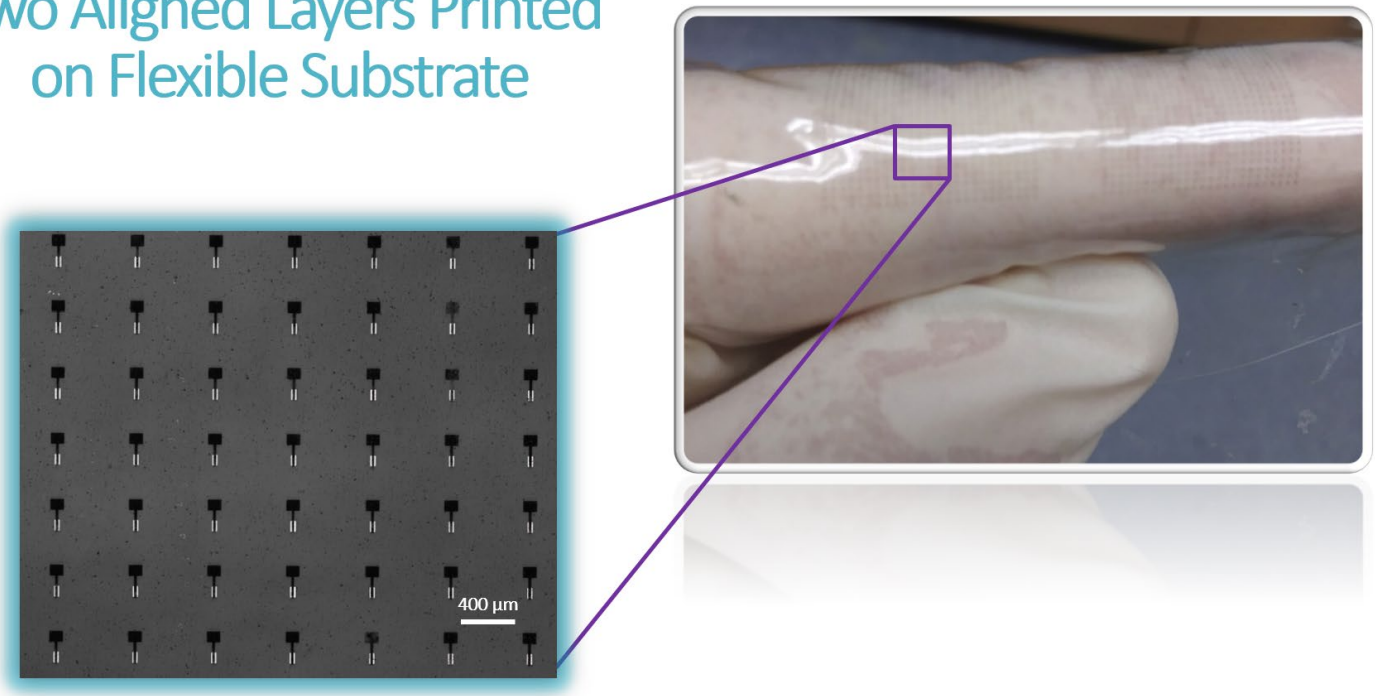
Printed Two aligned layers on Flexible Substrates (Polyurethane)

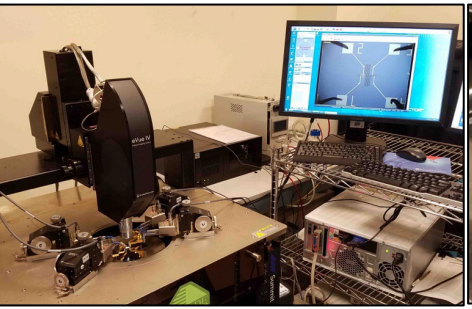
Two Aligned Layers Printed on Flexible Substrate

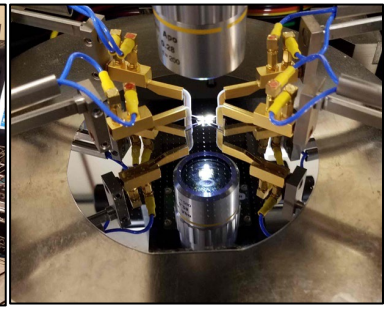


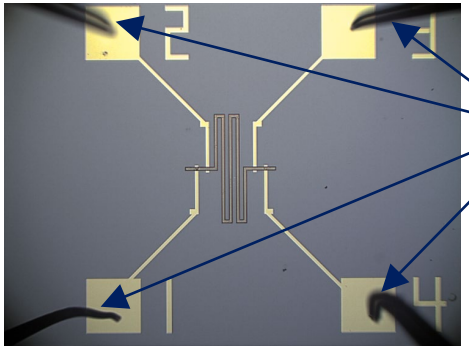
Aligned metal (silver) light color and polymer (dark color) on Polyurethane minimum feature size is 5 um with 2 um alignment accuracy

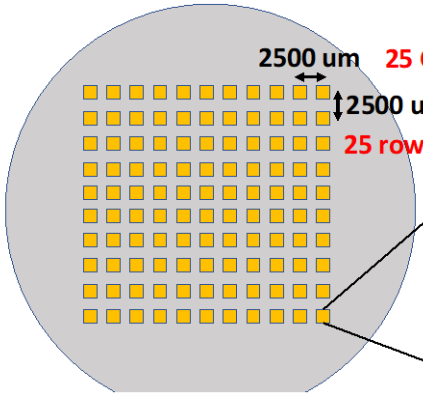
Applications

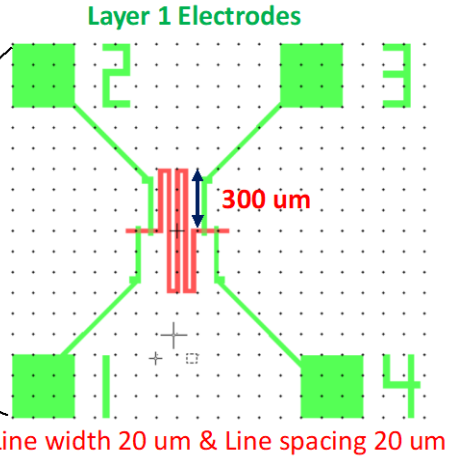
The Resistivity of Printed Metal Lines (Silver)

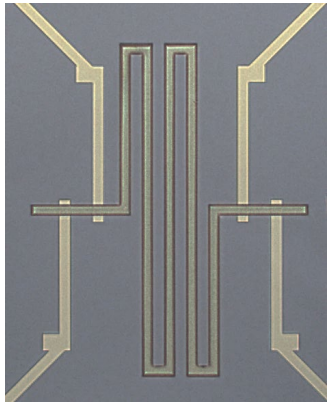












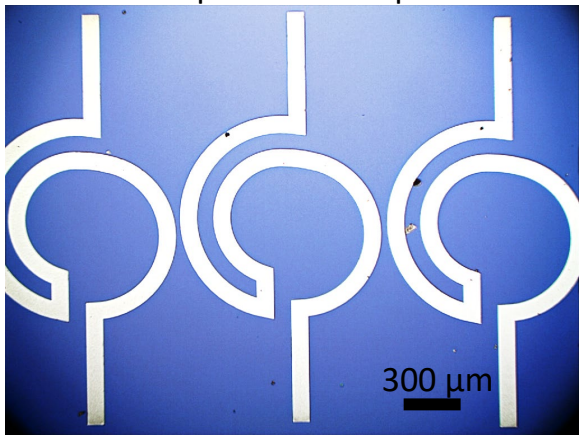
- Resistivity measurements of 3,125 printed patterns over five different substrates.
- It shows that the resistivity is about 2X of the bulk resistivity.

Printing of Metals

- Different materials has been optimized and printed on flexible and rigid substrates on large scale:

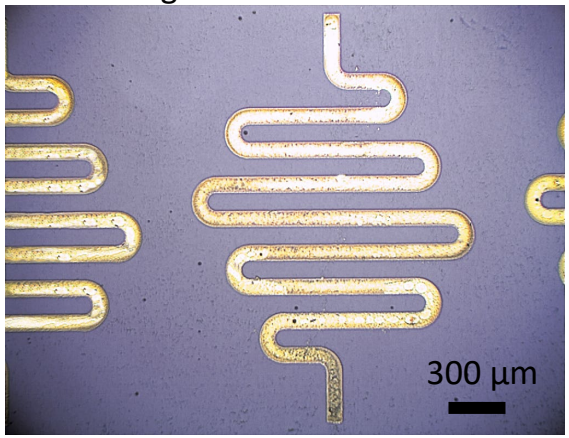
Platinum metal printing

Source: **nanoComposix** (Aqueous based Pt ink)



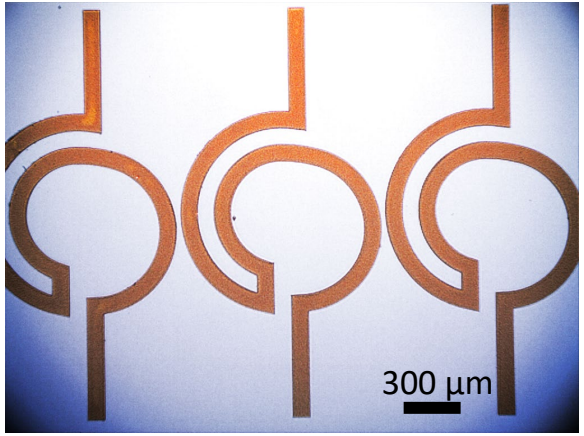
Gold metal printing

Source: **nanoComposix** (Aqueous based Au ink)



Copper metal printing

Source: **Novacentrix** (Organic based Cu ink)



Silver metal printing

Source: **Novacentrix** (Diethylene glycol-based Ag ink)

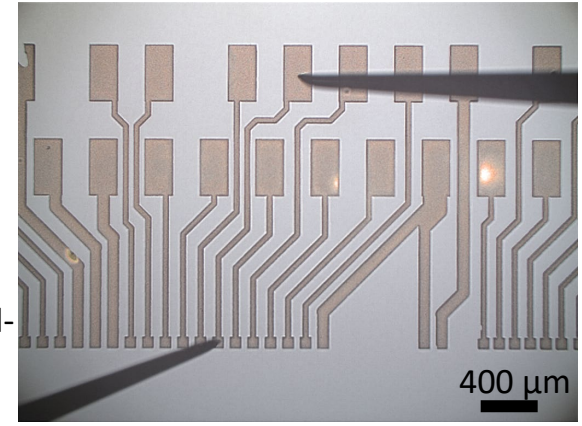
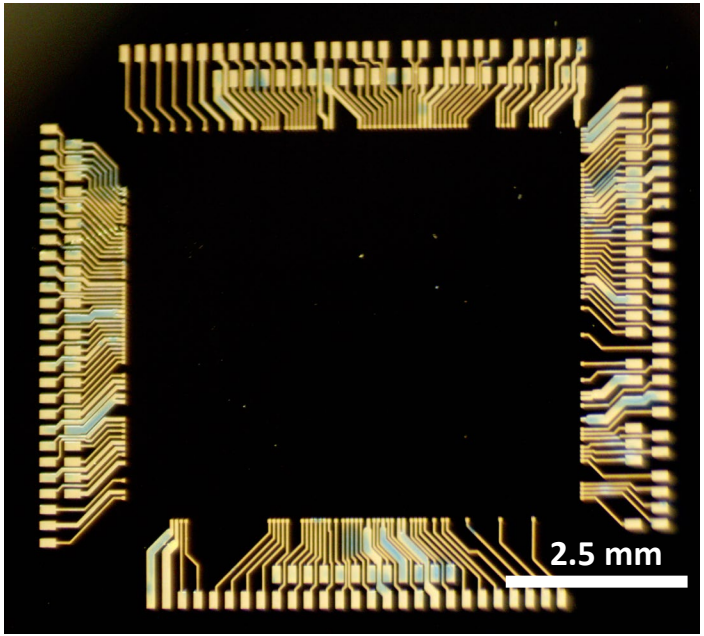
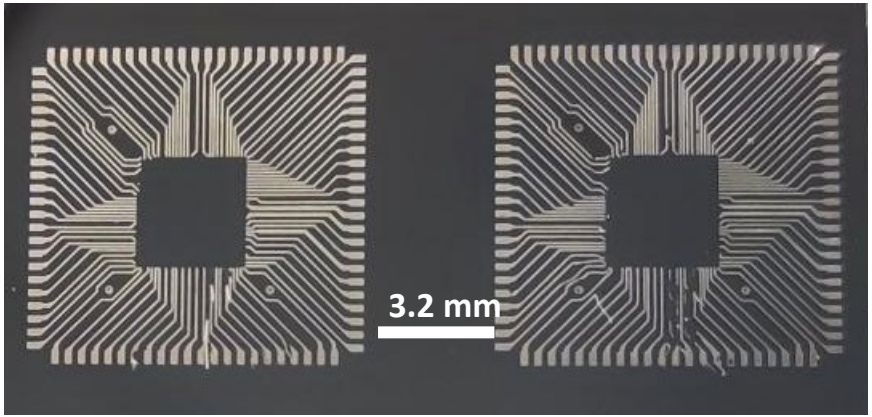


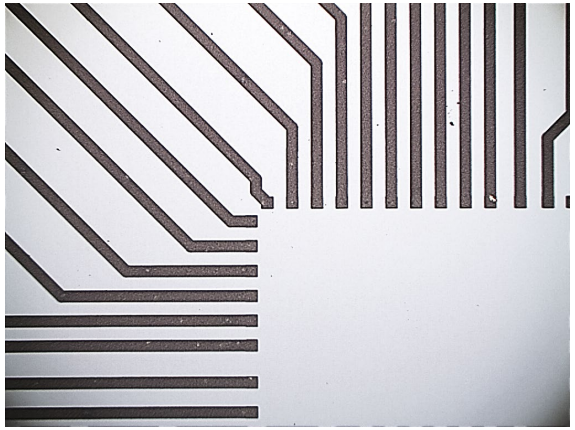
Photo Image of Flip Chip Fan Out Pattern

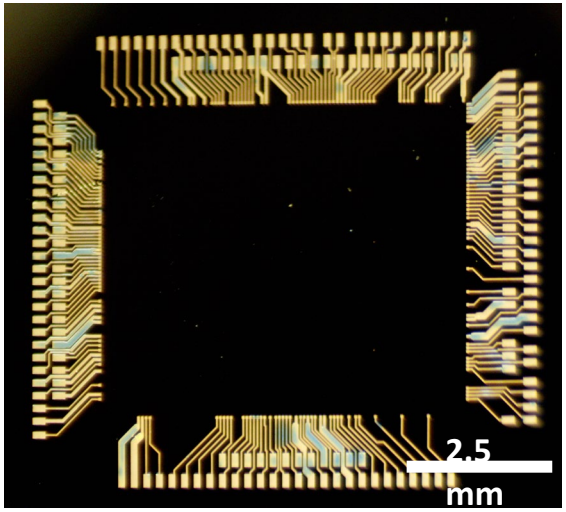
Printed Silver Flip Chip Fan Out Patterns

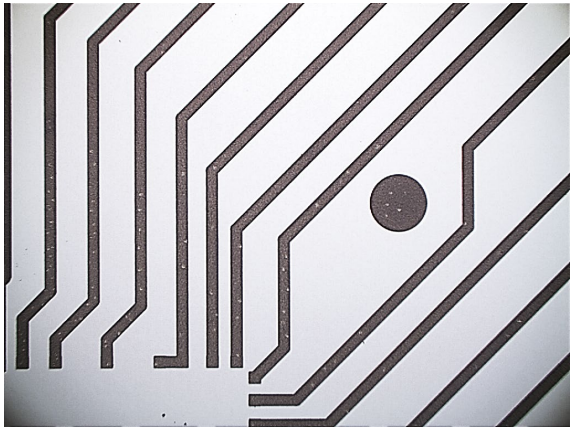


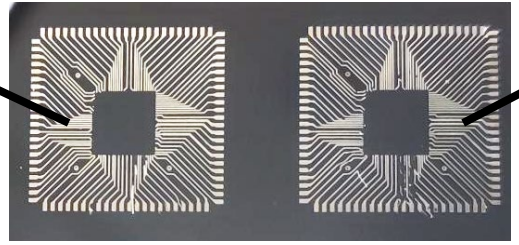


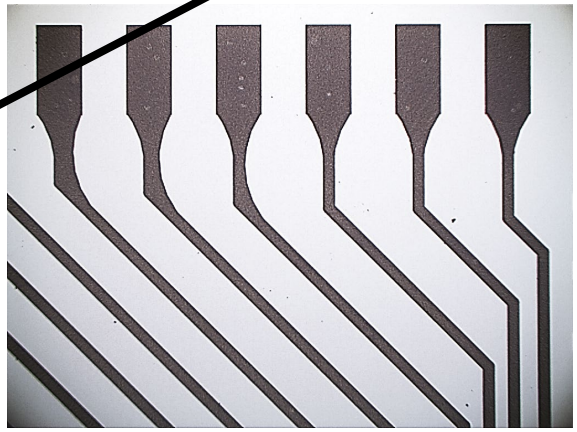
Flip chip images









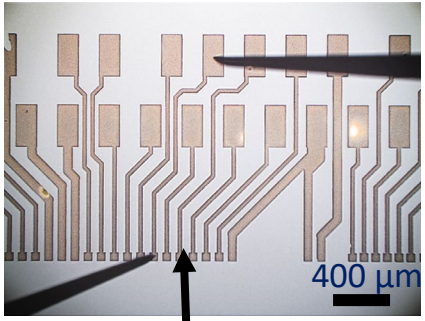


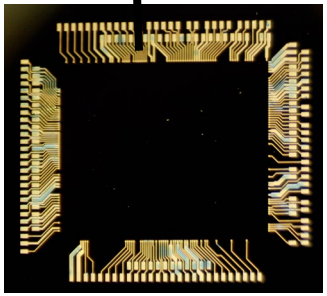
Printed Silver Flip Chip Fan Out Patterns

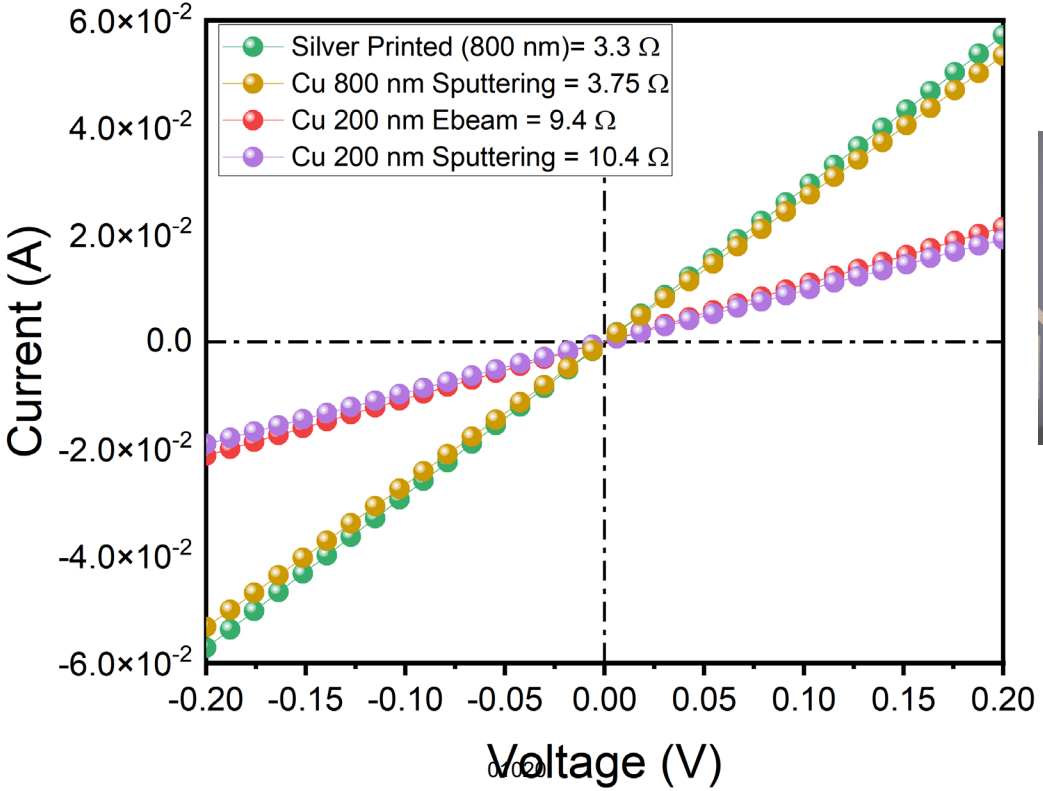
Printed Tracks

- The Flip chip pattern was printed using silver.
- The tracks conductivity is equivalent to vapor deposited copper at the same thickness.

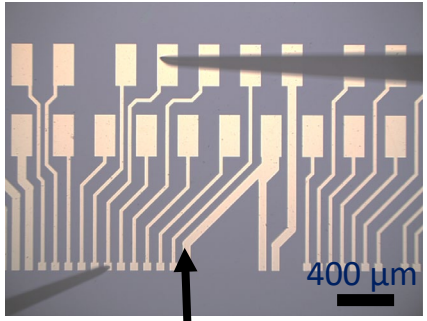
Silver (printed)

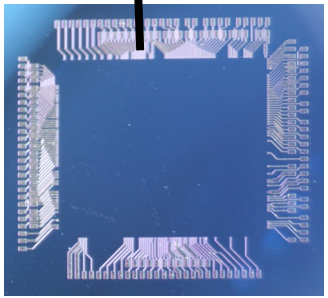






Copper (E-beam)

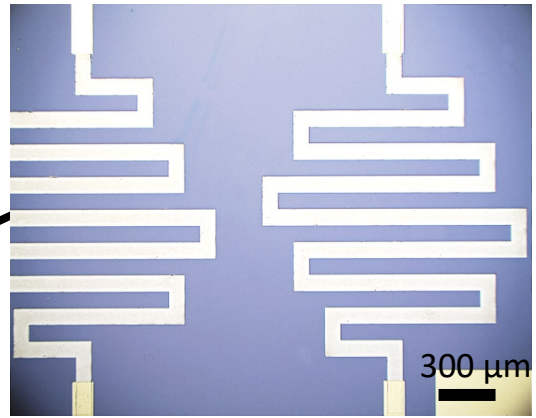


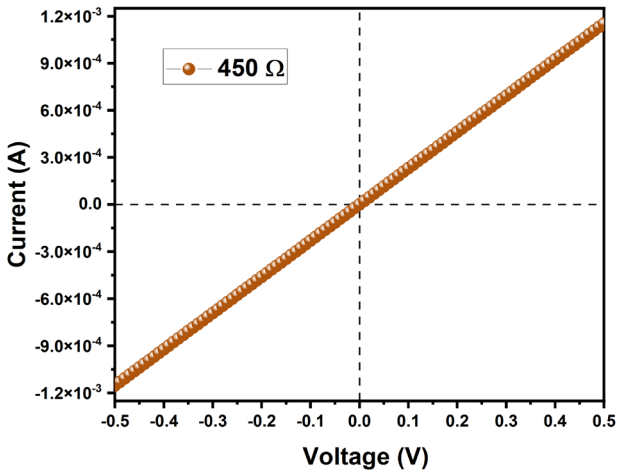


Devices Characterization: Resistors

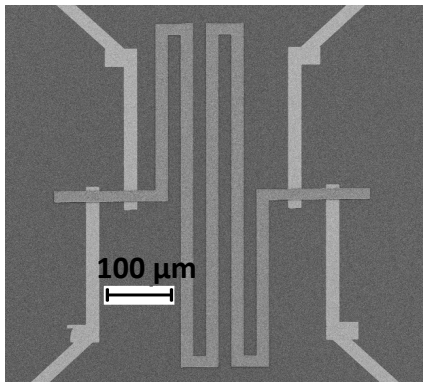
Metal film resistors

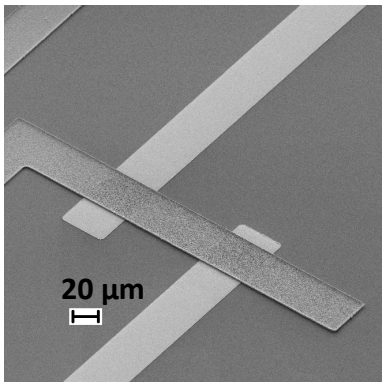
Printed Pt thin film resistors

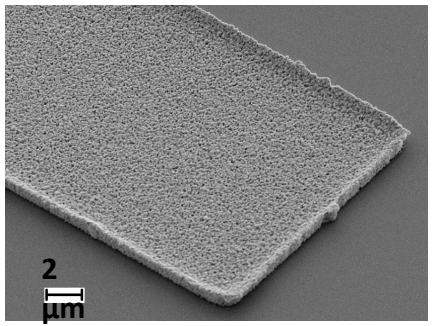


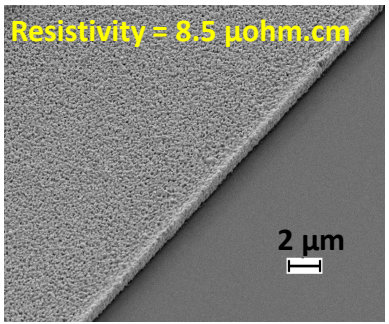


Metal film resistors



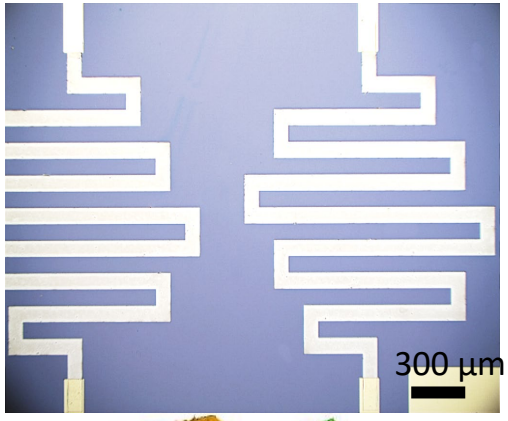


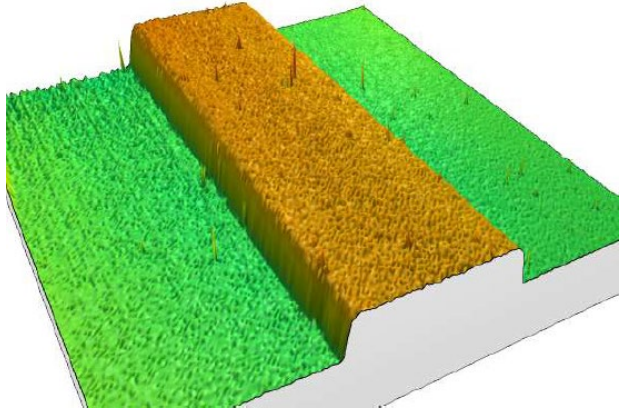


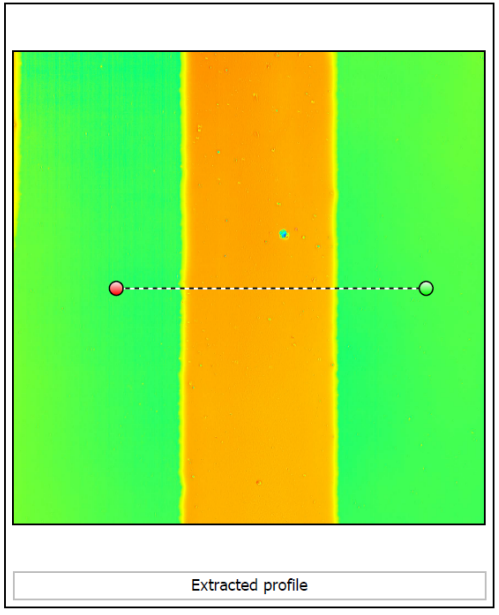


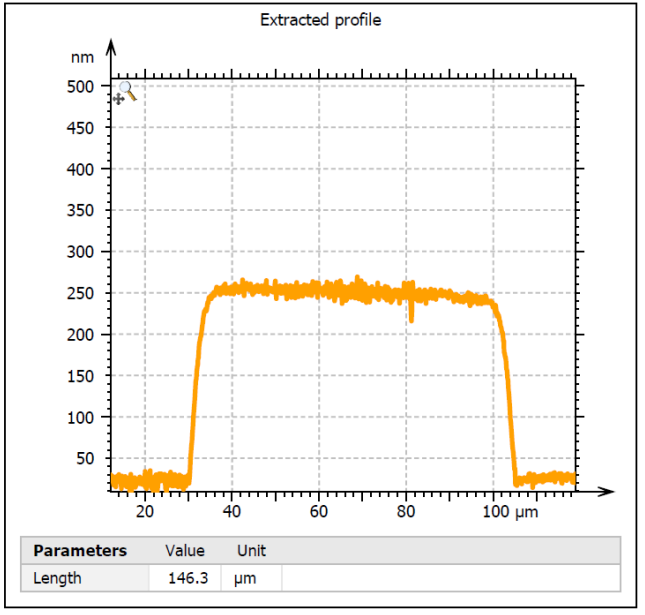
Printing of Platinum

- Confocal microscope measurements show an average thickness of 250 nm after annealing using RTP at 800 °C for 2 mins .





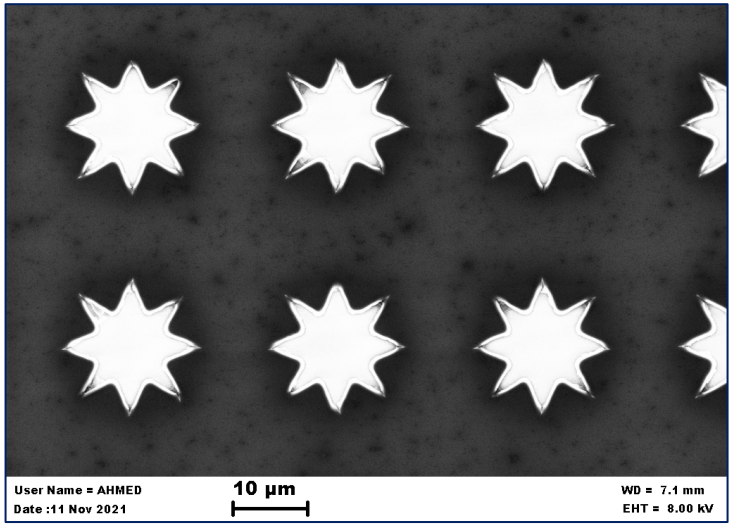


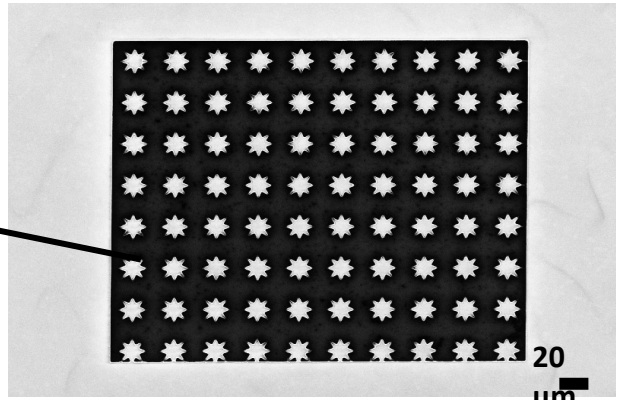


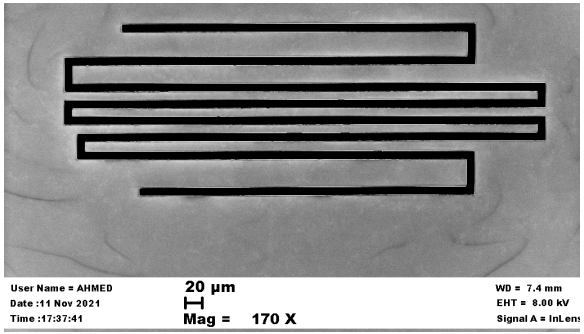
The printed pattern shows uniform and homogeneous surface morphology.

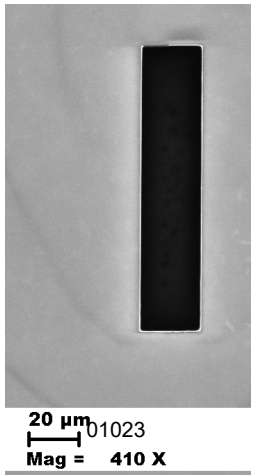
Printing of Dielectrics

- The SEM images below shows micropatterns printed using directed fluidic assembly.





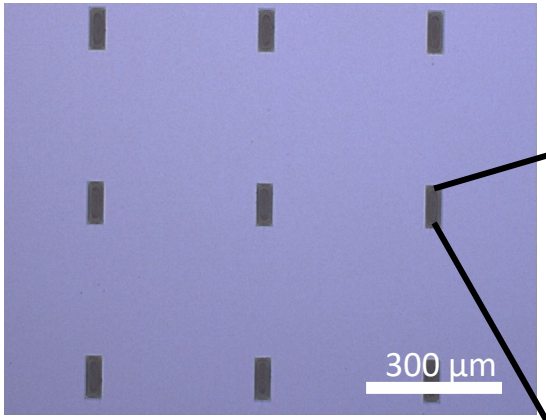




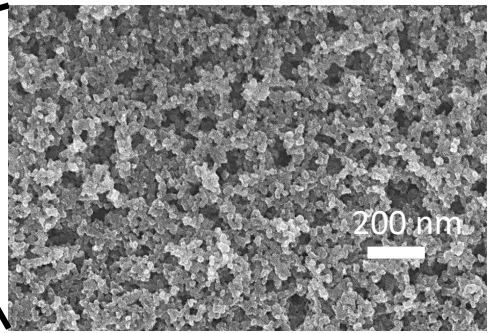
Dielectric channels
(10x200 microns and 50 nm thick)

Printing Resistors

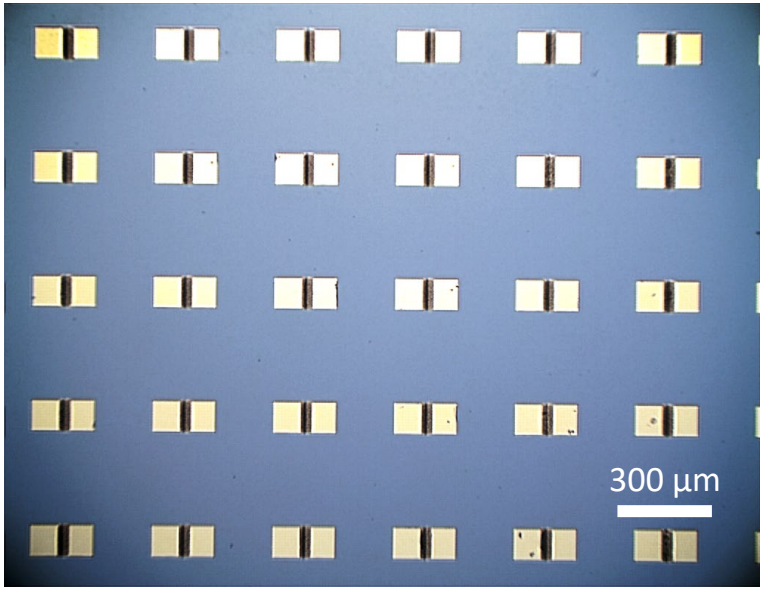
Carbon film resistors



Carbon nanoparticles film



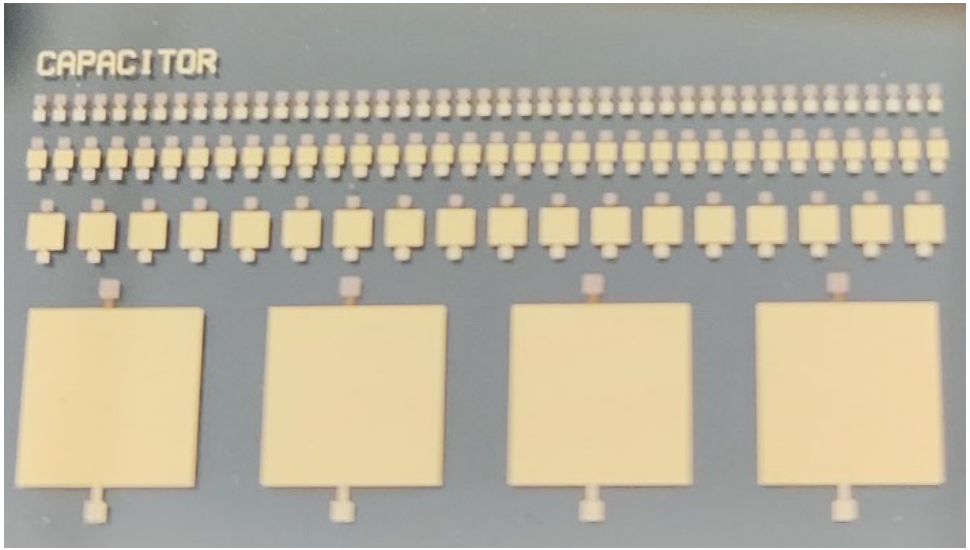
Carbon film resistors after Au contact

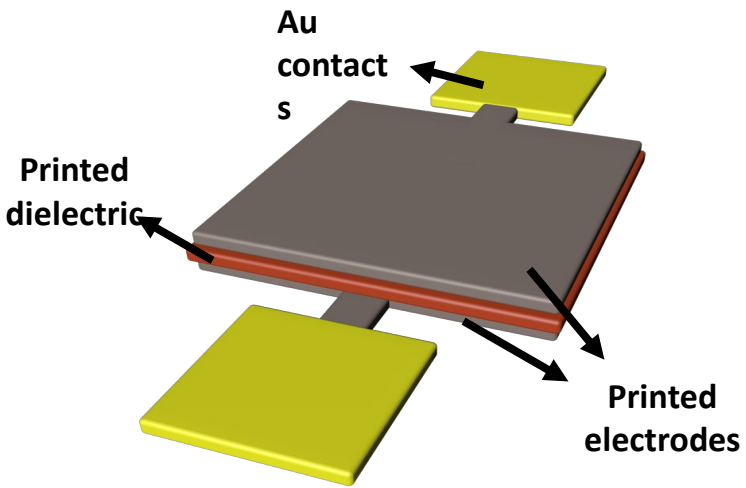


10 K Ohm Printed Carbon thin film resistors
(40x100 microns and 0.3 micron thick)

Printing of Capacitors

- **The optical image below shows the printed capacitor after Printing.**

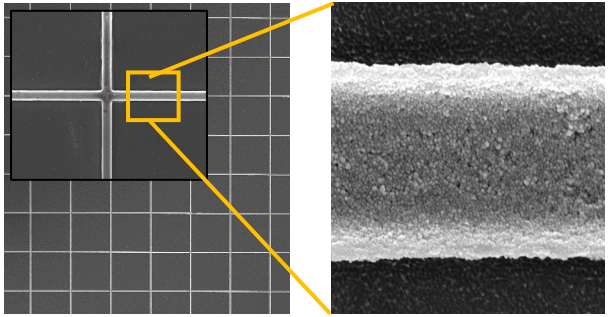




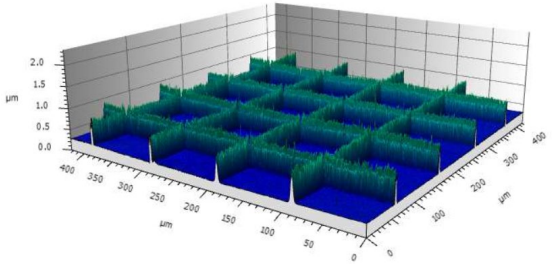
01025

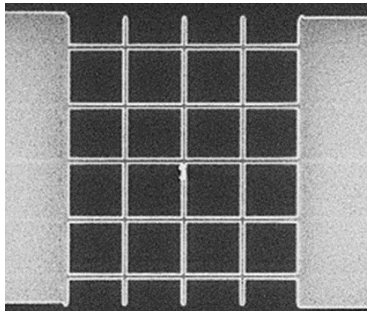
Printed Touch Screen with High Fidelity at the Micro and Nanoscale

Printed Ag grids for touch display applications

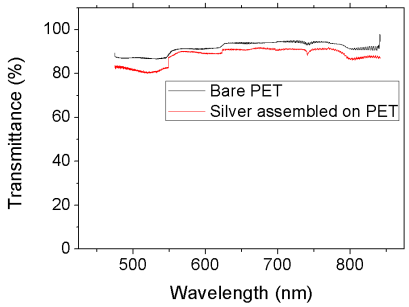


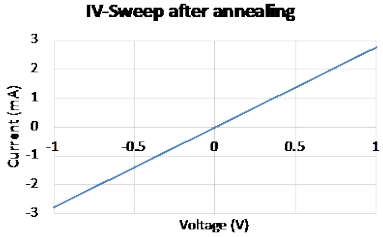
Line width 2 um

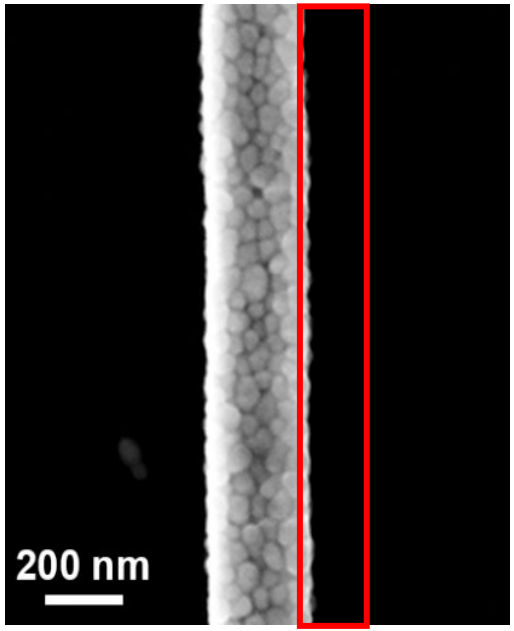




Line width 300 nm







Excellent Line edge roughness
3.7 nm
Using large nanoparticles

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Scalable Printing of High-Resolution Flexible Transparent Grid Electrodes Using Directed Assembly of Silver Nanoparticles

*Salman A. Abbasi, Zhimin Chai, and Ahmed Busnaina**

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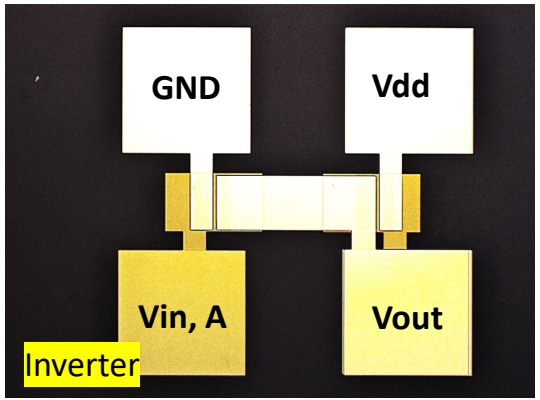
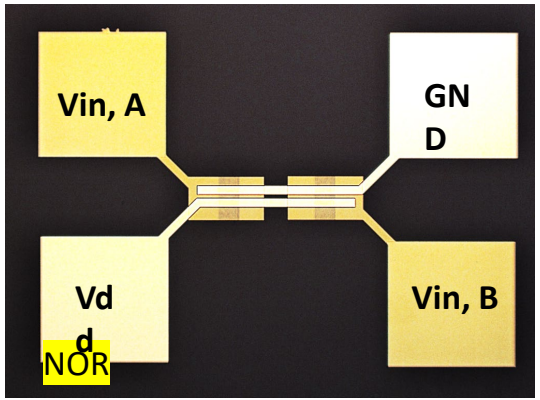
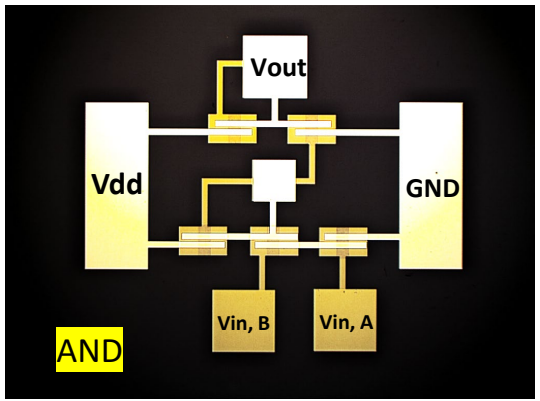
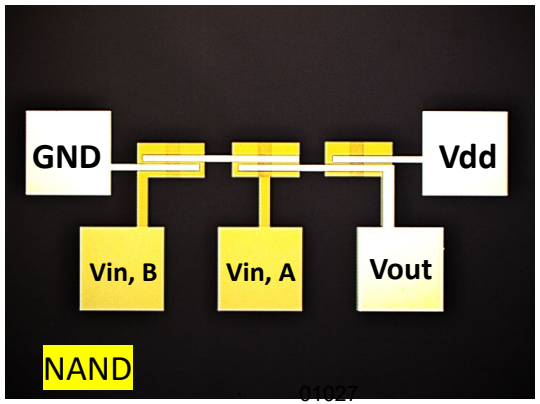
Logic Gate Electronics

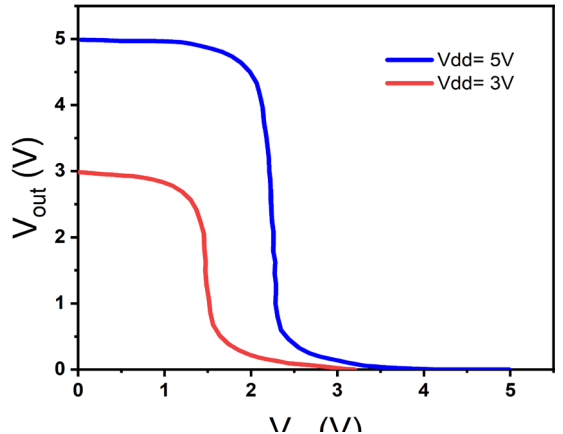
- Logic gates such as Inverters, AND, NAND, and NOR were fabricated based on SWCNTs FETs
- The figures below show the fabricated logic circuits

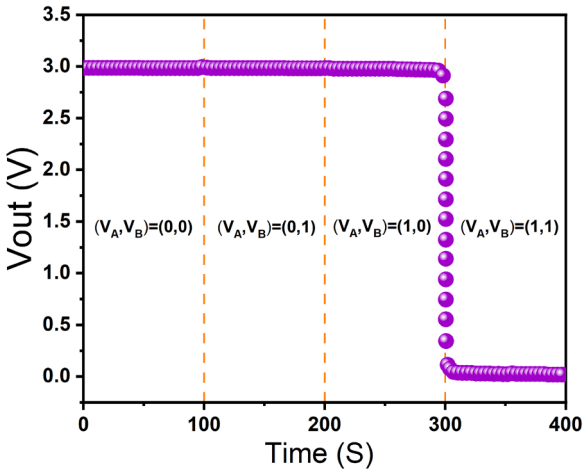




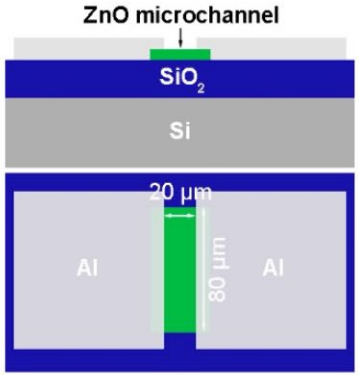


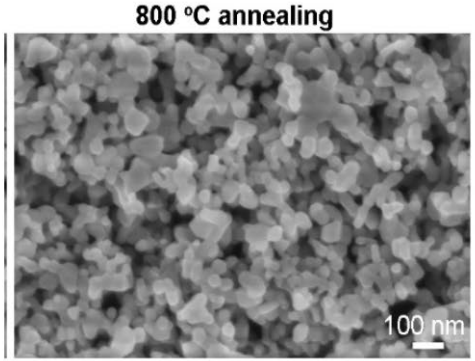


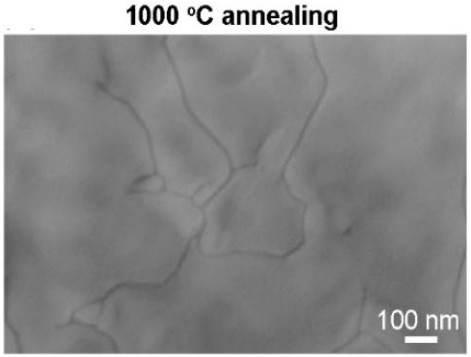


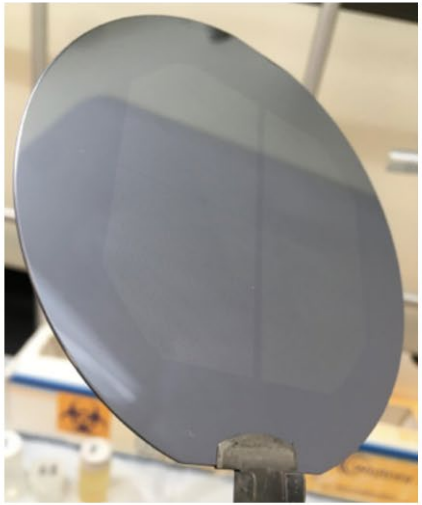


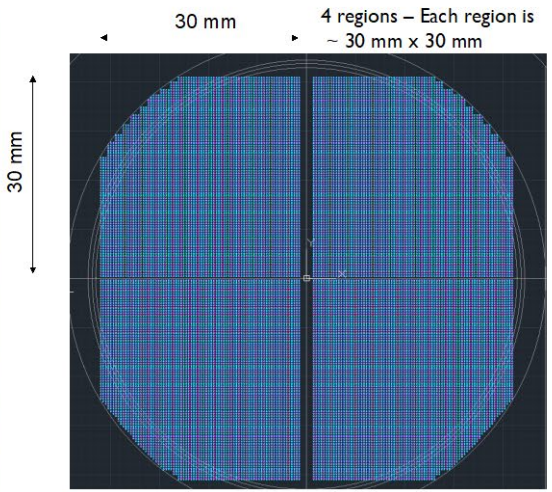
Field Effect Transistor (FETs) Using II-VI Semiconductors

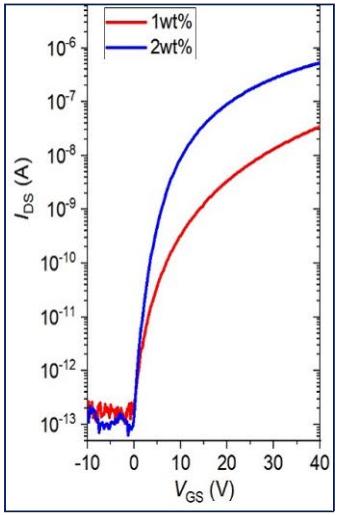












01028

Wafer level printing of 37,000 transistors exhibiting an on/off ratio higher than 10^6 after annealing.

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Scalable Fully-automated Fab-in-a-Tool

- Nano OPS has licensed exclusive rights to 35 inventions.
- Nano OPS is introducing two fully-automated a Fab-in-a-Tool platforms:
  - FLEX RD: designed to print flexible electronics at sub-micron scale.
  - FFx RD800: Can take a CAD file and deliver a completed product at sub-micron scale.
- Turnkey device fabrication incorporating **transistors, inverters, capacitors, diodes, inductors, photonic devices, and sensors for IoT, 5G, wearables, etc.**
- Secure (trusted) foundry service for feasibility studies and production (from zero trust to full trust).

Fab-in-a-Tool

Nano OPS©

The Future of Electronics Manufacturing

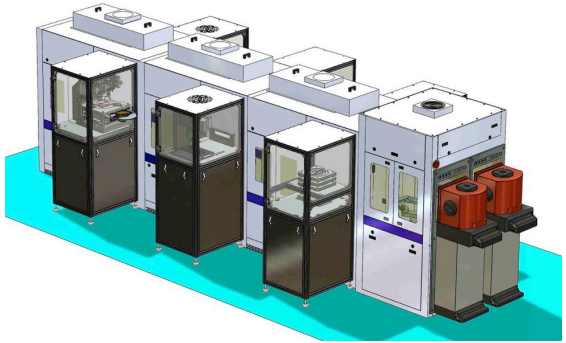
Any Material
Any Substrate

Minimum Feature Size
20 nm

High throughput
10 – 100x Faster

Cheaper 10 – 100x

Fab-in-a-Tool: A Fully Automated Nanoscale Electronics Manufacturing Platform



35 patents that cover printing, electronics and sensor applications.

The Future of Electronics Manufacturing

Fab-in-a-Tool Platform Advantage:

- ✓ Feature size comparable to advanced electronics manufacturing technology at 20nm
- ✓ 5 – 10x reduction in capital equipment cost as compared to current factories;
- ✓ 10 – 100x reduction in manufacturing cost compared to current technology;
- ✓ 10 – 100x faster as compared with current technology;
- ✓ 1000x reduction in materials use compared to current technology ;
- ✓ More than 1000x faster than inkjet or 3D printing;
- ✓ Prints crystalline metal and semiconducting structures at room temperatures.
- ✓ eliminating 100s of process steps;
- ✓ expanding material choices for specific design needs.
- ✓ Patented technology for printing nanometers to several hundred microns.
- ✓ From zero trust to full trust.