High-density Fan-Out Chip on Substrate using M-Series™ and Adaptive Patterning® Technology

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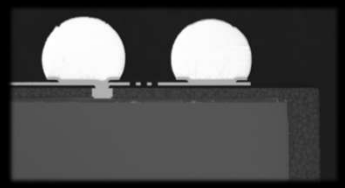
Agenda

- Introduction
- Industry Perspective
- Challenges & Solutions
- Design Study
- Conclusion

DECA Company introduction

- Deca was born of a passion to transform electronic interconnect with inspiration from SunPower's advanced solar wafer fab
- Our name describes our culture of 10X thinking, inspired by *Greek déka* (δέκα)
- Deca created 10X breakthroughs with M-Series™ & Adaptive Patterning®

1. 

*M-Series**

Chips first, chips up fan-out technology

Gen 1 & Gen 2

2. Adaptive DP™ Patterning

*Adaptive Patterning**

Real-time optimized design during manufacturing (every device on every wafer)

Now the industry's #1 fan-out technology

Over 3.5 million devices shipping per day in Q1'22

Note: Deca holds > 100 issued and pending patents on M-Series, Adaptive Patterning and related technology

Deca is Owned by Industry Leading Companies

Largest shareholder

Deca's Shareholders
(Equity owners of Deca)

Smallest shareholder

Infineon

Qualcomm

ASE GROUP

nexes

maxeon
POWERING POSITIVE CHANGE

DECA Employees

Board of Directors

Sam Geha – Chairman
Larry Michlovich - Director
Previously CYPRESS PERFORM

Shankar Ekambaram - Director

Rich Rice – ASE Director

Tae-Hoon Kim - Director

Neal Bergstrom (observer) *Previously* SUNPOWER

Tim Olson – CEO Director

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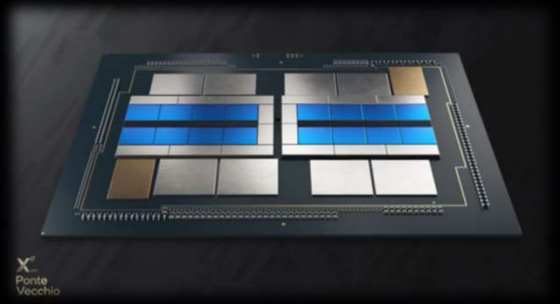
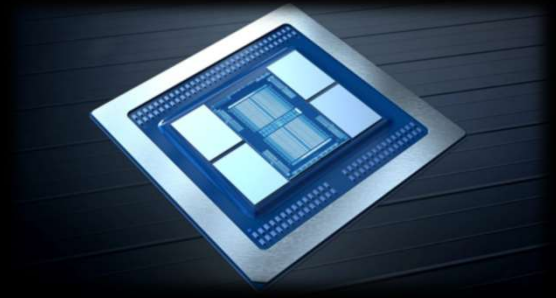
The future is now…



"…Ponte Vecchio Xe-HPC GPU, Over 100 Billion Transistors & 47 XPU Compute Tiles"

https://wccftech.com/intel-showcases-packaging-prowess-7nm-ponte-vecchio-xe-hpc-gpu-100-billion-transistors/

Intel's Ponte Vecchio



"AMD Radeon… with Chiplet Design"

https://www.hardwaretimes.com/amd-radeon-rx-7900-xt-rx-7800-xt-rx-7700-xt-to-leverage-tsmcs-5nm-6nm-node-w-chiplet-design/

AMD's Radeon

Chiplets are happening

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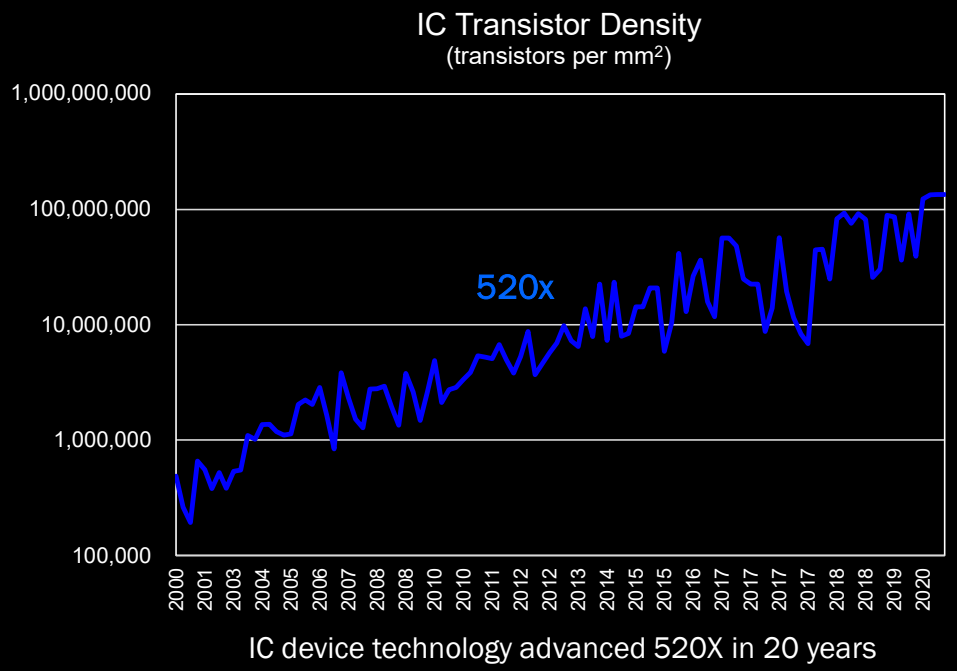
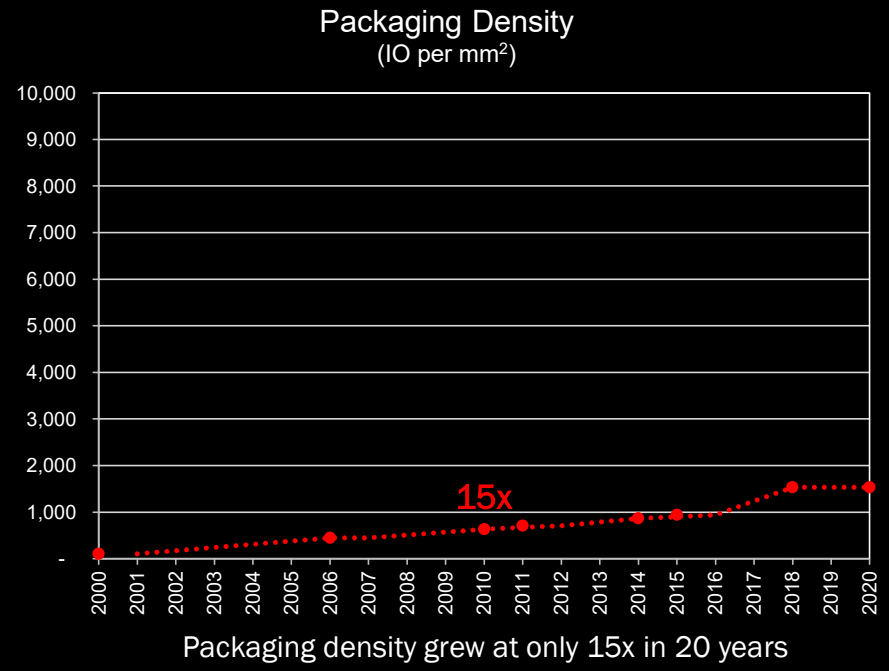
Challenge - Pitch Limitations

Packaging severely lagging semiconductor device technology (15x vs. 500x density increase in past 20 years)



IC device technology advanced 520X in 20 years

Source: Multiple industry sources compiled at en.wikipedia.org/wiki/Transistor_Count



Packaging density grew at only 15x in 20 years

Sources: 1. Chip scale Review: March-April 2020, IO/mm² derived from die pad pitch data
2. Tech Search Intl, Advanced Packaging Update, Vol 2, 2020

Packaging interface density orders of magnitude behind ICs

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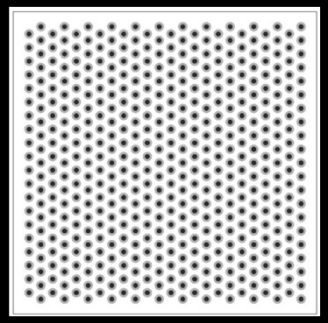
Challenge - Pitch Limitations

Industry leaders at 40µm to 45µm die pad pitch

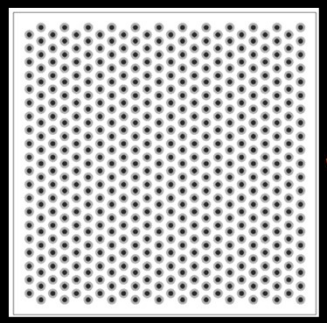
M-Series Gen 1
(Chips First Fan-out)



Die pad pitch: 45 µm
IO per mm^2: 492

Introduced in 2016

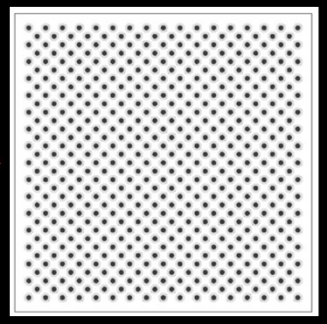
Intel EMIB
(Hybrid chips in substrate)



Die pad pitch: 45 µm*
IO per mm^2: 492

*45µm pitch reference: David Schor, Intel Unveils Foveros Omni And Foveros Direct; Leveraging Hybrid Bonding, WikiChip Fuse, July 26, 2021

TSMC InFO-R
(Chips First Fan-out)

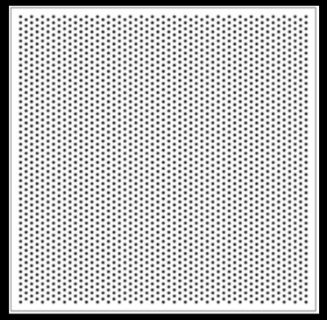


Die pad pitch: 40 µm
IO per mm^2: 545

*40µm pitch reference; Tom Dillinger, SemiWiki.com, Highlights of the TSMC Technology Symposium, 9/7/2020

Interface density

M-Series Gen 2
(Chips First Fan-out)



Die pad pitch: 20 µm
IO per mm^2: 2,518

Deca's Gen 2 delivers breakthrough 20µm die pad pitch thru Adaptive Patterning

5X interface density increase

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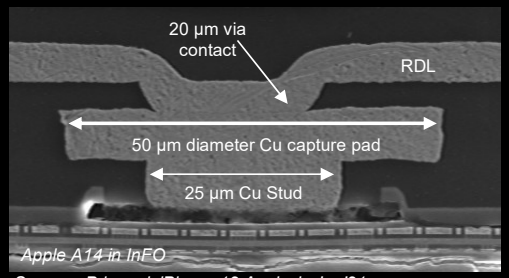
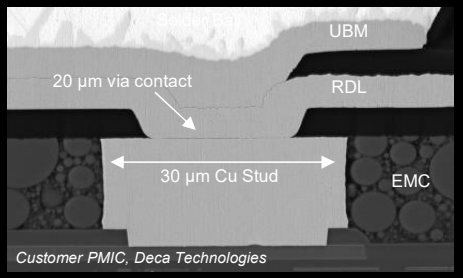
Solution – Eliminating the Capture Pad

Example – TSMC InFO



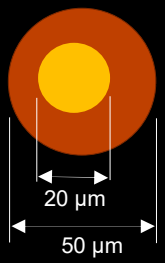
Source: Prismark iPhone 12 Analysis Jan'21

M-Series™ with Adaptive Patterning



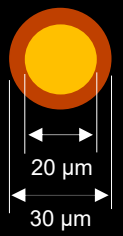
Source: Prismark iPhone 12 Analysis Jan'21

Via connection without Adaptive Patterning



Large Cu capture pad *(extra layer added to Cu stud)*

Via connection with Adaptive Patterning



Cu stud size *(no need for extra Cu layer)*

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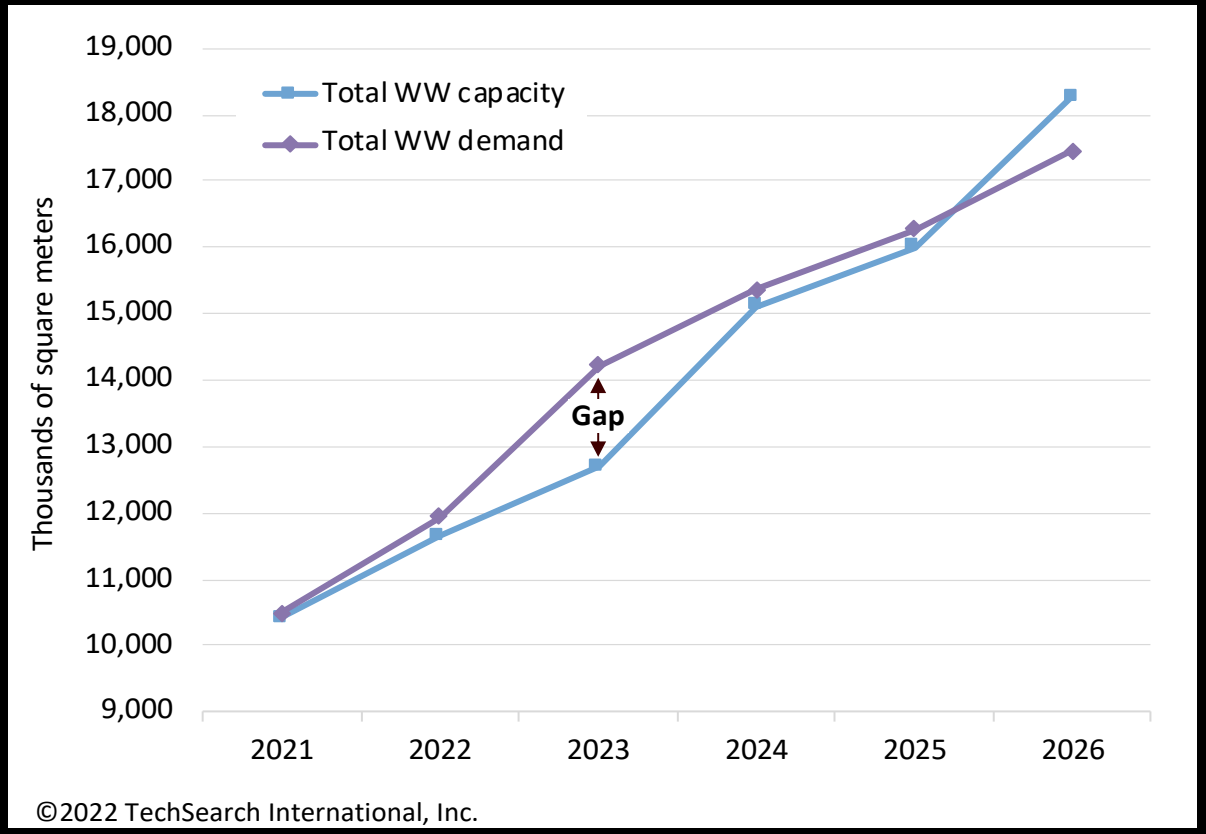
Obstacles - Substrate availability

Significant shortfall in advanced substrate capacity is forecasted to persist



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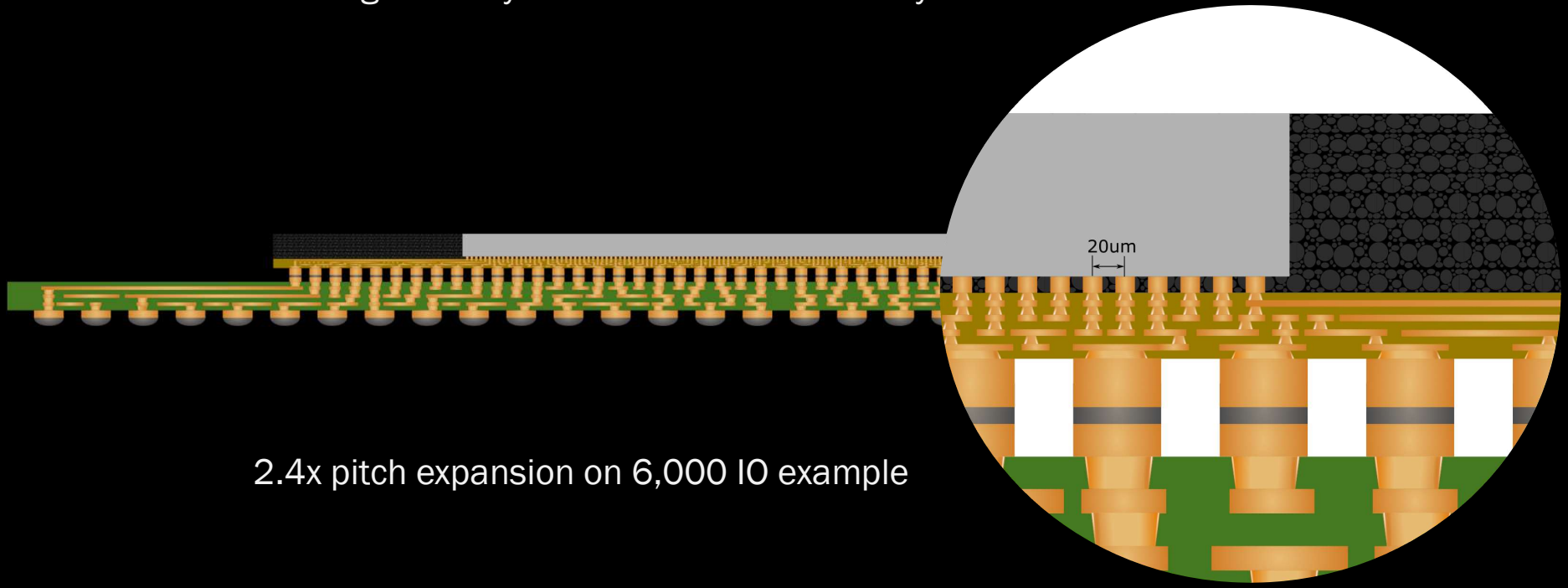
Solution – Simpler Substrates

FOCoS moves high-density interconnect to fan-out layers



2.4x pitch expansion on 6,000 IO example

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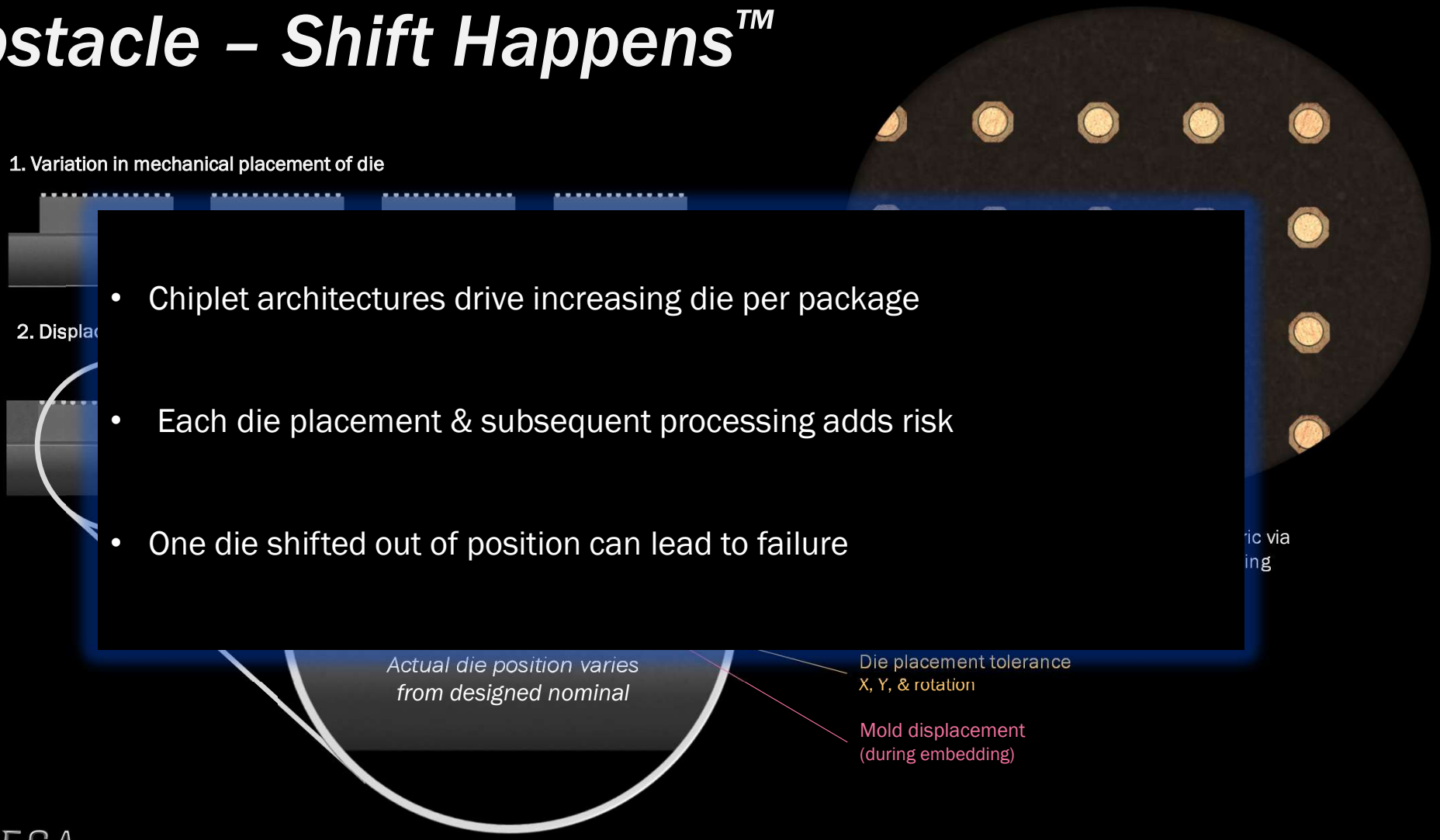
Obstacle – Shift Happens™



- Chiplet architectures drive increasing die per package
- Each die placement & subsequent processing adds risk
- One die shifted out of position can lead to failure

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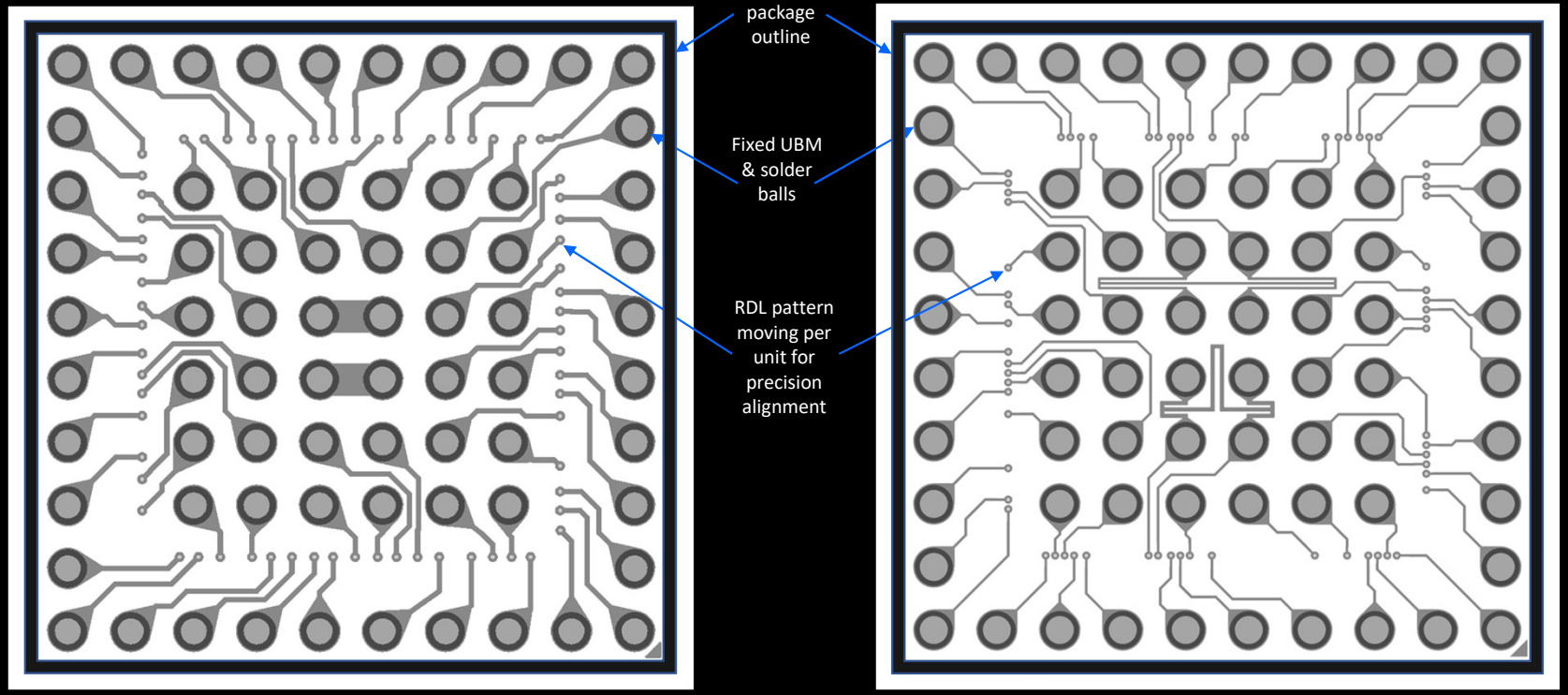
Adaptive Patterning Methods™

Adaptive Alignment

Translate & rotate entire RDL pattern to the measured die position

Adaptive Routing

Dynamically adapt small portion of RDL to the measured die position (s)



BGA array fixed to package outline – precise RDL pattern to die alignment

BGA array fixed to package outline – ideal for multi-die routing

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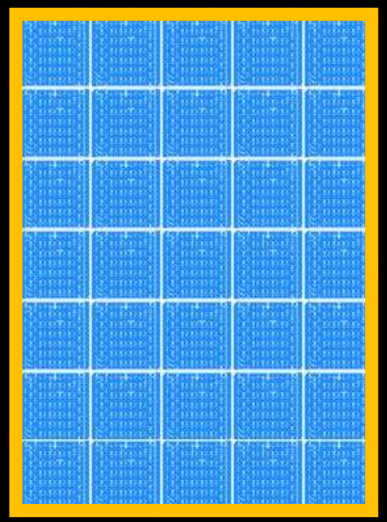
Note: Multiple patents issued & pending covering all facets of Adaptive Patterning

Obstacles - Reticle Size

- Reticle limits typically ~850mm^2
- Chiplet based devices often 36mm x 36mm (1,296mm^2) and larger
- Reticle stitching required – technically feasible, commercially unattractive

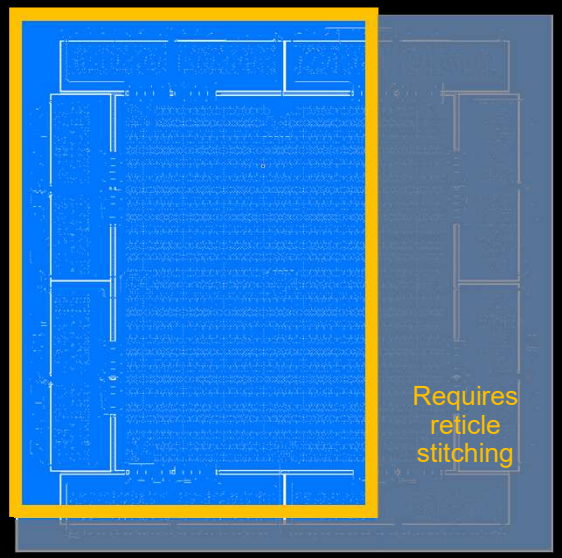
5x5 mm Device

Devices within reticle



36x36 mm Device

Beyond reticle size



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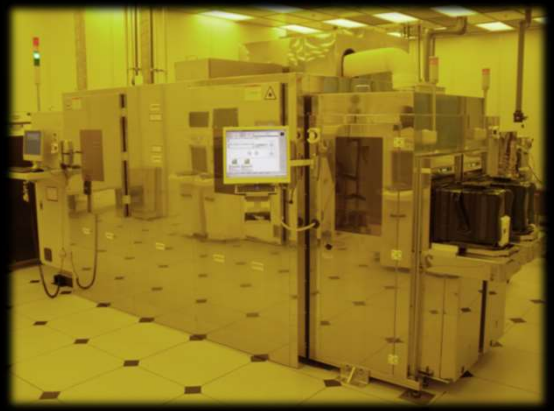
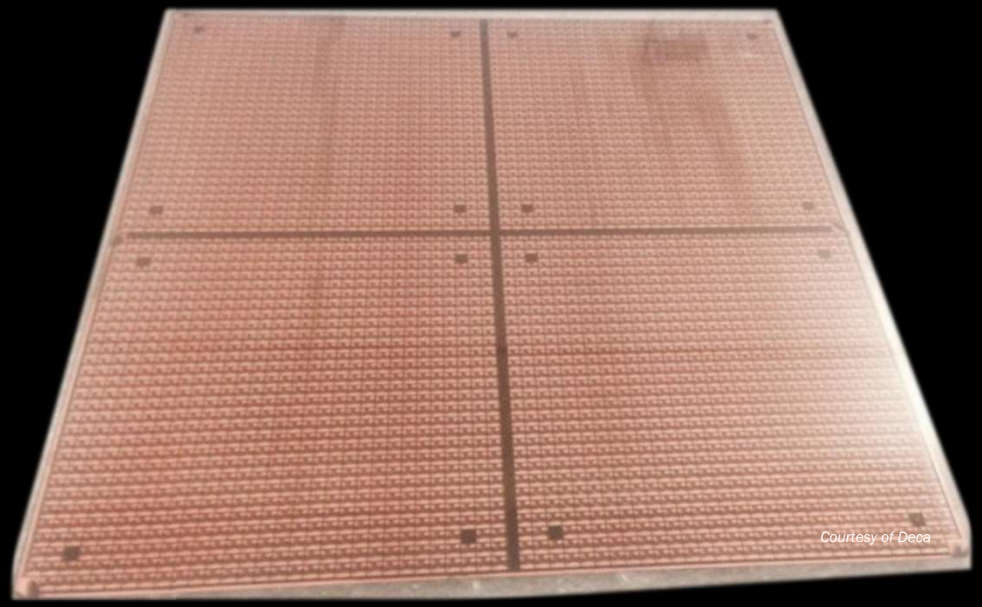
Solution – Eliminate the Reticle



Mask-less LDI lithography system

Large Panel Production



600mm x 600mm square panel

Adaptive Patterning utilizes fully digital lithography – no glass photomasks are used

Entire 300mm round or 600mm square panel is a single exposure field

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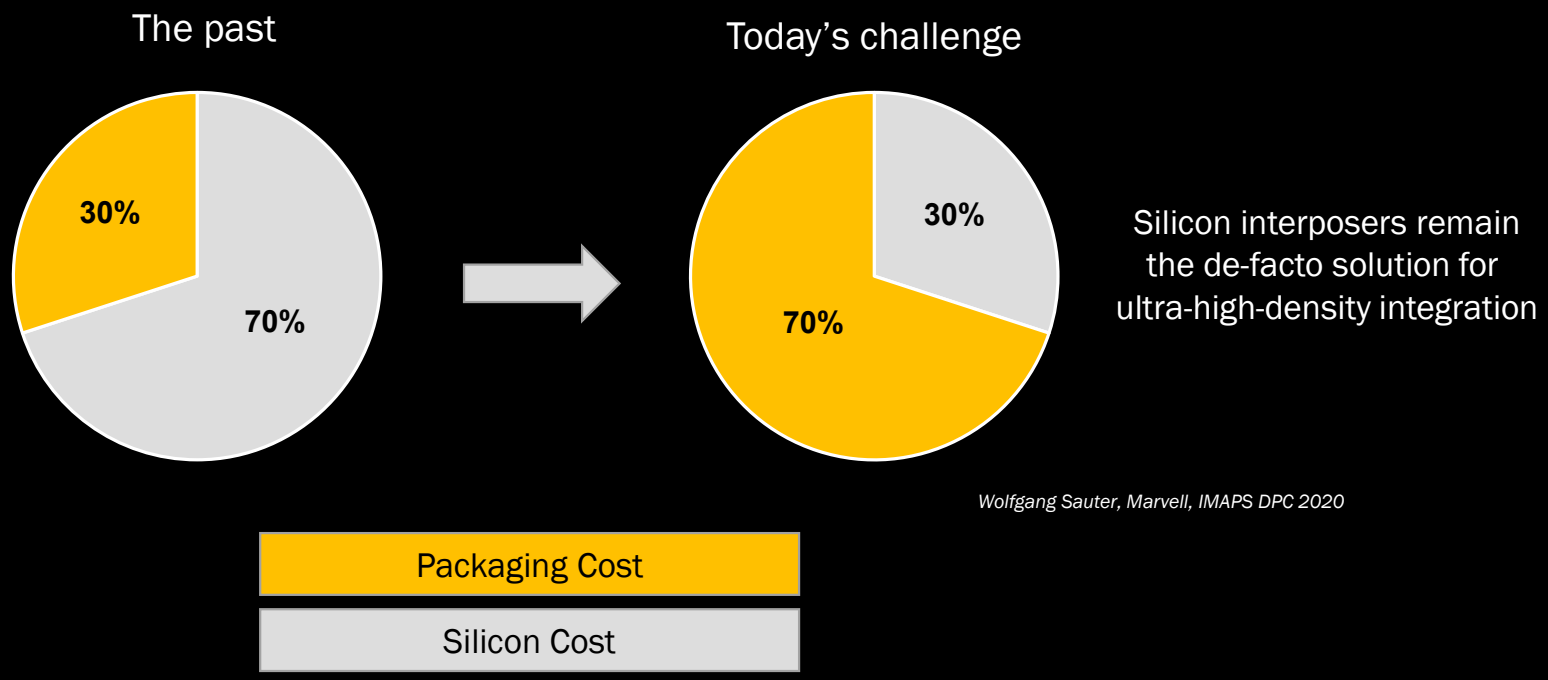
Obstacles - Cost

Next generation packaging technologies demand costly materials and processes



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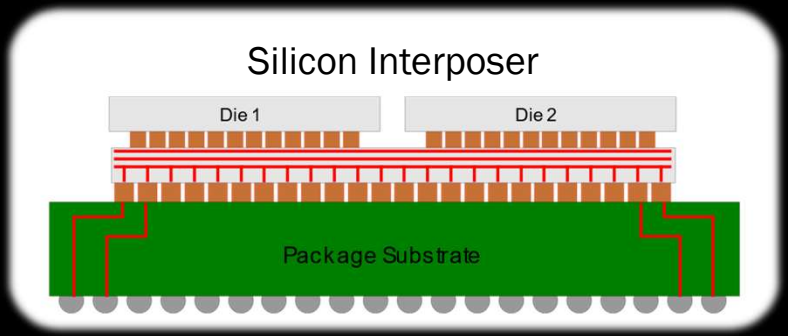
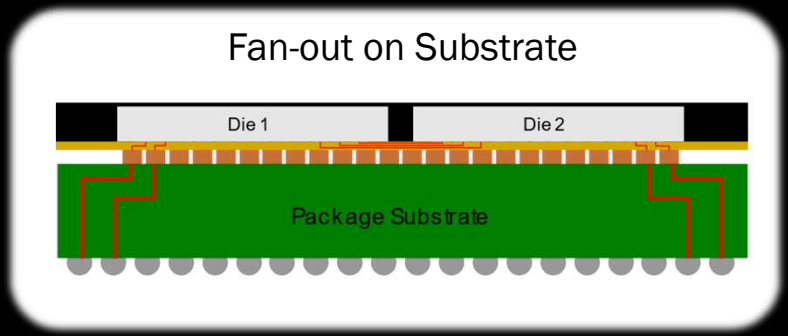
Solution – Eliminate the Si Interposer

Ultra-high-density organic solutions are positioned to replace Si interposers





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Obstacles – Emerging Proprietary Solutions

Established independent supply chain for semiconductor packaging through the OSATs

ASE GROUP

Amkor Technology®

JCET

PTI Powertech Technology Inc.

TF 通富微電 TONGFU MICROELECTRONICS CO., LTD.

However, latest advanced packaging technologies emerging from proprietary sources

intel®

tsmc

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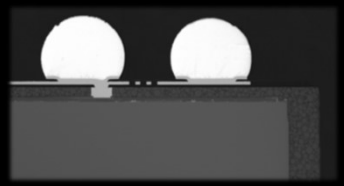
Solution – Independent Advanced Technology

Ready access to advanced packaging technology – Deca's proven solutions



M-Series Fan-out

Chips first, chips up fan-out technology

Gen 1 & Gen 2

Adaptive Patterning™

Adaptive Patterning*

Real-time optimized design during manufacturing (every device on every wafer)

Deca's current licensees

ASE GROUP 日月光集團

nepes corporation

skywater

And growing…

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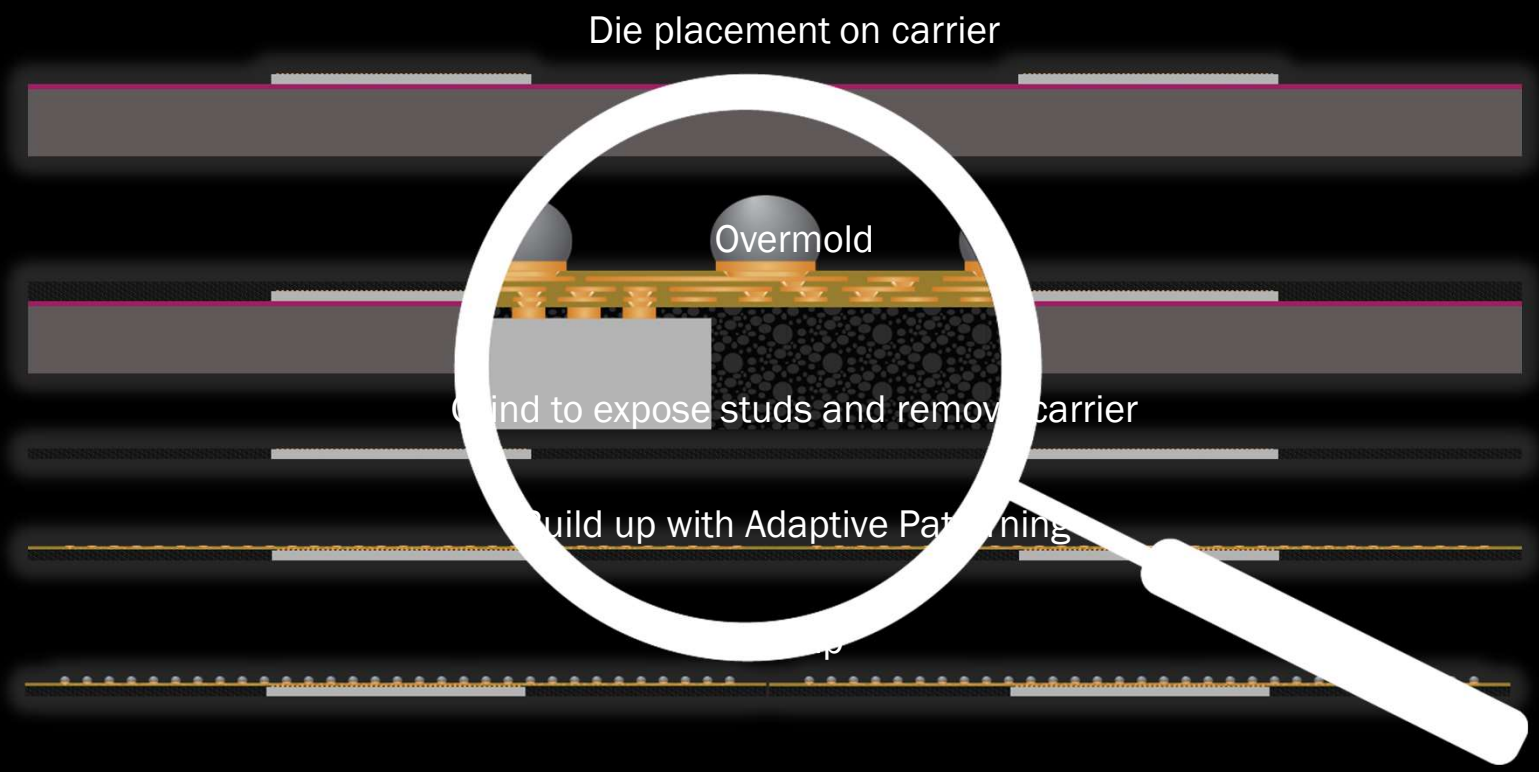
Solution – A Simple Process

M-Series chips first face up advanced fan-out technology



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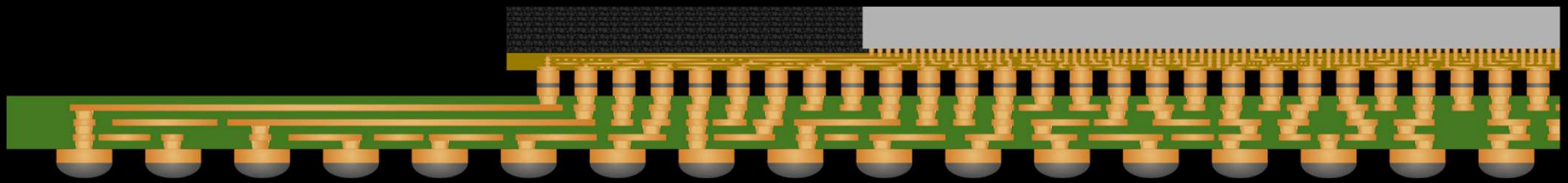
FOCoS Design Study

FOCoS moves high-density interconnect to fan-out layers



- 14mm x 16mm finished device
- 6,000 die pads with 2.4x expansion

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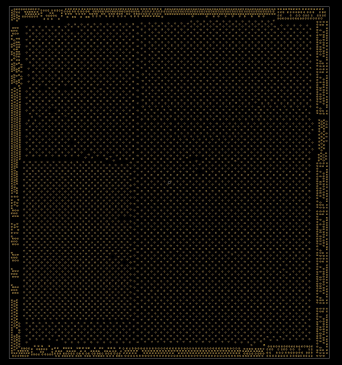
FOCoS Design Study

Die specifications

- 4nm silicon
- 12mm x 13 mm
- 4500 core pins – 150 µm pitch
- 1500 periphery pins – 90 µm pitch

Die



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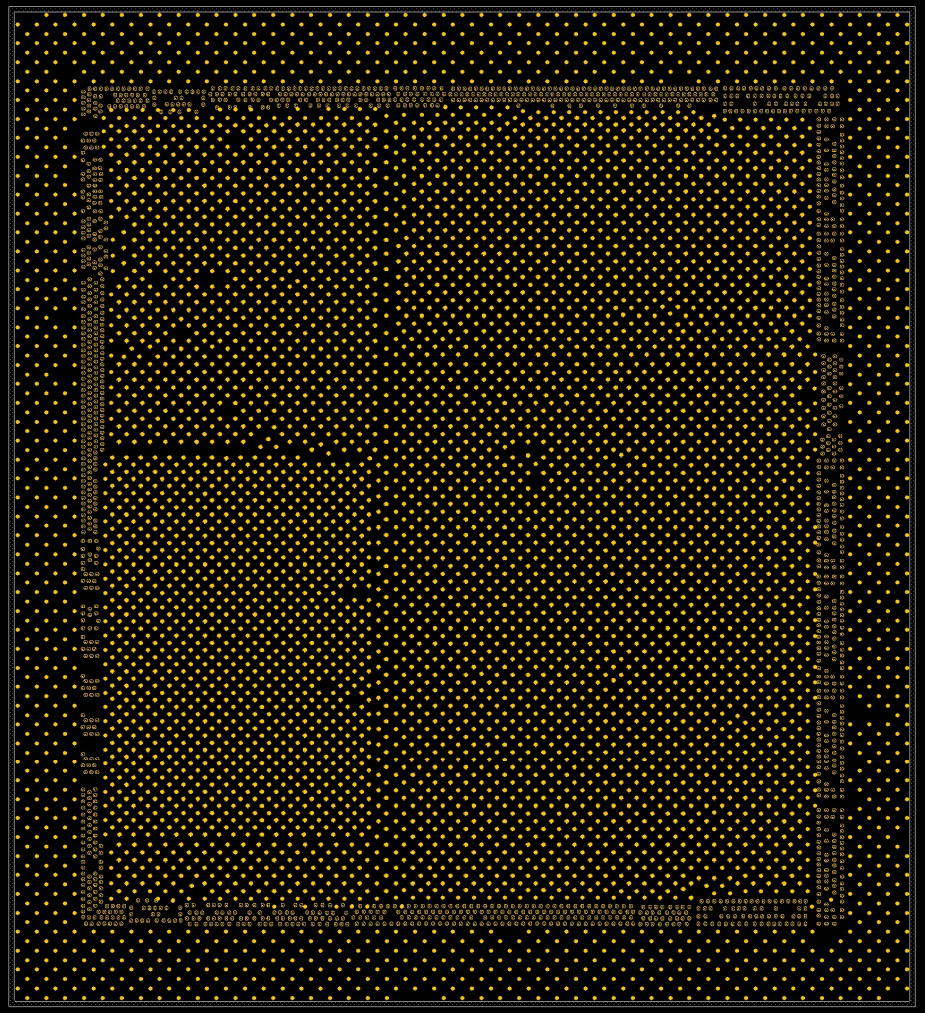
FOCoS Design Study

Molded M-Series Package

- 5 µm minimum trace & space
- 14 x 16 mm
- 1 routing layer
- 4500 core pins – 150 µm pitch
- 1500 periphery pins – 212 µm pitch

FOR = 1.44

Fan-Out Ratio



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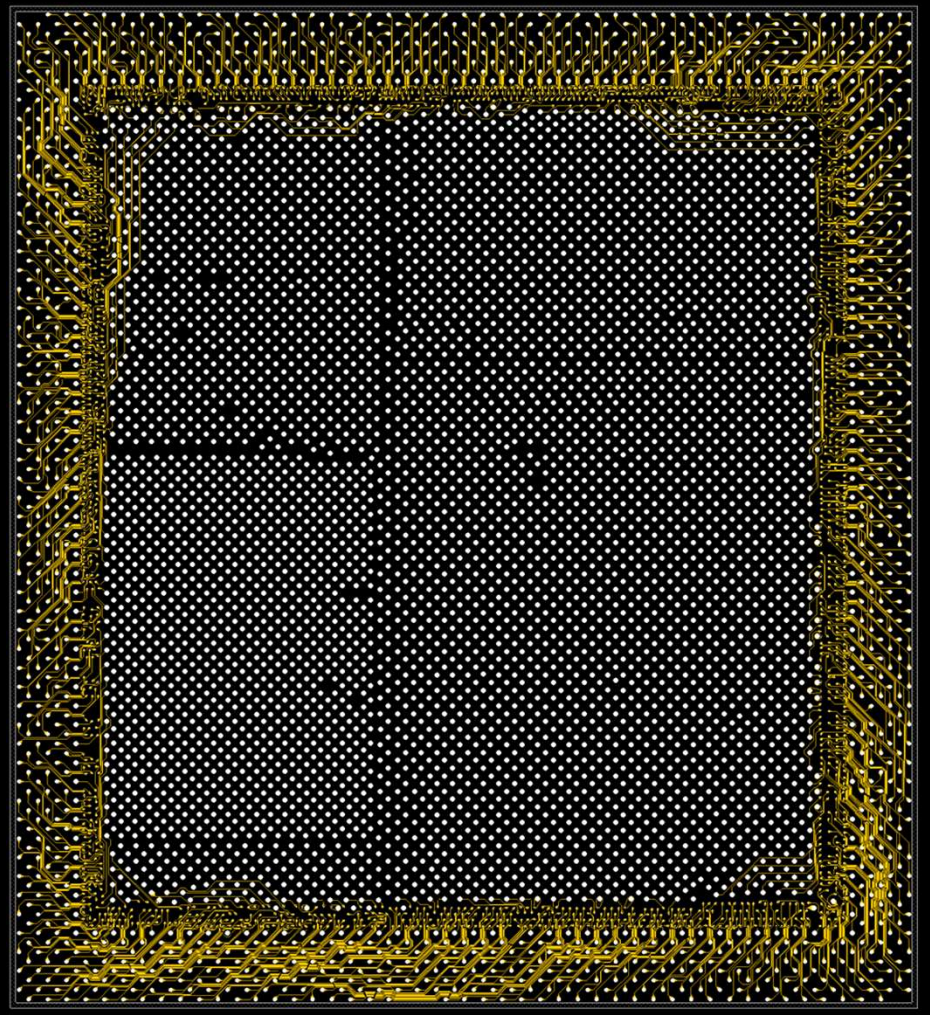
FOCoS Design Study

Adding RDL

- Achieved full routing in single layer
- 5 µm minimum trace & space



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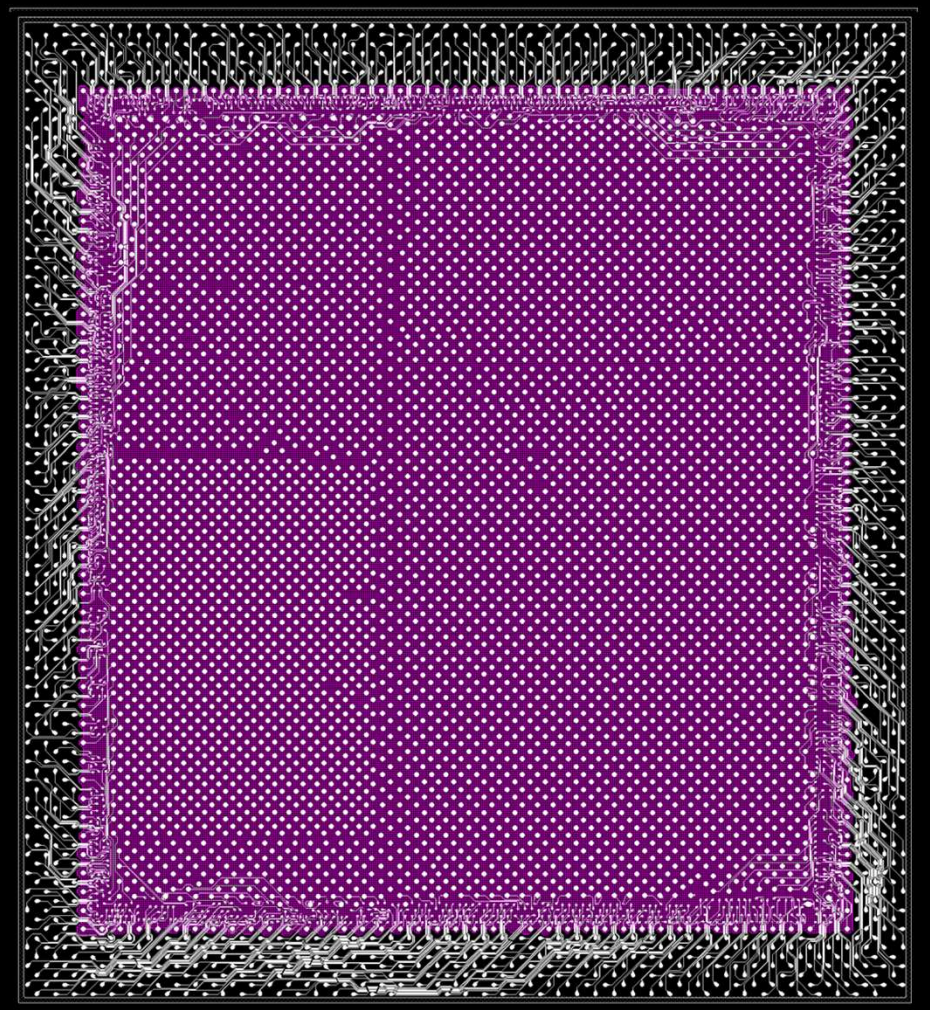
FOCoS Design Study

Adaptive Patterning

Adaptive Alignment

- Translates & rotates pattern precisely to measured die location (vias & RDL)



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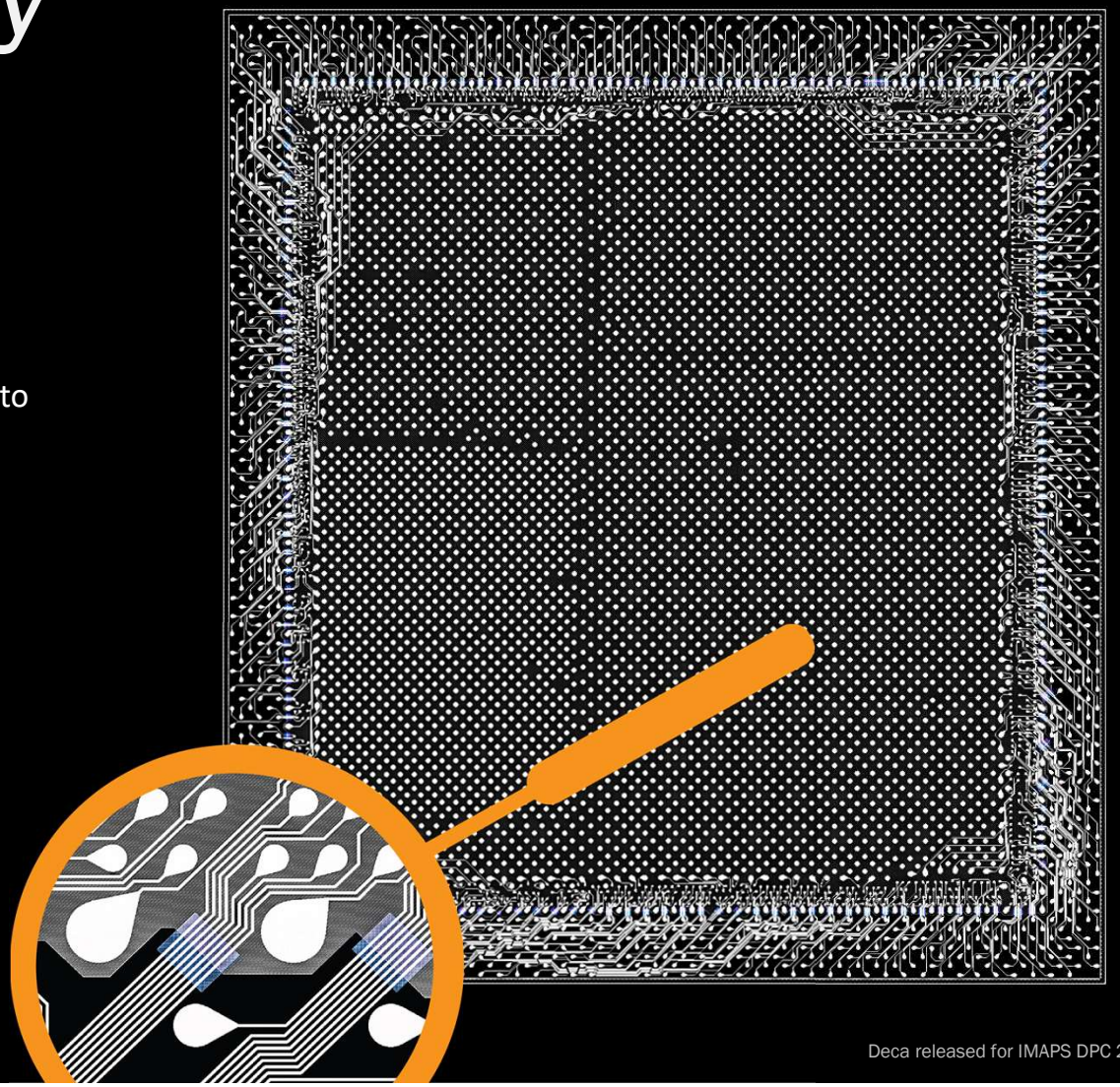
FOCoS Design Study

Adaptive Patterning

Adaptive Routing

- Dynamically adapt small portion of RDL to precisely complete the connection



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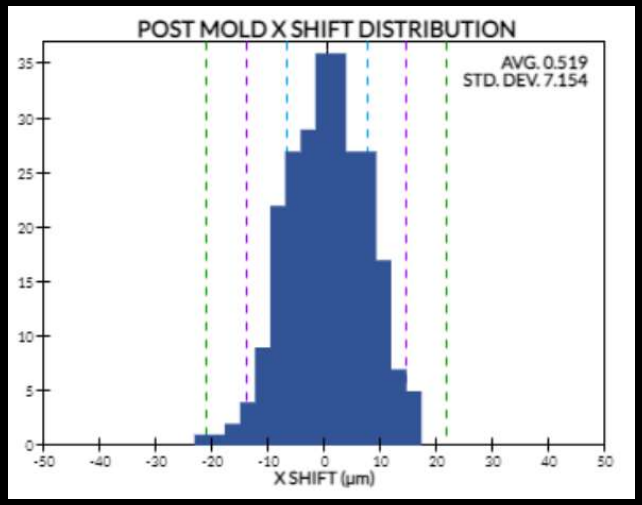
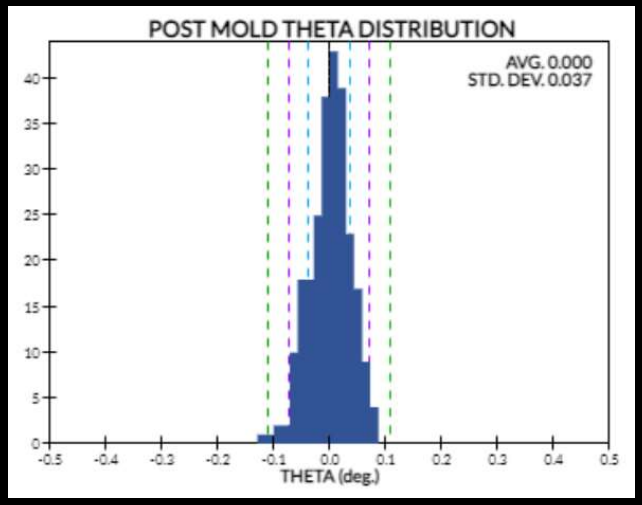
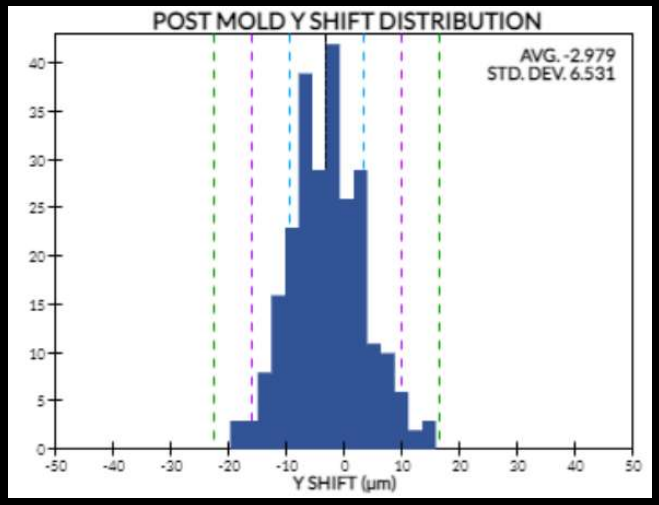
FOCoS Design Study

Simulated natural variation of ±20µm XY and ±0.1° rotation at 3σ (typical production values)







Simulated die displacement histograms

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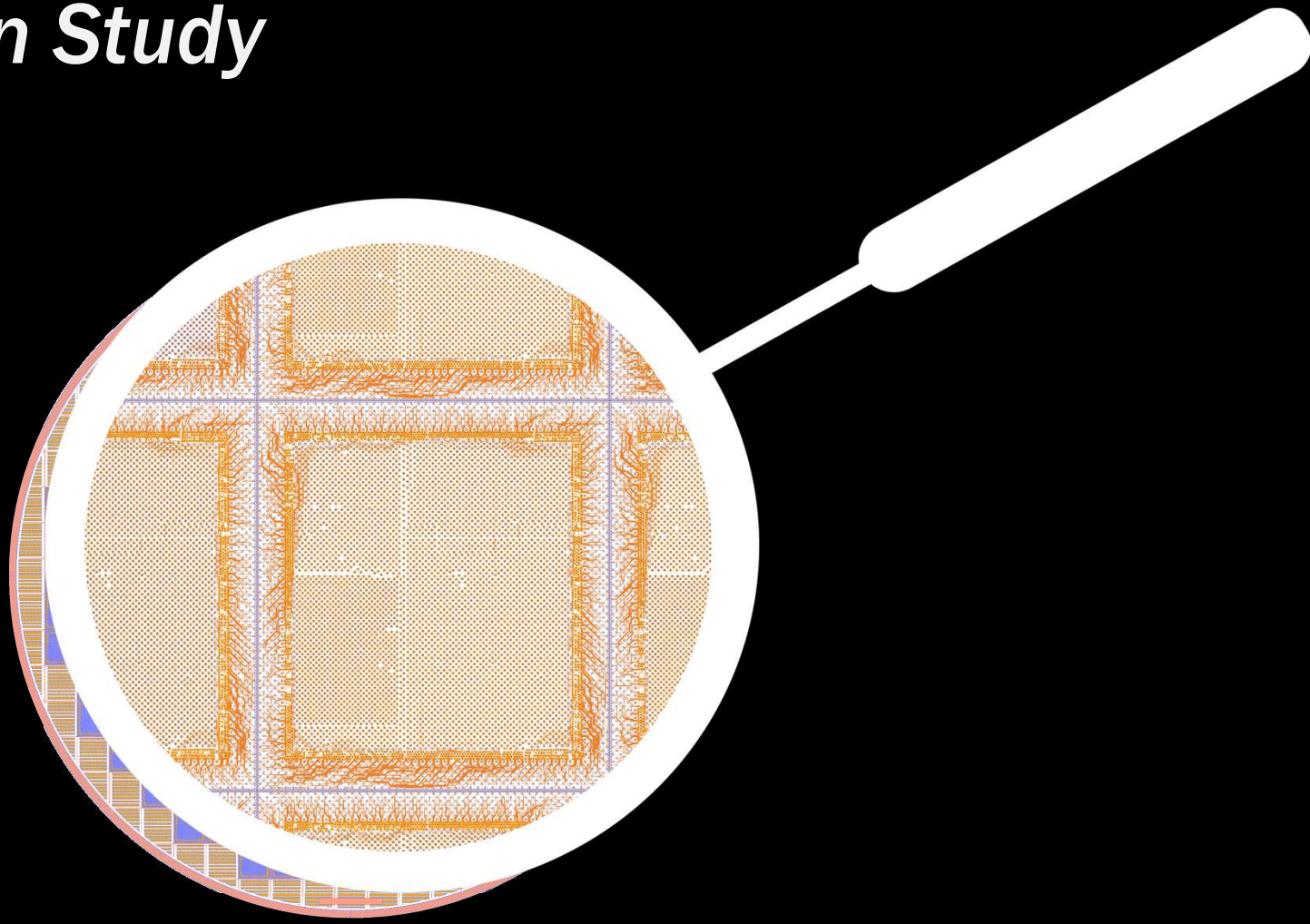
FOCoS Design Study

Simulation results

100% yield across
all die shifts



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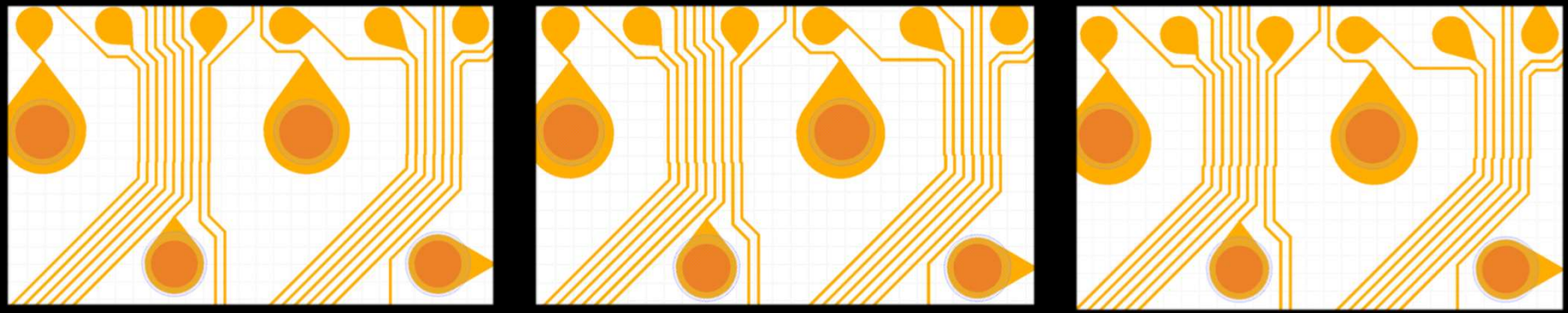
FOCoS Design Study

Physical trace variants across the simulated die shift range



Actual RDL variation is negligible

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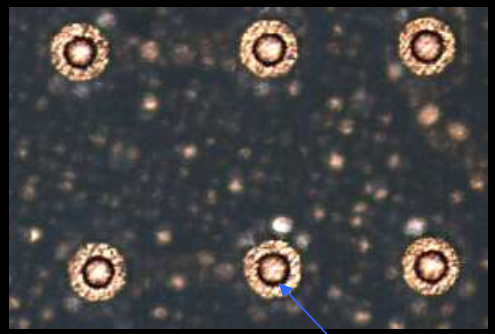
FOCoS Design Study

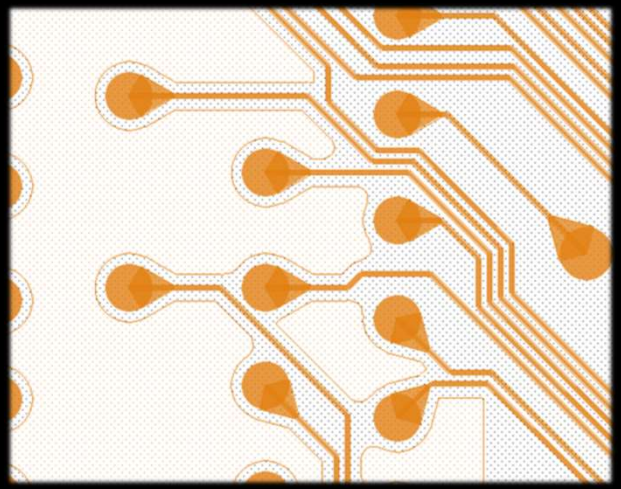
Actual customer device build

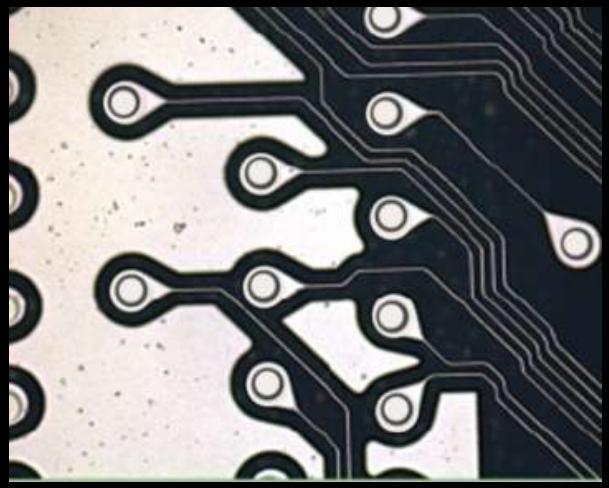
Adaptive Alignment

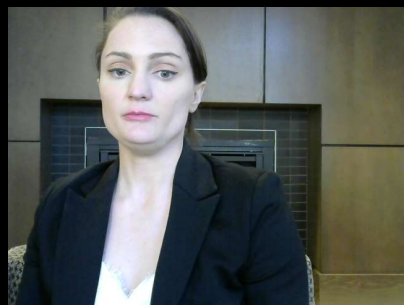


Vias aligned to
Cu stud centers

Adaptive Routing







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Conclusion

- Chiplets are now
- Multiple barriers currently exist for mass adoption
- M-Series & Adaptive Patterning provide powerful solutions
- Proven capability through actual FOCoS customer designs

The technology is ready

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Thank you from DECA

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