High-density Fan-Out Chip on Substrate using M-Series™ and Adaptive Patterning® Technology

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Agenda

• Introduction
• Industry Perspective
• Challenges & Solutions
• Design Study
• Conclusion
**Company introduction**

- Deca was born of a passion to transform electronic interconnect with inspiration from SunPower’s advanced solar wafer fab
- Our name describes our culture of 10X thinking, inspired by Greek déka (δέκα)
- Deca created 10X breakthroughs with M-Series™ & Adaptive Patterning®

**Now the industry’s #1 fan-out technology**

**Over 3.5 million devices shipping per day in Q1’22**

1. **M-Series**
   - Chips first, chips up fan-out technology
   - Gen 1 & Gen 2

2. **Adaptive Patterning**
   - Real-time optimized design during manufacturing (every device on every wafer)

*Note: Deca holds > 100 issued and pending patents on M-Series, Adaptive Patterning and related technology*
Deca is Owned by Industry Leading Companies

Board of Directors
Sam Geha – Chairman
Larry Michlovich - Director

Shankar Ekambaram - Director

Rich Rice – ASE Director

Tae-Hoon Kim - Director

Neal Bergstrom (observer)

Tim Olson – CEO Director
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The future is now...

Intel's Ponte Vecchio

AMD's Radeon

Chiplets are happening

"...Ponte Vecchio Xe-HPC GPU, Over 100 Billion Transistors & 47 XPU Compute Tiles"


"AMD Radeon… with Chiplet Design"

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Challenge - Pitch Limitations

Packaging severely lagging semiconductor device technology (15x vs. 500x density increase in past 20 years)

IC Transistor Density
(transistors per mm²)

Sources: 1. Chip scale Review: March-April 2020, IO/mm² derived from die pad pitch data

Packaging interface density orders of magnitude behind ICs
**Challenge - Pitch Limitations**

Industry leaders at 40µm to 45µm die pad pitch

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**M-Series Gen 1**  
(Chips First Fan-out)

Die pad pitch: 45 µm  
10 per mm²: 492

Introduced in 2016

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**Intel EMIB**  
(Hybrid chips in substrate)

Die pad pitch: 45 µm  
10 per mm²: 492

*45µm pitch reference: David Schor, Intel Unveils Foveros Omni And Foveros Direct; Leveraging Hybrid Bonding, WikiChip Fuse, July 26, 2021*

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**TSMC InFO-R**  
(Chips First Fan-out)

Die pad pitch: 40 µm  
10 per mm²: 545

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**M-Series Gen 2**  
(Chips First Fan-out)

Die pad pitch: 20 µm  
10 per mm²: 2,518

Deca’s Gen 2 delivers breakthrough 20µm die pad pitch thru Adaptive Patterning

5X interface density increase

*40µm pitch reference: Tom Dillinger, SemiWiki.com, Highlights of the TSMC Technology Symposium, 9/7/2020*
**Solution – Eliminating the Capture Pad**

**Example – TSMC InFO**

Via connection without Adaptive Patterning

20 µm via contact

50 µm diameter Cu capture pad

25 µm Cu Stud

Large Cu capture pad (extra layer added to Cu stud)

20 µm

50 µm

Source: Prismark iPhone 12 Analysis Jan’21

**M-Series™ with Adaptive Patterning**

Via connection with Adaptive Patterning

20 µm via contact

30 µm Cu Stud

Cu stud size (no need for extra Cu layer)

20 µm

30 µm

Source: Prismark iPhone 12 Analysis Jan’21

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**Solution – Eliminating the Capture Pad**

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Obstacles - Substrate availability

Significant shortfall in advanced substrate capacity is forecasted to persist
Solution – Simpler Substrates

FOCoS moves high-density interconnect to fan-out layers

2.4x pitch expansion on 6,000 IO example
Obstacle – Shift Happens™

1. Variation in mechanical placement of die
   - Actual die position varies from designed nominal

2. Displacement during encapsulation (molding)
   - Dielectric via opening
   - Designed position (nominal)
   - Die placement tolerance X, Y, & rotation
   - Mold displacement (during embedding)
   - Obstacle – Shift Happens™

- Chiplet architectures drive increasing die per package
- Each die placement & subsequent processing adds risk
- One die shifted out of position can lead to failure
Adaptive Patterning Methods™

Adaptive Alignment
Translate & rotate entire RDL pattern to the measured die position

Adaptive Routing
Dynamically adapt small portion of RDL to the measured die position(s)

Note: Multiple patents issued & pending covering all facets of Adaptive Patterning
Obstacles - Reticle Size

- Reticle limits typically ~850mm²
- Chiplet based devices often 36mm x 36mm (1,296mm²) and larger
- Reticle stitching required – technically feasible, commercially unattractive
Solution – Eliminate the Reticle

Adaptive Patterning utilizes fully digital lithography – no glass photomasks are used

*Entire 300mm round or 600mm square panel is a single exposure field*
Obstacles - Cost

Next generation packaging technologies demand costly materials and processes

The past

Today's challenge

Silicon interposers remain the de-facto solution for ultra-high-density integration

Wolfgang Sauter, Marvell, IMAPS DPC 2020
Solution – Eliminate the Si Interposer

Ultra-high-density organic solutions are positioned to replace Si interposers
Obstacles – Emerging Proprietary Solutions

Established independent supply chain for semiconductor packaging through the OSATs

However, latest advanced packaging technologies emerging from proprietary sources
Solution – Independent Advanced Technology

Ready access to advanced packaging technology – Deca’s proven solutions

- **M-Series Fan-out**
  - Chips first, chips up fan-out technology
  - Gen 1 & Gen 2

- **Adaptive Patterning***
  - Real-time optimized design during manufacturing (every device on every wafer)

Deca’s current licensees

- ASE GROUP
- nepes corporation
- skywater

And growing...
Solution – A Simple Process

M-Series chips first face up advanced fan-out technology

Die placement on carrier

Grind to expose studs and remove carrier

Build up with Adaptive Patterning

Overmold
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FOCoS Design Study

FOCoS moves high-density interconnect to fan-out layers

- 14mm x 16mm finished device
- 6,000 die pads with 2.4x expansion
FOCoS Design Study

Die specifications

- 4nm silicon
- 12mm x 13 mm
- 4500 core pins – 150 µm pitch
- 1500 periphery pins – 90 µm pitch
FOCoS Design Study

Molded M-Series Package

- 5 µm minimum trace & space
- 14 x 16 mm
- 1 routing layer
- 4500 core pins – 150 µm pitch
- 1500 periphery pins – 212 µm pitch

FOR = 1.44
Fan-Out Ratio
**FOCoS Design Study**

Adding RDL

- Achieved full routing in single layer
- 5 µm minimum trace & space
**FOCoS Design Study**

Adaptive Patterning

**Adaptive Alignment**

- Translates & rotates pattern precisely to measured die location (vias & RDL)
FOCoS Design Study

Adaptive Patterning

Adaptive Routing

• Dynamically adapt small portion of RDL to precisely complete the connection
**FOCoS Design Study**

Simulated natural variation of ±20µm XY and ±0.1° rotation at 3σ (typical production values)

Simulated die displacement histograms
FOCoS Design Study

Simulation results

100% yield across all die shifts
FOCoS Design Study

Physical trace variants across the simulated die shift range

Actual RDL variation is negligible
FOCoS Design Study

Actual customer device build

Adaptive Alignment

Adaptive Routing

Vias aligned to Cu stud centers
Conclusion

• Chiplets are now

• Multiple barriers currently exist for mass adoption

• M-Series & Adaptive Patterning provide powerful solutions

• Proven capability through actual FOCoS customer designs

The technology is ready
Thank you from DECA