# FOWLP Thermal Debonding: Easing Manufacturing Constraints

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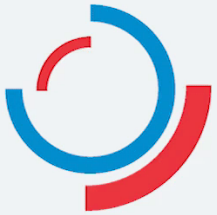


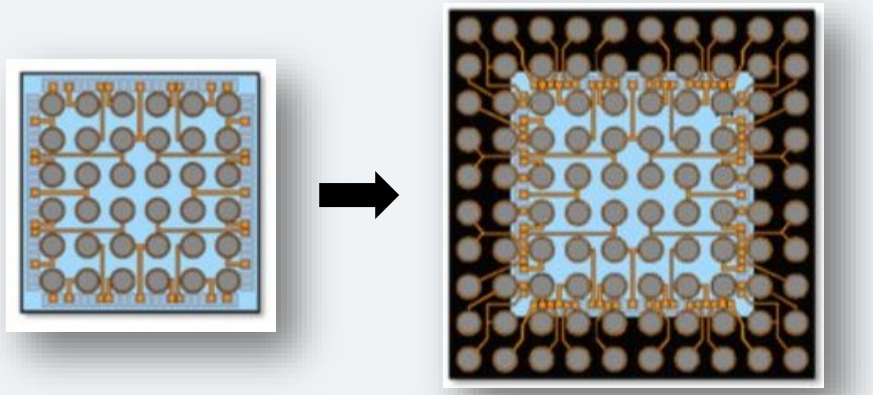




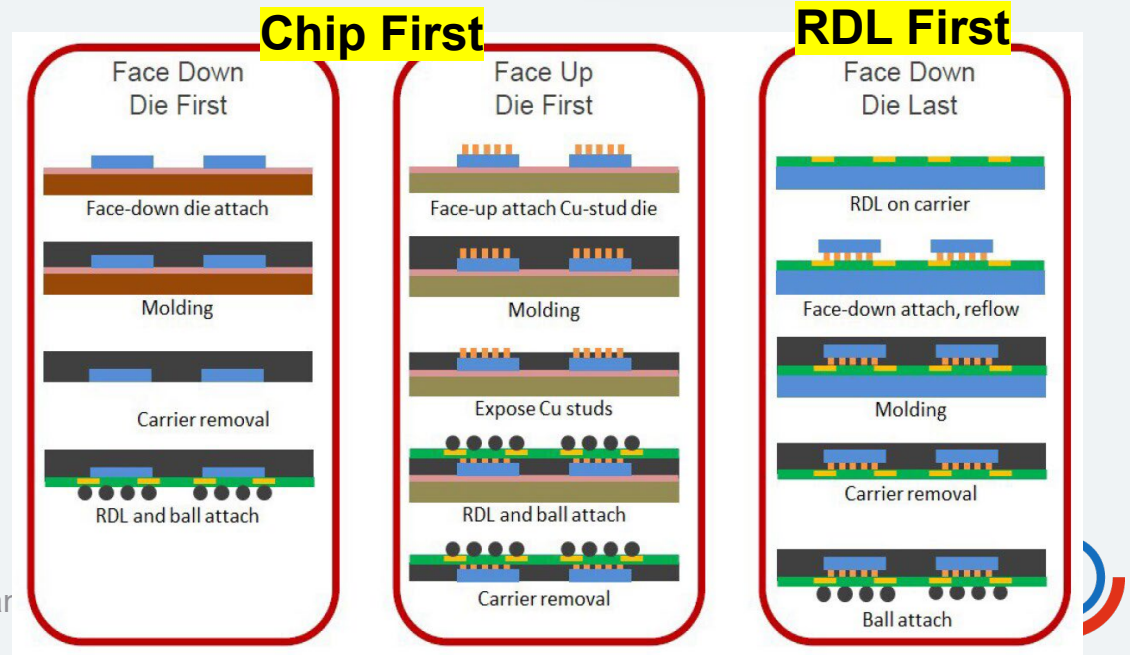

ERS

# What is Fanout?

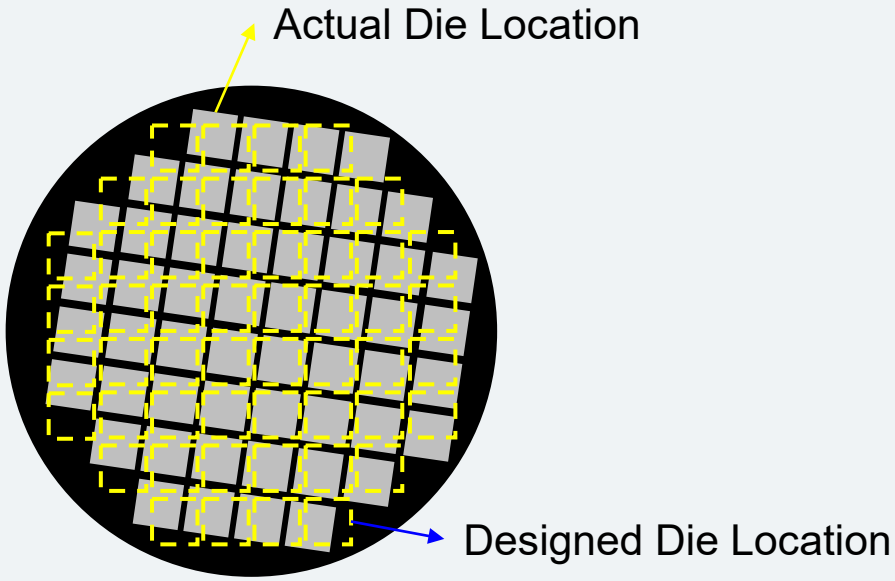
- **Fan-out** is a type of advanced chip packaging where the redistribution layer (RDL) are routed outside the surface area of the die.
- Several noted advantages are:
  - Good electrical performance
  - Enables high density routing
  - Enables multi die package configuration



*Credits: ASE*



# Fanout's Dilemma



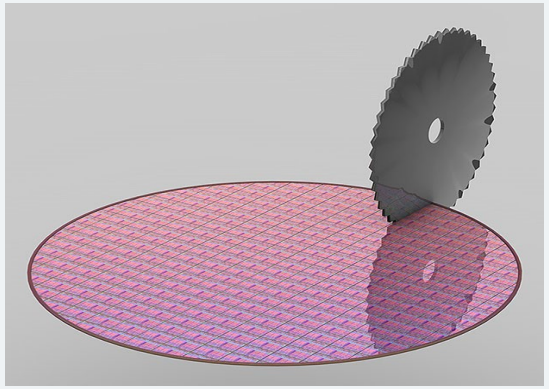

Die Shift is a defect in which the actual die location has an offset from the pre-defined position by a certain distance.

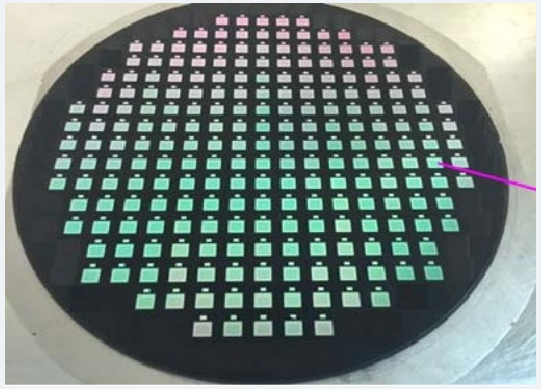
Warpage is the physical deformation encountered by the wafer due to coefficient of thermal expansion (CTE) mismatch between silicon and mold

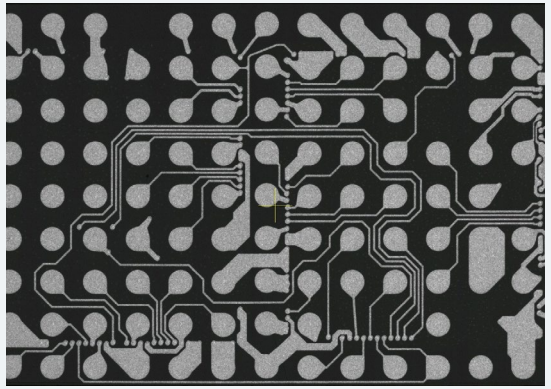
# Fanout Process

## Chip First – Face up or Face down

| Die Preparation | Wafer Reconstruction | Layer Build Up (Redistribution) | Die/Package Finishing |
|---|---|---|---|







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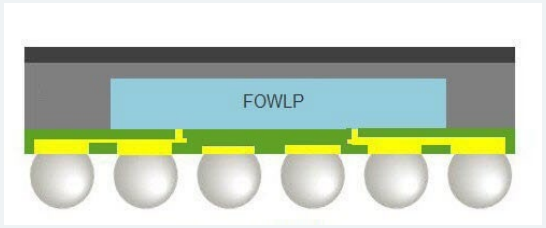
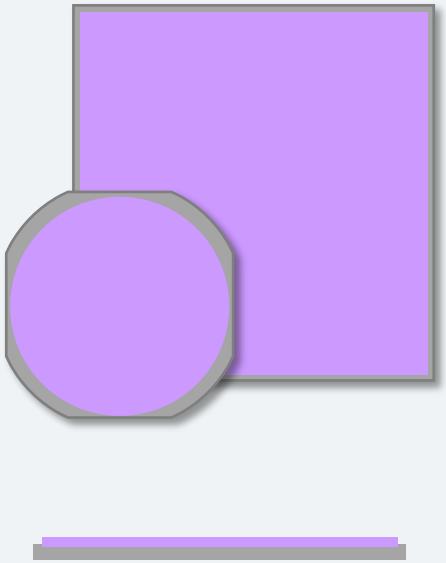
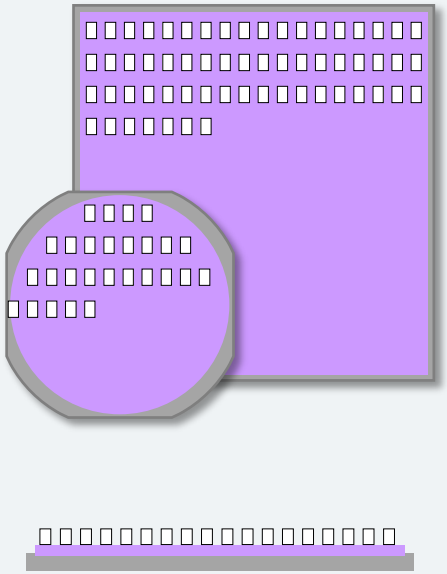


# Fanout Reconstruction Process

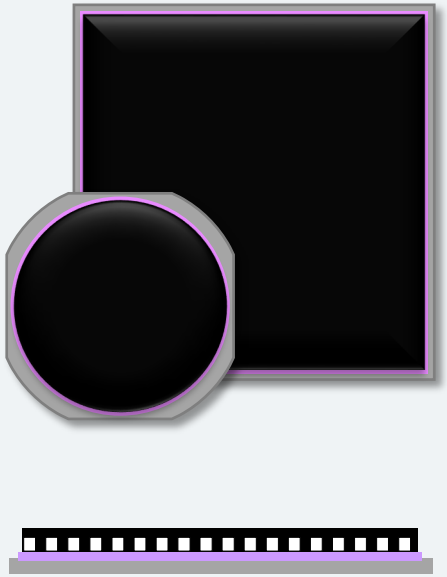
Carrier Lamination



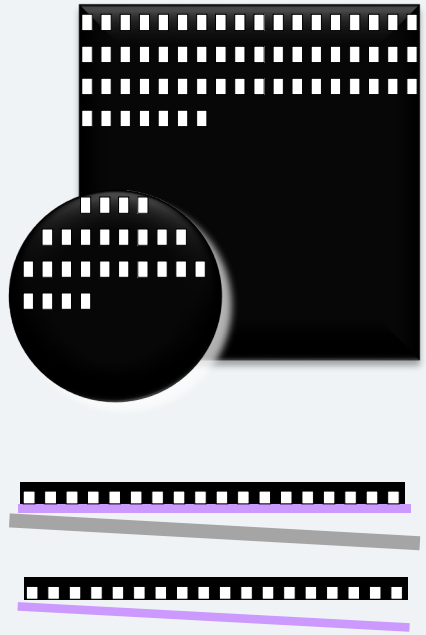
Die Bonding



Molding



Carrier Removal and Detaping



The reconstruction (wafer) or panelization (panel) process is the key differentiator of Fanout in comparison to *WLCSP/Fan-in process

*Wafer Level Chip Scale Packaging*

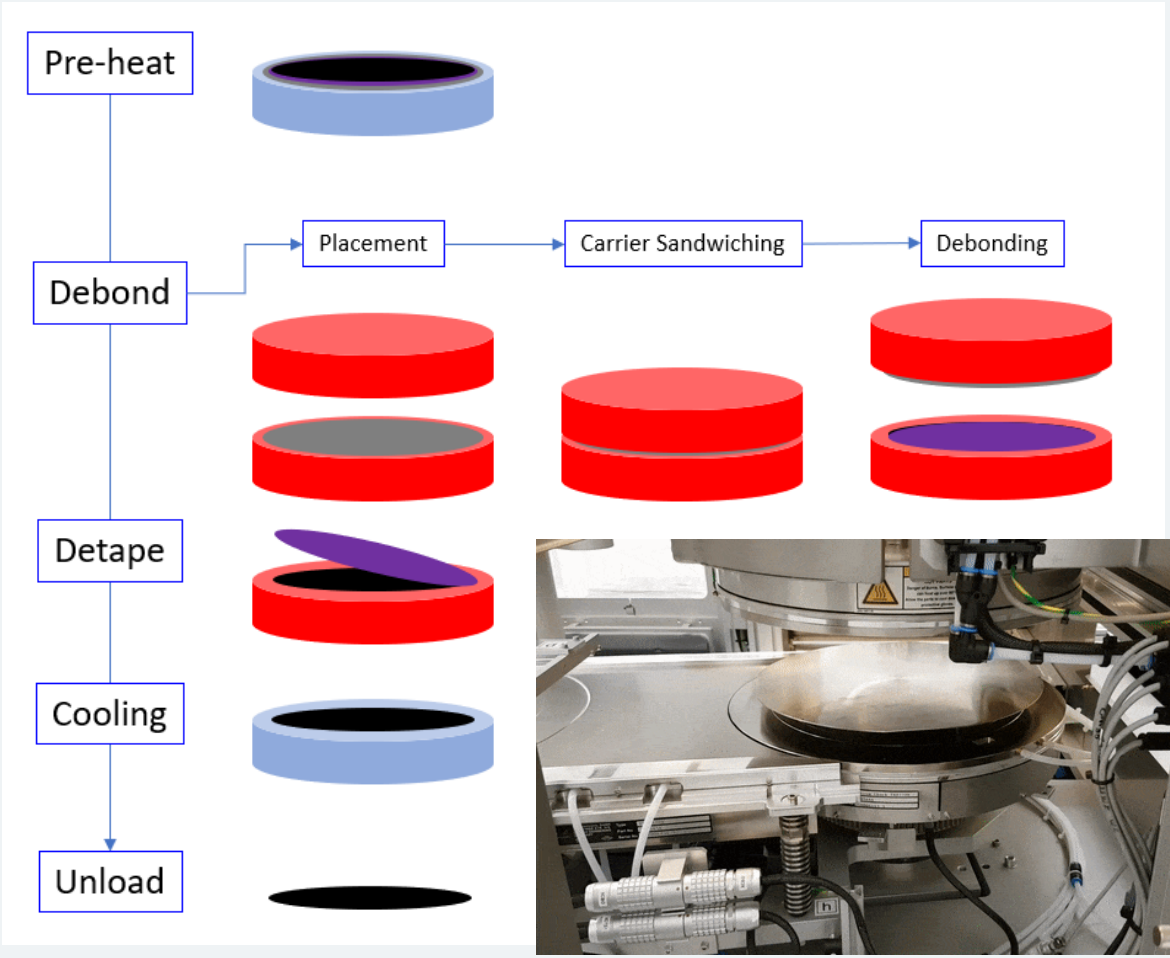
# Thermal Debond

Thermal debonding is the process of separating the reconstructed wafer from its carrier.
The whole process is composed of several thermal treatment with the aim of

- Stress free carrier removal
- Smooth Detaping
- No tape residue
- Minimal warpage

Key parameters

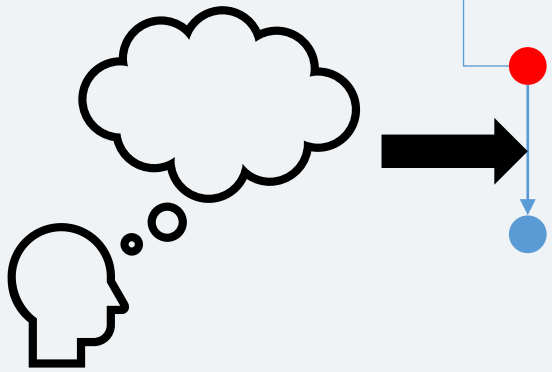
- Temperature
- Soak time
- Detape speed
- Detape angle

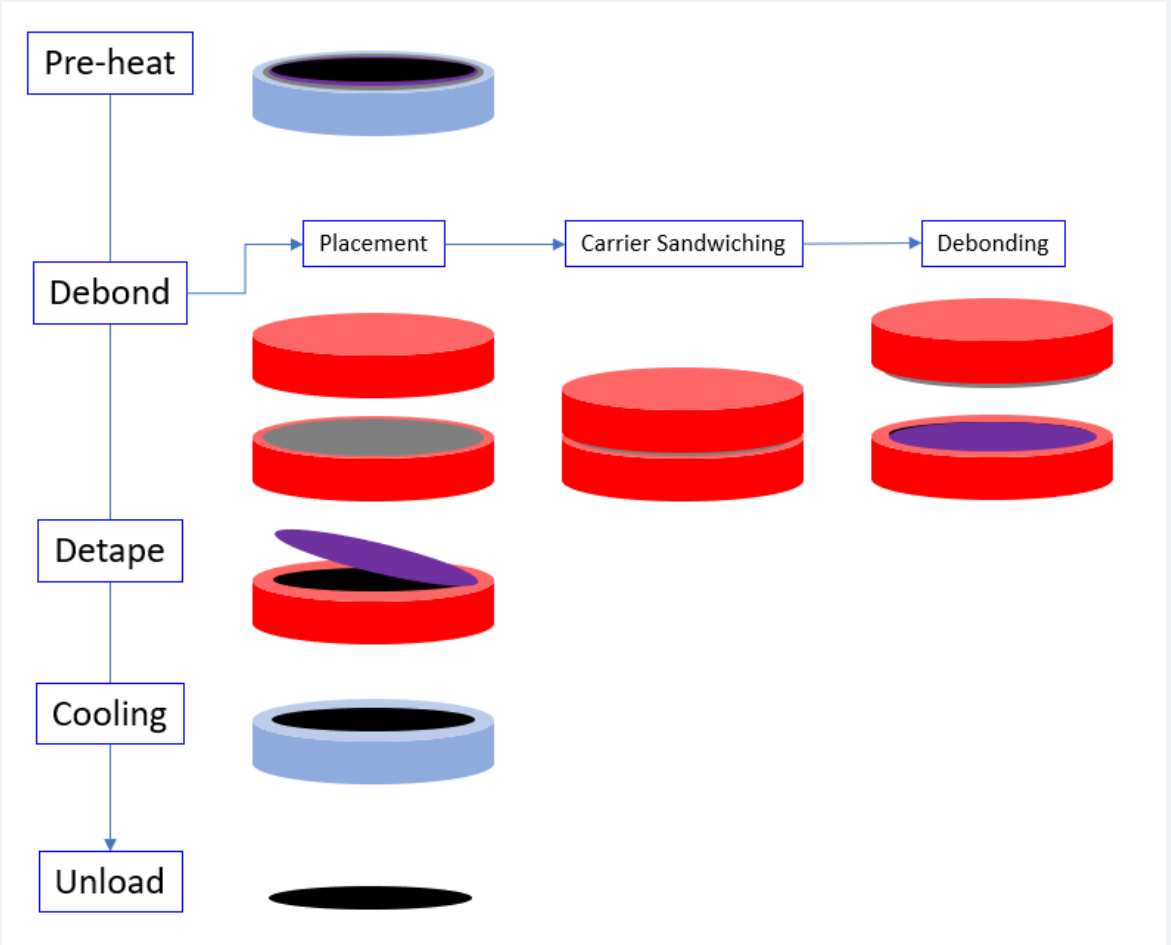


# Thermal Debond

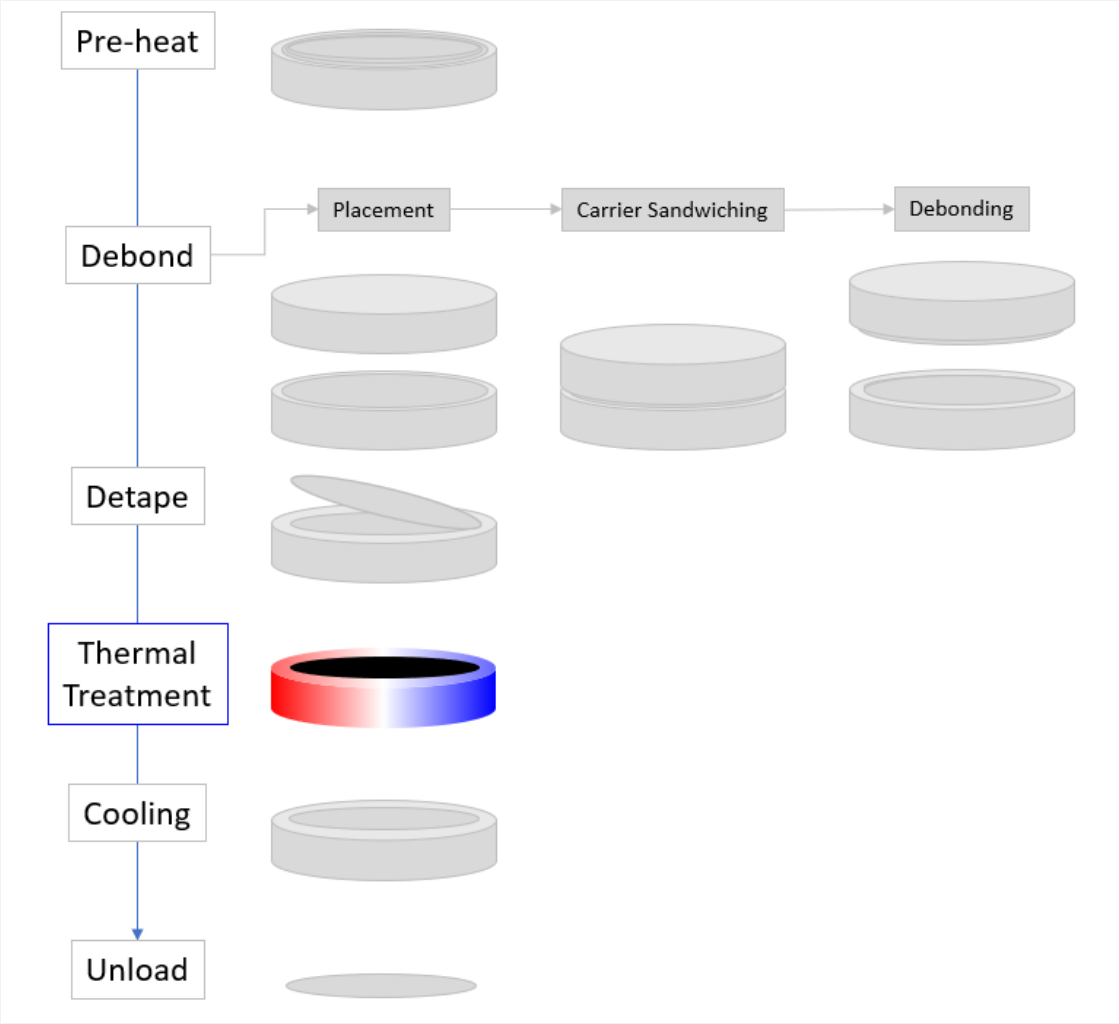
The wafer then goes into cooling stage.

This base process for thermal debond





# Enhanced Thermal Debond

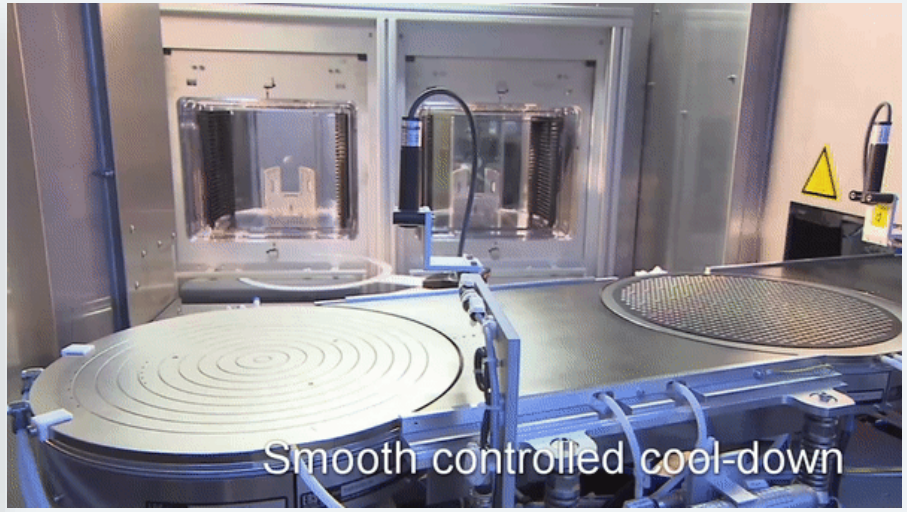



Improvement for thermal Debond

1. Add a second heating treatment

# Enhanced Thermal Debond

## TriTemp and AirCushion

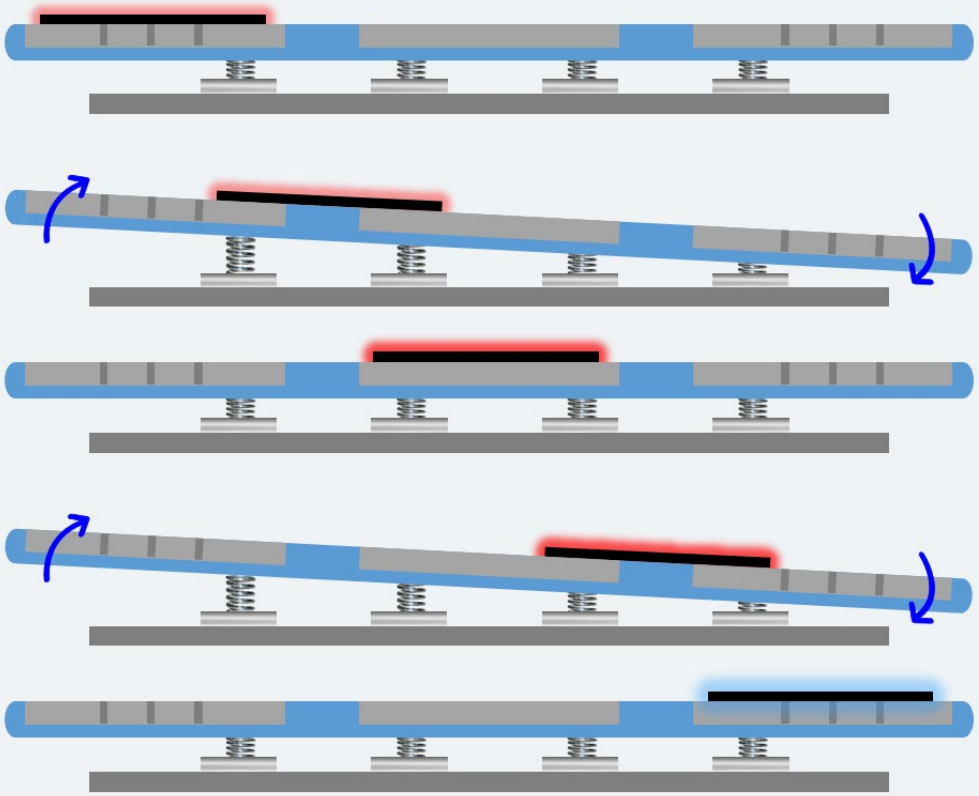


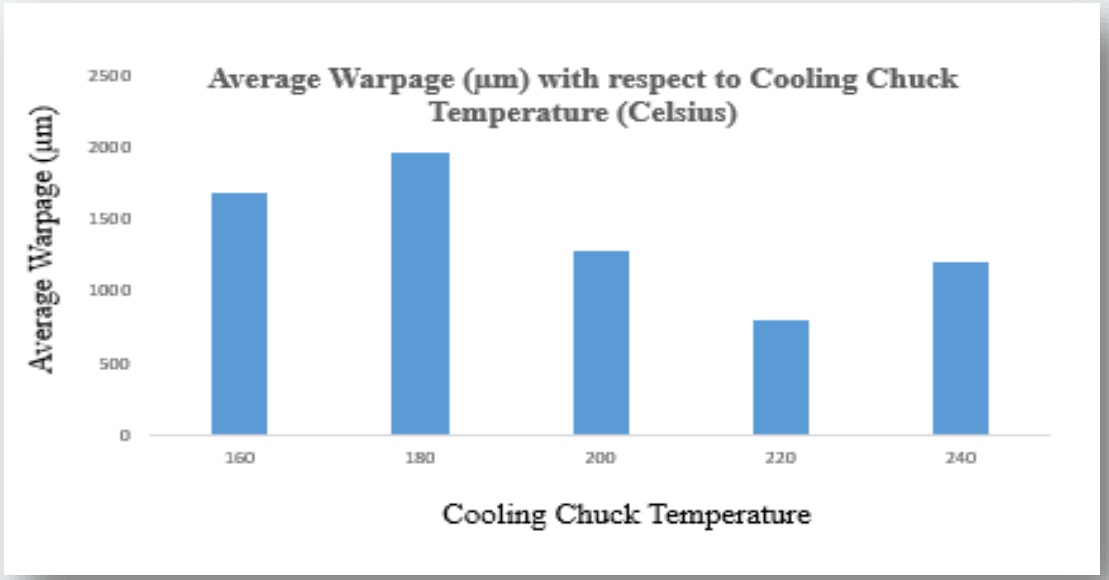

Benefits of a 2nd heating treatment

1. Allows “shock and lock” method which is a way to lock flatness into the wafer
2. Intermediate – slow cooling; instead of straight from debond temp (~180°C to 200°C) to room temperature, an intermediate temp of ~60°C to 110°C is done

# Enhanced Thermal Debond

## Shock and Lock

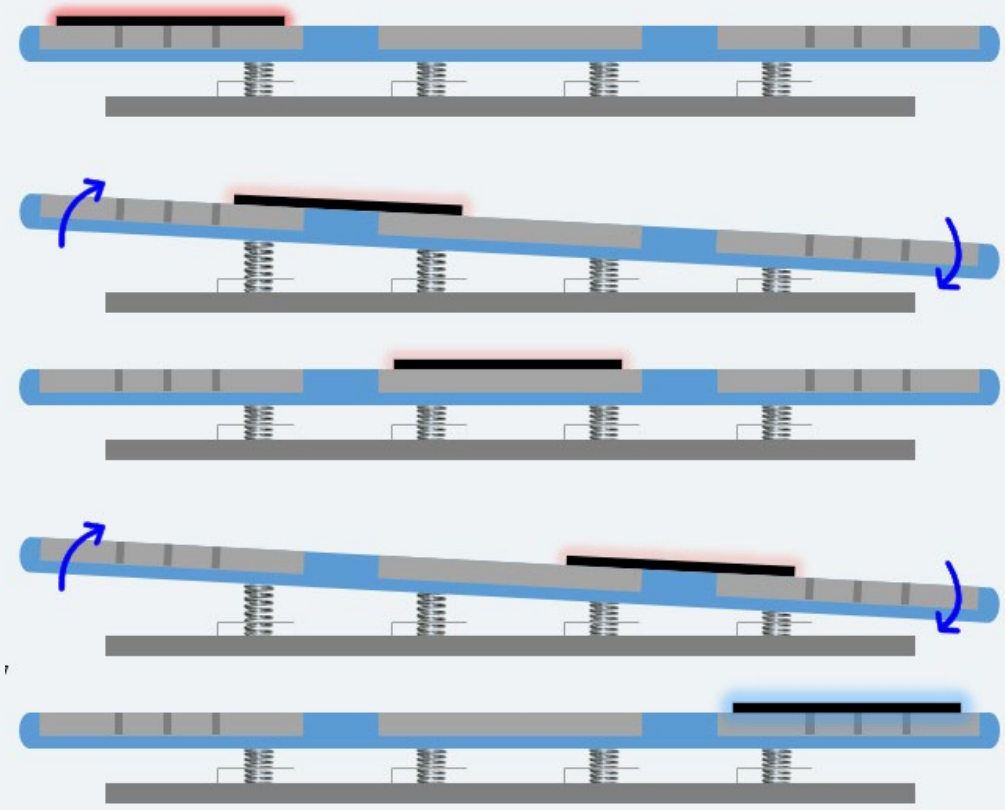


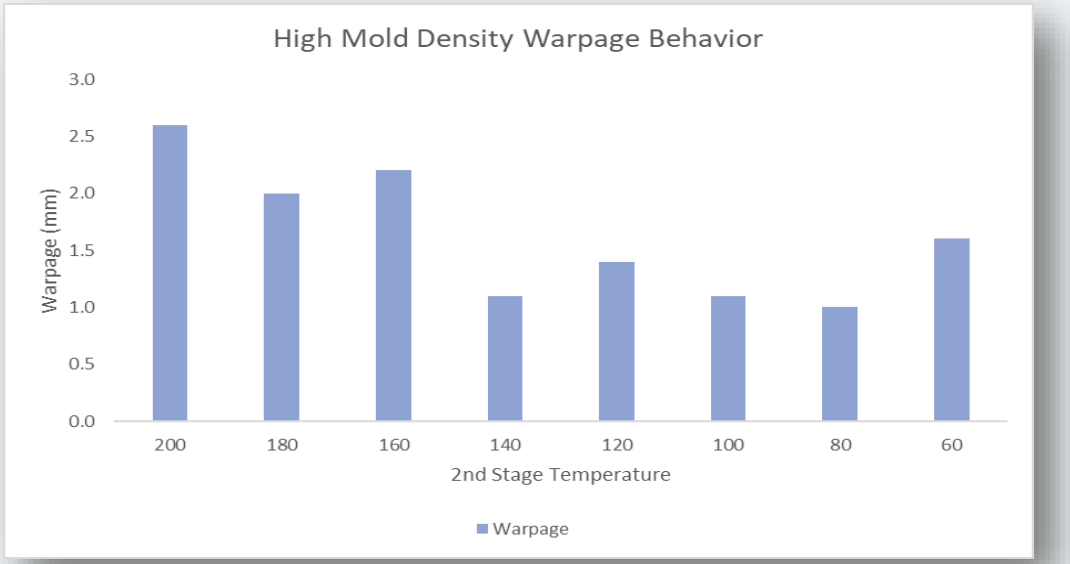



*For wafers with higher silicon content, high temperature for 2nd treatment showed better warpage performance

# Enhanced Thermal Debond

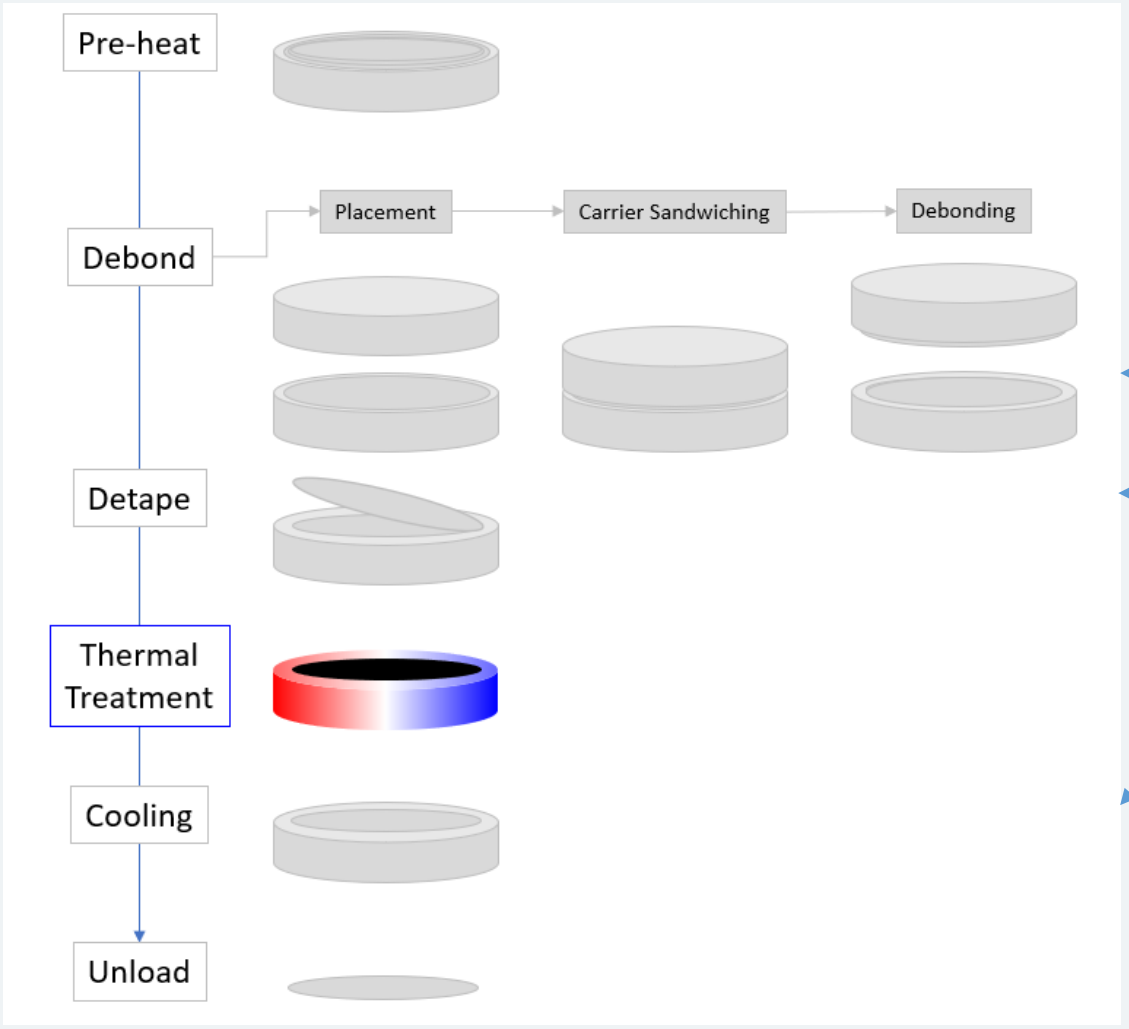
## Intermediate – Slow Cooling

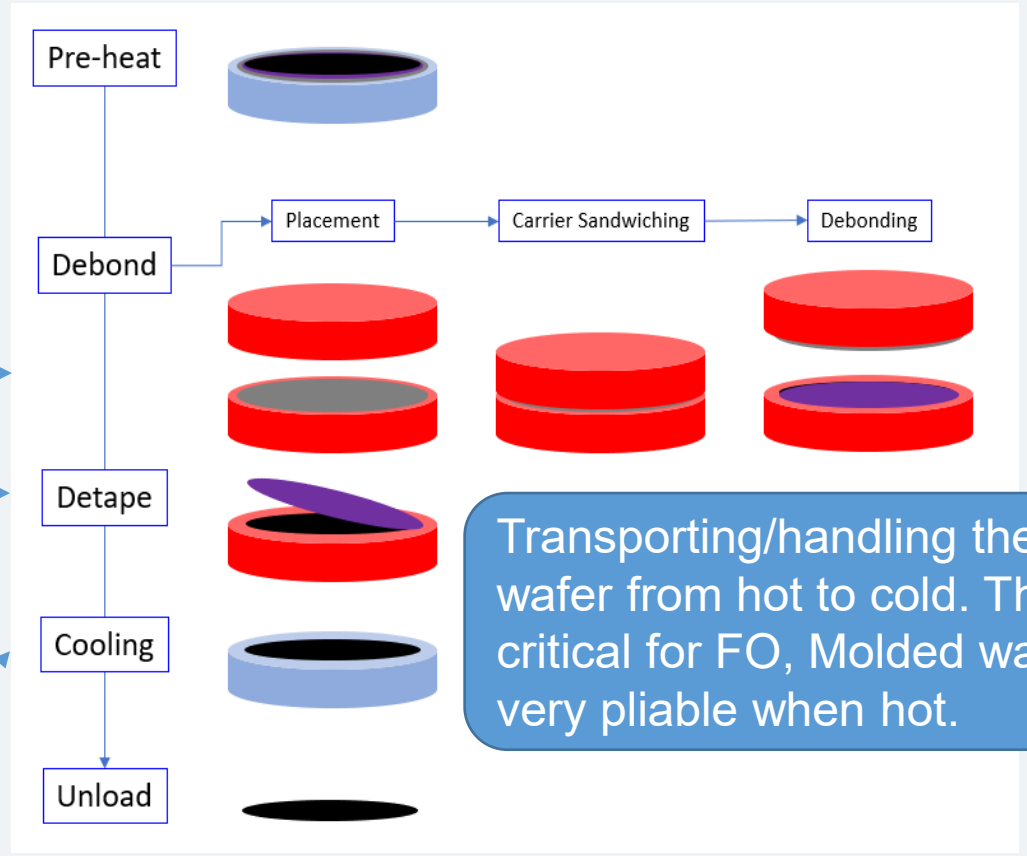





For wafers with more mold compound (thick overmold), warpage is minimal with slow cooling

# Enhanced Thermal Debond

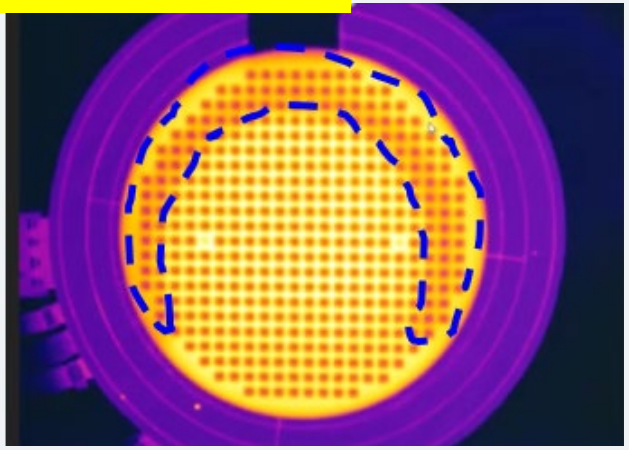


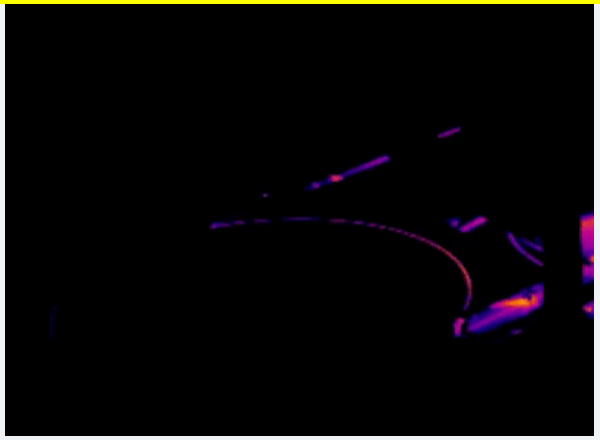

Transporting/handling the wafer from hot to cold. This is critical for FO, Molded wafer is very pliable when hot.

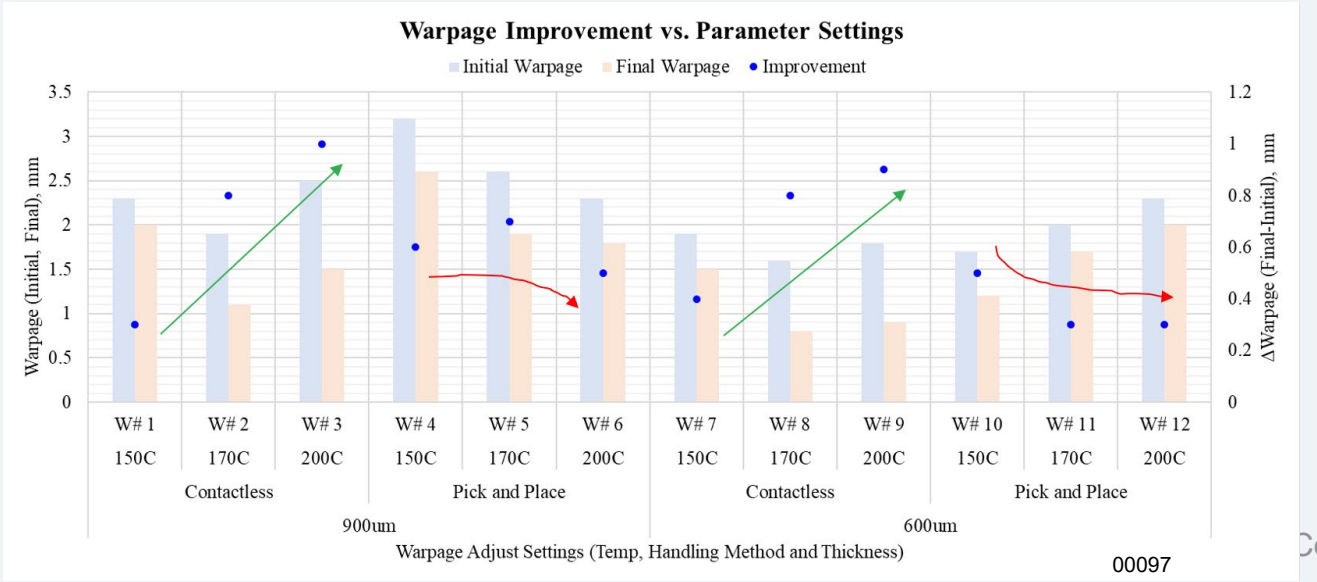
# Enhanced Thermal Debond

Pick and Place



TriTemp and AirCushion






- We have observed a different heat dissipation behavior between slide system and pick and place
- Slide system being more uniform and resulting to better warpage behavior
- Data also shows increasing temp result to higher warpage when doing pick and place

# Conclusion

- Enhancing Thermal Debond method shows great benefits in reducing warpage, this is done by
  - Adding a 2nd stage of thermal treatment
  - Eliminating pick and place handling when wafer is in high temperature state
- This minimal warpage output of the end process of the reconstruction module can greatly address the issues of handling in the next FO step which in RDL

# Thank You!
# Vielen Dank!

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