Designing Silicon Interposers For 2.5/3DIC Heterogeneous Integration - Meeting Foundry And OSAT Requirements

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Why Silicon Interposers?

1. Applications like AI, ML, and HPC driving demand for HBM
   Integration of HBM with silicon typically require sub-5um geometry

2. Heterogeneous integration of multiple technologies and processes
   Platform to disaggregate large SoCs into multiple Chiplets

3. Lower risk/cost alternative to advanced node monolithic devices
Silicon Interposer characteristics

Incorporates multiple devices and substrates
  • Heterogeneous data in different formats and from different sources – diverse supply chain

Utilizes device and/or substrate stacking
  • Stack definition and management, dual sided devices with internal connections

Very high pin count die and substrates >200K pins
  • Data capacity and performance

Neither a chip or package but incorporates elements of both
Workflow for 2.5D Interposer Design

ASIC/Die Physical Design and Verification

System Inputs

Co-Design Planning & Prototyping

Physical Implementation

Sign-off & Verification

Modeling Fidelity

Predictive

In-Process

Final

SI/PI/EM Analysis

Thermo-Mechanical Stress Analysis

Substrate Verification

Assembly Verification

Data Management / Trust & Assurance

Ecosystem Integration – PDK/ADK/CDK and MCAD
Design Setup

Data from Foundry / OSAT

Process Design Kit

- Technology file
- Design Rule Manual
- Verification rule decks for final sign-off (DRC, LVS, etc.)
Assembly Planning

Predictive Modeling

Verilog
Assembly – Design Example

- Reference flow for major foundry
- One SoC, 4 HBM
- Graphically assembled with > 200K pins
Early Verification

- Confirm all die and interface are DRC clean
- Assembly DRC – bump overlap, centering
- Begin initial substrate DRC Checks
  - Manufacturing rule regions
  - Chip finishing layers
- Verify continually – don’t wait for sign-off
Physical Implementation

Physical Substrate Implementation

- Detailed constraint import & setup
- Detailed placement – stacking, embedding, etc.
- Design routing including high-speed tuning
- Power plane/striping and degassing generation
- Physical IP block reuse and team-based design
- SI/PI and DFM validation
- Generate manufacturing outputs & docs

Qualified design ready for implementation

PDK/ADK/CDKs Tech templates

In-process identification/resolution of overt SI/PI, DFM & thermal errors to minimize sign-off iterations

Signal Integrity

Thermal Analysis

Power Integrity

In-process DFM

Manufacturing Outputs

GDS
OASIS
Gerber
ODB++
IPC-2581
Others…

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Power Distribution – Traditional Packaging

Power and ground are implemented as plane metal in traditional packaging and PCB design.

Metal stress relief voids and density can be met using today’s EDA tools, but meeting DRC rule requirements can be tricky.

Power striping is typically used in IC design for power distribution – and we’ve implemented this in our reference example.
Power Distribution – IC Design

IC designers typically use a multi-layer power striped mesh to distribute power.

Automated, hierarchical, scalable.
SoC Mesh (Layers 1, 2, and 3 with bumps included)

Layer 1 Only. Pins connect directly to layer 1 with stub. VDD and VSS and are in checkered pattern

Layer 2 stripes interdigitated pattern VDD, VSS using vias

Layer 3 Only. Pins connect directly to layer 3 with stub. VDD and VSS and are in checkered pattern
Adapt power striping to include several custom types for power domains

Nested power networks
Fanout to Routing Levels

Fanout from bottom bump to routing layer (3)

Fanout from top bump to routing layer (1)
Adaptive Routing Breakouts

Break-out routing from signal bumps to ordered signal channel lines

Enhances automated routing performance
HBM Channel Routing
Resulting Design
Verification Performance

Complete N40 DRC rule deck

- Version with squares
- Version with hatched ground plane

- Total CPU time
- Real time
- Total LVHEAP

MB

Time (s)
Verify physical implementation connectivity matches netlist with LVS

Typically, foundries/OSATs do not accept design submissions unless the are verified LVS/DRC clean
Summary

Challenges to IC interposer design

• Design start / setup / technology data from foundry
• Floor-planning needs with very large pin counts
• Implementation of traditional IC design constructs
• Foundries require sign-off verification of manufacturing data

This is how you do it in a packaging tool

• Work with foundry to install PDK
• Graphical floor-planning and assembly with connectivity management
• Automated fan-outs/break-outs, signal routing, power routing
• Verify – early and often

Utilize your IC design and packaging resources
Thank You