HETEROGENEOUS INTEGRATION WITH 3D PACKAGING

Rahul Agarwal, Patrick Cheng, Priyal Shah, Brett Wilkerson, Raja Swaminathan, John Wuu
OUTLINE

- Motivation
- Packaging choices
- AMD 3D V-Cache Overview/Technology
- Performance
- Summary
OUTLINE

- Motivation
- Packaging choices
- AMD 3D V-Cache Overview/Technology
- Performance
- Summary
LARGE L3 CACHES PROVIDE IPC UPLIFT

But SRAM don’t scale as fast as logics

* Naffziger, VLSI Short Course, 2020
FIGURE OF MERITS

- COST OF PACKAGING ($)
- TESTABILITY
- THERMAL DENSITY & EFFECTIVENESS OF HEAT EXTRACTION (Qja: C/W)
- ENERGY PER UNIT BIT TRANSFERRED BETWEEN CHIPLETS (pJ/bit)
- LATENCY OF CHIPLET-TO-CHIPLET CHANNELS (ns)
- RELIABILITY
- SUPPORT SPEED MATCHING OF CHIPLETS
- EFFICIENT POWER/GROUND DISTRIBUTION (Z)
- B.W. DENSITY OF CHIPLET-TO-CHIPLET DATA COMMUNICATION (Gb/sec/sq.mm)
OUTLINE

- Motivation
- Packaging choices
- AMD 3D V-Cache Overview/Technology
- Performance
- Summary
HYBRID BONDING

HYDROPHILIC DIELECTRIC-DIELECTRIC BONDING + DIRECT CU-CU BONDING
**AMD 3D ARCHITECTURE**

- Hybrid Bond (9u pitch)
- Back End Like TSV

**>3X**
Interconnect Energy Efficiency
Compared to Micro Bump 3D

**16X**
Interconnect Density
Compared to Micro Bump 3D

**BETTER SIGNAL/POWER**
Lower TSV capacitance, inductance
Compared to Micro Bump 3D

* R. Swaminathan, “Hot chips Tutorials, HC33, 2021*
• Face to back stacking approach used for seamless inter-portability of bottom die design.
• Chip on Wafer stacking scheme used to enable different die sizes in the stack.
OUTLINE

- Motivation
- Packaging choices
- **AMD 3D V-Cache Overview/Technology**
- Performance
- Summary
ENGINEERING THE 3D CHIPLET ARCHITECTURE

- Structural silicon
- 64MB L3 cache die
- Direct copper-to-copper bond
- Through Silicon Vias (TSVs) for silicon-to-silicon communication
- Up to 8-core "Zen 3" CCD

AMD 3D V-CACHE COMPONENTS

“Zen 3” x86-64 CPU Core Complex Die (CCD)
- TSMC 7nm technology
- 8 cores per Core Complex (CCX)
- 32MB shared L3 Cache
- 81mm²
- AMD 3D V-Cache support integrated from Day 1

AMD 3D V-Cache extended L3 Die (L3Die)
- TSMC 7nm Technology
- 64MB L3 Cache Extension
- 41mm²

AMD 3D V-Cache Structural Dies
- Structural support for thinned CCD
- Thermal dissipation for CPU cores
STACKING DETAILS

- TSMC SoIC process
- Cu-Cu Hybrid bonding using Bond Pad Metal (BPM)
- TSV pitch = Hybrid bond pitch
- Bond Pad Via (BPV) connects BPM to M13
- Die to Wafer bonding process
- Face to back integration scheme
- 9um minimum TSV pitch
- MCM Package with C4 bump attach to substrate
Cu-Cu inter-diffused interface is ultra robust
Successfully passed various JEDEC specific package level reliability tests
OUTLINE

- Motivation
- Packaging choices
- AMD 3D V-Cache Overview/Technology
- Performance
- Summary
AMD 3D V-CACHE™ PRODUCT PORTFOLIO

- AMD 3rd Gen EPYC™ Server CPU
- AMD RYZEN™ 7 5800X3D Gaming CPU

- AMD 3D V-Cache™ supports L3 Cache extension for both server and desktop product families
DESKTOP PERFORMANCE

AMD RYZEN™ 7 5800X3D WITH AMD 3D V-CACHE™

Watch Dogs®... 1.36X
Far Cry® 6 1.24X
Gears 5™ 1.21X
Final Fantasy™ XIV 1.16X
Shadow of the... 1.09X
CS:GO™ TIE

~15% faster gaming at 1080p high
STATE OF THE ART COMPARISON

AMD RYZEN™ 7 5800X3D WITH AMD 3D V-CACHE™

World’s fastest gaming processor
SERVER PERFORMANCE

24.4 JOBS/HOUR
3RD GEN AMD EPYC™ 16-CORE
WITHOUT AMD 3D V-CACHE™

~66% FASTER RTL VERIFICATION
SYNOPSYS® VCS®

40.6 JOBS/HOUR
3RD GEN AMD EPYC™ 16-CORE
WITH AMD 3D V-CACHE™

RESULTS MAY VARY. SEE ENDTNOTES: MLNX-001R
OUTLINE

- Motivation
- Packaging choices
- AMD 3D V-Cache Overview/Technology
- Performance
- Summary
SUMMARY

- AMD 3D V-Cache is industry’s 1st 3D product for HPC applications
- AMD 3D V-cache is industry’s 1st demonstration of hybrid bonding in HPC space
- Packaging scheme of choice allows for easy portability of chiplets across product families
- Technology has been fully qualified in MCM packages
ACKNOWLEDGEMENT

The authors would like to thank TSMC R&D, DTP, BD, and CSV organizations for their collaboration and support and colleagues in AMD Cores, Advanced Packaging Technology, Product Development Engineering, Device Analysis Labs, and Foundry Technology Operations for their contributions.
ENDNOTES

RSK-003: Testing by AMD performance labs as of 09/01/2020. IPC evaluated with a selection of 25 workloads running at a locked 4GHz frequency on 8-core "Zen 2" Ryzen 7 3800XT and "Zen 3" Ryzen 7 5800X desktop processors configured with Windows® 10, NVIDIA GeForce RTX 2080 Ti (451.77), Samsung 860 Pro SSD, and 2x8GB DDR4-3600. Results may vary.

EPYC-026: Based on calculated areal density and based on bump pitch between AMD hybrid bond AMD 3D V-Cache stacked technology compared to AMD 2D chiplet technology and Intel 3D stacked micro-bump technology.

EPYC-027: Based on AMD internal simulations and published Intel data on *Foveros®* technology specifications.

RSK-106: Based on testing by AMD as of 12/14/2021. Performance evaluated with Watch Dogs Legion, Far Cry 6, Gears 5, Final Fantasy XIV, Shadow of the Tomb Raider and CS:GO. All games tested at 1920x1080 resolution with the HIGH in-game quality preset (or equivalent). System configuration: Ryzen 7 5800X3D and AMD Reference Motherboard, Ryzen 9 5900X and ASUS Crosshair VIII Hero with BIOS 3802. Both systems configured with 2x8GB DDR4-3600, GeForce RTX 3080 with 472.12 driver, Samsung 980 Pro 1TB, NIXT Kraken X62, and Windows 11 28000.282.

RSK-107: Based on testing by AMD as of 12/14/2021. Performance evaluated with Watch Dogs Legion, Far Cry 6, Gears 5, Final Fantasy XIV, Shadow of the Tomb Raider and CS:GO. All games tested at 1920x1080p resolution with the HIGH in-game quality preset (or equivalent). System configuration: Ryzen 7 5800X3D and AMD Reference Motherboard with 2x8GB DDR4-3600, Core i9-12900K and ROG Maximus Z690 Hero motherboard with BIOS 0702 and 2x16GB DDR5-5200. Both systems configured with GeForce RTX 3080 on driver 472.12, Samsung 960 Pro 1TB, NIXT Kraken X62, Windows 11 28000.282.

MLNX-0011: EDA RTI Simulation comparison based on AMD internal testing completed on 9/20/2021 measuring the average time to complete a test case simulation, comparing: 1x 16C 3rd Gen EPYC CPU with AMD 3D V-Cache Technology versus 1x 16C AMD EPYC® 73F3 on the same AMD *Daytona* reference platform. Results may vary based on factors including silicon version, hardware and software configuration and driver versions.
DISCLAIMER AND COPYRIGHT

©2022 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD Arrow logo, EPYC, Ryzen, Infinity fabric, and combinations thereof are trademarks of Advanced Micro Devices, Inc.
Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions, and typographical errors.
The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. Any computer system has risks of security vulnerabilities that cannot be completely prevented or mitigated. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

This information is provided "as is." AMD makes no representations or warranties with respect to the contents hereof and assumes no responsibility for any inaccuracies, errors, or omissions that may appear in this information. AMD specifically disclaims any implied warranties of non-infringement, merchantability, or fitness for any particular purpose. In no event will AMD be liable to any person for any reliance, direct, indirect, special, or other consequential damages arising from the use of any information contained herein, even if AMD is expressly advised of the possibility of such damages.