Hybrid Bonding for the Next Generation of High-Performance Devices

Laura Mirkarimi
VP of Engineering, 3D Portfolio and Bonding Technology

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Topics for Discussion

• Market Drivers for Hybrid Bonding
• Direct Bond Interconnect (DBI®) Description and Value Proposition
• Technology Demonstrations
• Supply Chain Readiness
• Market Adoption of Hybrid Bonding Technology
Market Drivers for Technology Adoption of Hybrid Bonding

- More than Moore Revolution

- Chiplet Architectural Concepts for Performance Enhancement and Cost Reduction

- Limitations in Solder Interconnect
Moore’s Law Reaching Limits

What Options Do We Have to Solve This Challenge?

• New Materials for Transistors
• Innovation in Computing Approaches
• Innovation in Packaging and Chip Architecture


L. Mirkarimi, “Hybrid Bonding: Fueling Advanced Memory and High-Performance Compute Roadmaps,” IMAPS Webinar; July 2020.
Key Drivers in Heterogeneous Integration

• Disaggregation is distributing functions onto separate wafers or die

• Advantages:
  • Select optimized Si process and nodes for the particular function
  • Shorter time to market improves flexibility to bring innovative products to the market

• Chiplet Library Menu

<table>
<thead>
<tr>
<th>Circuit Function</th>
<th>Cores</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoC</td>
<td>14nm</td>
<td>I/Os</td>
</tr>
<tr>
<td>FPGA</td>
<td>10 nm</td>
<td>Thermal Budget</td>
</tr>
<tr>
<td>Memory</td>
<td>5 nm</td>
<td>Comms</td>
</tr>
<tr>
<td>Accelerator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sensor Type</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ASIC</td>
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</tr>
</tbody>
</table>

• Cost savings of 2x with chiplet compared to monolithic
• Higher performance over monolithic
• Mixing and matching would allow economies of scale for many companies.

• Challenges at the package level during Re-aggregation
  • Thermal; electrical; reliability performance
  • Interconnect scalability for highly parallel interconnection requires interconnect scaling
Hybrid Bonding and Direct Bond Interconnect (DBI®)

Features

- **Bond Metal**: Cu, Ni
- **Bond Pad Size**: <1μm to 20μm
- **Low Temperature**: ~150 – 400°C
- **Compatible Dielectrics**: SiₓOᵧ, SiₓOᵧNₓ, SiₓCᵧNₓ

Cross Section

- Spontaneous bond between dielectric interface at room temperature
- Metal interconnect forms at elevated temperature, but no external pressure
- Interdiffusion of the metal pads requires time at temperature for metallurgical bond.
Hybrid Bonding Advantages

Hybrid Bonded Module

- **DBI® Ultra Interconnect**
- **Memory Stack**
- **Logic (CPU, GPU, FPGA or SoC)**
- **2.5 D / 3D DBI® Ultra Hybrid Bonding Solutions**

Interconnect Comparison

**Micro-Bump**
- Standoff
- Solder cap
- Cu pillar
- UBM/Barrier
- Active Device Area

**Die 1**
- RDL
- M4

**Die 2**
- RDL
- M4

**Key Challenge**
- Standoff of ~20 um
- UBM Fab… (Masks)
- Underfill
- High Temp Bonding
- >35 um pitch

**Direct Bond Interconnect**
- **When Less is More …**
- Hybrid Bond Interface

**Advantage**
- No Standoff
- No UBM
- No Underfill
- No Heat at Bond
- No Pitch constraints

**More**
- Scalability
- High Throughput Bonding
- Improved Thermal Performance
- Higher Speed Binning Stacks
- Improved Electrical Performance
- Improved Reliability and Yield
- Heterogenous Integration
- Cost Savings
- Flexibility in Architecture
- Path to Chiplet Proliferation
- Uniformity of Packaging Platforms
Hybrid Bonding Advantages

**Hybrid Bonded Module**

- **DBI®**
- **DBI® Ultra**

Memory Stack

DBI Ultra Interconnect

Logic (CPU, GPU, FPGA or SoC)

2.5 D / 3D DBI® Ultra Hybrid Bonding Solutions

**Interconnect Comparison**

**Micro-Bump**

- Die 1
- Die 2
- Solder cap
- Cu pillar
- UBM/Barrier
- Active Device Area
- Standoff

**Key Challenge**

- Standoff of ~20 um
- UBM Fab… (Masks)
- Underfill
- High Temp Bonding
- >35 um pitch

**Direct Bond Interconnect**

- **When Less is More…**

- **More**
  - Scalability
  - High Throughput Bonding
  - Improved Thermal Performance
  - Higher Speed Binning Stacks
  - Improved Electrical Performance
  - Improved Reliability and Yield
  - Heterogenous Integration
  - Cost Savings
  - Flexibility in Architecture
  - Path to Chiplet Proliferation
  - Uniformity of Packaging Platforms

- **Advantage**
  - No Standoff
  - No UBM
  - No Underfill
  - No Heat at Bond
  - No Pitch constraints
Enhanced Electrical and Thermal Performance

**Simulation Comparison**

**TCB-Pad**
- DC Resistance (mOhm): 11.7
- Self-inductance (pH): 2
- Capacitance (fF): 6.1

**DBI-Pad**
- DC Resistance (mOhm): 32.7
- Self-inductance (pH): 25.3
- Capacitance (fF): 141.7

A. Agrawal et al, ECTC 2017

**4-Die Stack Simulation Comparison**

**TCB-Pad**
- HBM—4 Die Stack
- Tj (°C): 67
- ΔT between die (°C): 9

**DBI-Pad**
- HBM—8 Die Stack
- Tj (°C): 59
- ΔT between die (°C): 1
- Forced Convection (3m/s); 25°C

A. Agrawal et al, ECTC 2017

**DBI® Interconnect Advantage in Die Stacks**

- Tj is reduced by 19-25 degrees
- Differential Temperature
  - 1 degree for 4 die stack (9x better)
  - 4 degrees for 8 die stack (7x better)

**DBI® Interconnect Offers**

- 1/50th size of typical TCB pad
- 96% less Capacitance (faster)
- 64% less Resistance (lower DC power)
- 92% less Self-inductance
- Smaller electrical load; less power


**Design Analysis 2D/3D; Hybrid/TCB**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>2D</th>
<th>3D</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock period (ns)</td>
<td>5.5</td>
<td>-0.68%</td>
<td>-13%</td>
</tr>
<tr>
<td>Total Power (mW)</td>
<td>23.5</td>
<td>+20%</td>
<td>+18%</td>
</tr>
<tr>
<td>Area (μm²)</td>
<td>193,600</td>
<td>+10%</td>
<td>-429%</td>
</tr>
</tbody>
</table>

**Hybrid Bond Pads 3D Architectural Advantage**

- Up to 33% Improvement in Power Reduction
- Up to 10% of an Area Improvement over
**DBI® Integration Reduces Process Steps**

**4-Die Stack Test Vehicles**

- Optical Cross Section
- Die 4
- Die 3
- Die 2
- Die 1
- Host

**Interconnects:**
- Face to Face at Die to Host
- Face to Back at Die to Die

**Die-Wafer Level Process Savings**

<table>
<thead>
<tr>
<th>Module Steps</th>
<th>Frontside Process</th>
<th>TSV Side Processing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>UBM Solder</td>
<td>DBI</td>
</tr>
<tr>
<td>1</td>
<td>Passivation opening</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>Lithography</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Adhesion layer, Cu seed layer</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>Cu electroplating</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>Ni electroplating</td>
<td>NO</td>
</tr>
<tr>
<td>6</td>
<td>Solder electroplating</td>
<td>NO</td>
</tr>
<tr>
<td>7</td>
<td>Resist strip</td>
<td>NO</td>
</tr>
<tr>
<td>8</td>
<td>Wet etch (Cu + adhesion layer)</td>
<td>NO</td>
</tr>
<tr>
<td>9</td>
<td>Solder reflow</td>
<td>NO</td>
</tr>
<tr>
<td>10</td>
<td>Cu CMP: NO</td>
<td>Yes</td>
</tr>
</tbody>
</table>

DBI Module Steps = 5 - 1 CMP = 4
TCB Module Steps = 9

DBI Module Steps = 1
TCB Module Steps = 7

**11 Fewer Wafer Process Module Steps for DBI over Solder µBump**

G. Gao et al, ECTC 2020

L. Mirkarimi- Hybrid Bonding for the Next Generation of High-Performance Devices
DBI®Ultra Direct Bond Interconnect Process Flow Schematic

Die to Wafer Hybrid Bonding

BEOL Cu Damascene  Clean/Dice  Activate  Bond  Anneal

DIE PREPARATION

Metal Bond Pad  Silicon Wafer

WAFER 1

Metal Bond Pad  Silicon Wafer

WAFER 2

Chemical Mechanical Polishing

WAFER SURFACE PREPARATION

Chemical Mechanical Polishing

Wafer Activation

Diced Wafer

Tape Frame

Die Activation

Plasma

Die Pick

Flip, Align & Bond

Wafer

Low Temperature Batch Anneal

ROOM TEMPERATURE DIE TO WAFER BONDING

Repeat

Wafer Activation

Die Pick

Plasma

Flip, Align & Bond

Repeat

Low Temperature Batch Anneal

Wafer Activation

Die Pick

Plasma

Flip, Align & Bond

Repeat

Low Temperature Batch Anneal

Wafer Activation

Die Pick

Plasma

Flip, Align & Bond

Repeat

Low Temperature Batch Anneal

Wafer Activation
Technology Demonstrations

• Build test vehicles to demonstrate the technology capability
• Test structures similar to real applications
  • pad diameter
  • pad pitches
  • die dimensions (x,y, and z)
Validated Hybrid Bonding Technology Demonstrations

<table>
<thead>
<tr>
<th>Die Size</th>
<th># Interconnects in Main Chain of Test Vehicle Circuit</th>
<th>Pad Diameter (mm)</th>
<th>Pad Pitch (mm)</th>
<th>Assembly Technology</th>
<th>IO</th>
<th>Reliability Tests</th>
<th># Die Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 x 12</td>
<td>&gt;8,000,000</td>
<td>1.2</td>
<td>2.4</td>
<td>wafer to wafer</td>
<td>Face to Face</td>
<td>Not Tested</td>
<td>1</td>
</tr>
<tr>
<td>1.9 x 1.9</td>
<td>114,920</td>
<td>1.9</td>
<td>3.8</td>
<td>wafer to wafer</td>
<td>Face to Face</td>
<td>Not Tested</td>
<td>1</td>
</tr>
<tr>
<td>8x12</td>
<td>1,600,000</td>
<td>2</td>
<td>4</td>
<td>die to wafer</td>
<td>Face to Face</td>
<td>Planned</td>
<td>1</td>
</tr>
<tr>
<td>8x12</td>
<td>31,000</td>
<td>10 ; 5</td>
<td>40</td>
<td>die to wafer</td>
<td>Face to Face</td>
<td>Completed</td>
<td>1</td>
</tr>
<tr>
<td>8x12</td>
<td>9480</td>
<td>10</td>
<td>38</td>
<td>die to wafer</td>
<td>Face to Face, Face to Back; TSV to DBI</td>
<td>Completed</td>
<td>5</td>
</tr>
</tbody>
</table>

- The size range for a chiplet die (~10mmx10mm)
- DRAM die ~ 8mm x12mm
- TSV pitch ~ 38-40 um
- Logic applications require finer pitch
DBI® Ultra: DBI to DBI and TSV to DBI Memory Test Vehicle Details

- 8 x 12 mm Test Chip
- 2 Layer Metal Pattern: RDL + DBI Bond Pads
- 10 µm pad on 40 µm pitch
- Main Center Array: 50 mm² with 31,356 daisy chain links
- Edge Arrays: 3400 – 5000 links, with links within 200 µm of die edge
- Both 200 mm and 300 mm substrates and component die

Tom Workman et al., IMAPS (March 2020)

- Size: 8.0 mm x 12 mm x 50 µm thickness
- TSV: 5 µm diameter on 35 µm pitch / DBI 15um on 35um pitch
- Main Array: 316 x 30 = 9,480 links
- Right & Left Chains: 316 x 2 = 632 links
- Left Edge Array: 316 x 8 = 2,528 links

G. Gao et al, “ECTC 2021”
### DBI® Ultra Interconnect Reliability Performance

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Condition</th>
<th>Results</th>
<th>Test Condition</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td>-40C to 150C 2000 cycles</td>
<td>Pass</td>
<td>-40C to 125C 2000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>Autoclave</td>
<td>121C, 100%RH, 15PSI, 168hrs</td>
<td>Pass</td>
<td>121C, 100%RH, 15PSI, 168hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Moisture Sensitivity MLS3</td>
<td>24hr prebake+30C/60 %RH 192hrs + 3X Reflow</td>
<td>Pass</td>
<td>24hr prebake+30C/60 %RH 192hrs + 3X Reflow</td>
<td>Pass</td>
</tr>
</tbody>
</table>

- Hybrid Bond Interconnect (DBI) is More Reliable than μbump Interconnect:
  - Enhanced Reliability (all Cu interconnect, no underfill)
  - Enhanced Resistance to Electromigration (all Cu interconnect)
  - Dielectric Hermeticity protection (<10^{-11} atm-cc/s)
DBI® Ultra: DBI to DBI Fine Pitch Logic Test Vehicle

Face to Face Fine Pitch Logic TV

- Size: 8 mm x 12 mm
- 2 μm pad on 4 μm pitch
- 5 Daisy Chain Arrays

<table>
<thead>
<tr>
<th>Array</th>
<th>Area (mm²)</th>
<th>Links</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center Main (DC)</td>
<td>50</td>
<td>1,600k</td>
<td>9 subchains</td>
</tr>
<tr>
<td>Top &amp; Bottom (DCT)</td>
<td>6</td>
<td>190k</td>
<td></td>
</tr>
<tr>
<td>Left (DCL)</td>
<td>8</td>
<td>250k</td>
<td>2 subchains intertwined serpentines</td>
</tr>
<tr>
<td>Right (DCR)</td>
<td>8</td>
<td>125k</td>
<td>2 subchains intertwined serpentines</td>
</tr>
</tbody>
</table>

Experimental Results

- 250°C Anneal; 1.6M interconnects

Lot Void Free (%)
- Lot 1: 95%
- Lot 2: 97%
- Lot 3: 96%

- Fine pitch (2 μm pad); 1.6M interconnects test vehicle yields at 250°C anneal
- High electrical test vehicle yield
  - Even with pad off set of (0.8*Pad Diameter)
  - Similar for both coarse and fine pitch test vehicles
Hybrid Bonding Development Areas in Packaging Industry

- Extending the Die Size Range in Die to Wafer
- Further Reduction of Thermal Budget in Final Anneal
- More Design Flexibility in the Bond Layer Metallization
- Improved Integration for Performance and Cost Reduction
Extending The Hybrid Bonding Technology Demonstration Range

Semiconductor Die Size with Application Space

- Heterogenous Integration
  - LEDs
  - MEMs
  - RF, 5G
  - Lasers
  - Image Sensors
    - NAND
    - DRAM SRAM
    - 3D Chips
    - Chiplets
    - HPC, FPGA

0.1mm² - 1mm² - 10mm² - 100mm² - 900mm²

Feasibility, Yield, Reliability

Multi-Chip Modules

Single Die and Multi-Die Stacking
- 4-die Stack
- 8-die Stack

SoC and Large Die Modules

IMAPS 18th International Conference on DEVICE PACKAGING | March 7-10, 2022 | Fountain Hills, AZ USA
<table>
<thead>
<tr>
<th>Thermal Budget Reduction</th>
<th>DBI Hybrid Bond Layer Innovation</th>
<th>Integration Improvements</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Prior Demonstrations</td>
<td>• DBI Bond Layer Design</td>
<td>• Technology adoption will lead to the ability to innovate with integration</td>
</tr>
<tr>
<td>• 250 and 200C</td>
<td>• CMP Improvement(^4)</td>
<td></td>
</tr>
<tr>
<td>• Industry Wants Lower Temp</td>
<td>• Design Flexibility(^5)</td>
<td>• Availability of this platform technology will unleash the imagination of chip architects.</td>
</tr>
<tr>
<td>• &lt;200C</td>
<td>• Rework: Is it possible?</td>
<td>• Architectural improvements</td>
</tr>
<tr>
<td>• Industry Activity:</td>
<td>• BEOL Materials Innovations</td>
<td>• Die to Die</td>
</tr>
<tr>
<td>• Cu microstructure</td>
<td>• Dielectrics(^6)</td>
<td></td>
</tr>
<tr>
<td>• Nanotwin Cu(^1,2)</td>
<td>• Cu passivation</td>
<td></td>
</tr>
<tr>
<td>• Alternative options</td>
<td>• Metals</td>
<td></td>
</tr>
<tr>
<td>• are being investigated(^3)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. L. Mirkarimi et al, *ECTC* June 2022
5. Theil et al; ECTC, June 2022
7. Gao et al; ECTC, June 2022
Supply Chain Readiness

• How did we get where we are today?
• Industry Activity
# 3DIC Hybrid Bonding: R&D Evolution and HVM Timelines

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>• W2W bonding (&lt;200°C)</td>
<td>• D2W SiO2-SiO2 Interconnect-over the edge</td>
<td>• First DBI D2W Ni DBI</td>
<td>• W2W Cu DBI 2 µm pitch</td>
<td>• Cu D2W HVM D2W Process</td>
<td>• Solving Fundamental Challenges</td>
</tr>
<tr>
<td>• Heterogeneous mm Wave III-V to AlN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Reliability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Fine Pitch D2W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Lower Total Thermal Budgets</td>
</tr>
</tbody>
</table>

## R&D Timeline

- **1998**
  - W2W bonding (<200°C)
  - Heterogeneous mm Wave III-V to AlN
- **2000**
  - D2W SiO2-SiO2 Interconnect-over the edge
- **2005**
  - First DBI D2W Ni DBI
  - 25um pitch
- **2010**
  - W2W Cu DBI 2 µm pitch
- **2015**
  - Cu D2W HVM D2W Process

## Manufacturing Timeline

- **2005**
  - (D2W W2W) Hybrid Bonding
- **2010**
  - BSI-CIS (W2W) Direct Bonding
- **2015**
  - Compute Intensive Modules (2.5 and 3D) (D2W)
- **2020**
  - Licensed ZiBond, DBI and DBI Ultra
  - Licensed DBI Portfolio
- **2025**
  - Professional Integration of DBI Portfolio
Industry Supply Chain Readiness for Hybrid Bonding

✓ Wafer Fabrication Availability
✓ Equipment Availability and Manufacturer Roadmap Alignment
✓ Availability of Metrology Equipment for Process Control

Xperi Working with Key Equipment Vendors Since 2017

Flip Chip Bonder Equipment Vendors with Hybrid Bonding Roadmaps

- Besi
- Kulicke & Soffa
- Süss MicroTec

Metrology and Process Equipment Vendors

- Park Systems
- AXUS Technology
- Lam Research
- Applied Materials
- Veeco
- DISCO
Hybrid Bonding Activity is Increasing in the Industry

<table>
<thead>
<tr>
<th>Semiconductors Company Type</th>
<th>Companies with Hybrid Bonding Activity and/or Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertically Integrated</td>
<td>Sony, Samsung, SK Hynix, Micron, YMTC, Intel, Nanya, Kioxia</td>
</tr>
<tr>
<td>Foundry</td>
<td>UMC, TSMC, Samsung, Global Foundries, Tower Semi</td>
</tr>
<tr>
<td>Foundry+ Assembly</td>
<td></td>
</tr>
<tr>
<td>Fabless</td>
<td>Omnivision, AMD, Meta, Nvidia, Arm, Xilinx, Google</td>
</tr>
<tr>
<td>Government Focused</td>
<td>N’Hanced, Raytheon, Sandia National Labs, Lincoln Labs</td>
</tr>
</tbody>
</table>

Partial list.
Hybrid Bonding Delivering Performance in Next Generation Devices

Hybrid bonding technology is a toolkit enabling the next generation of packaging modules

• **Examples of Widespread Adoption**
  - 1st hybrid-bonded 3D NAND product from YMTC (2020). Wafer to Wafer process.1
  - AMD Ryzen 5000 series CPU with Hybrid Bonding at Computex 2021, Enhanced Performance (~12%) with hybrid bonding equivalent to an entire processing node.2
  - At Connecting Heterogeneous System Summit, Facebook keynote speaker (Facebook AR/VR reality lab) presented hybrid bonding as critical aspect of AR/VR image sensor for pixel level interconnect.3
  - Intel Foveros Direct with an interconnect pitch of 10 um or less to be in production in 2023.4

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2. AMD, Lisa Su, “Computex 2021”
3. Facebook, Barbara De Salvo, Connecting Heterogeneous Systems Summit”, May 2021.
4. Intel, K. Radhakrishnan; “Connecting Heterogeneous Systems Summit”, May, 2021
Summary

• Demonstrated multiple test vehicles with hybrid bonded DBI interconnects have a high yield, enhanced reliability and improved performance over solder μbump.

• Hybrid bonding technology is just beginning to become available in chip to wafer formats in HVM
  • Market adopting at the major pain points
  • Proliferation anticipated across broad segments
  • As more companies access to the DBI toolkit, innovation will follow.

• Hybrid bonding is creating innovation opportunities in SEMI-industry
  • Architecture
  • Materials and Process Integration
  • Assembly Technology
  • Applications and Systems
Thank you for your attention!

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Contact Information: laura.mirkarimi@xperi.com