Heat Dissipation Design of High-Power Wide-Bandgap Power Module with Insulated Metal Substrate

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Abstract

In general, power modules are manufactured as direct bonding copper (DBC) substrates to withstand high temperatures and high power. The DBC substrate has a sandwich structure in which copper layers are formed on upper and lower parts and ceramic is formed as an insulating layer therebetween. Ceramic has excellent insulation properties but is difficult to process and is vulnerable to mechanical stress due to a difference in coefficient of thermal expansion (CTE) between copper. In this regard, research on the development of power modules using various materials is being conducted. In this paper, an insulating metal substrate (IMS) was designed and analyzed using a dielectric film as an insulating layer. IMS substrates are easier to process than ceramics and have a higher CTE, so they are more resistant to mechanical stress than DBC substrates. In addition, it may be made very thin through easy processing, thereby overcoming low thermal conductivity compared to ceramic. In this paper, IMS substrates of various thicknesses were designed based on the easy processability of the dielectric film, and simulations were performed to compare heat dissipation characteristics with Al_2O_3-based DBC substrates.

Key words

Power module, SiC MOSFET, High temperature, FEM

I. Introduction

Recently, in response to global environmental problems and energy saving demands, development of eco-friendly, energy-saving, high-efficiency power semiconductor devices and system technologies for energy saving has become a major issue. Wide band-gap (WBG) devices are attracting attention as the most promising ways to significantly increase energy efficiency and reduce potential power loss by more than 50% as high-efficiency power semiconductor devices [1-3]. Among WBG devices, SiC MOSFET is the most widely used device because its thermal conductivity and high temperature operations are improved compared to Si-based devices. The high thermal conductivity and high-temperature operating performance of SiC MOSFETs have always been an active research topic due to new applications such as automobiles, aircraft, and deep space exploration [3-5]. However, since the operating characteristics of the SiC MOSFET are closely related to heat (e.g., $R_{DS,}$on, Vth), excellent heat dissipation through packaging is required for operational reliability in applications requiring high-temperature operation. The direct bonded copper (DBC) substrate is a conventional power module packaging method. It has a structure in which a ceramic substrate is placed in the center and a copper layer is wrapped in the form of a sandwich in the upper and lower parts. In the industry, three types of ceramic insulator substrates are most frequently used: aluminum nitride (AlN), aluminum oxide (Al_2O_3), and silicon nitride (Si_3N_4). The aluminum nitride substrate has the best thermal conductivity and breakdown voltage characteristics, but is more expensive than the Al_2O_3 substrate, so it is used in designing high-performance power modules. On the other hand, Al_2O_3 substrates are most widely used because they are relatively inexpensive and easy to combine and manufacture metals and ceramics because oxide layers exist on ceramics [6]. Recently, studies on Si_3N_4 substrates excellent in mechanical properties have been actively conducted. In this paper, an insulating metal substrate (IMS) is proposed as an alternative to DBC. The IMS insulates the conductive layer using a dielectric film. The dielectric film has a lower thermal conductivity than the ceramic insulator. However, the main advantage is that the dielectric film can be processed into a very thin layer, enabling conductivity and flexible layer design for the dielectric layer, facilitating the manufacture of

electrical layouts and multi-layer design. In addition, the wide elastic deformation range of the dielectric material is advantageous for reliability problems compared to ceramic insulators [7]. In order to fabricate a high-power module, the dielectric layer must have a high breakdown voltage. In this paper, the breakdown voltage of the IMS dielectric layer is 6KV, which is similar to 5.7KV of Al_2O_3. The various advantages of IMS and the resulting breakdown voltage levels are an attractive solution to replace DBC-based power modules. In this paper, we will design and analyze power modules that can replace Al_2O_3-based DBC by varying the thickness of the dielectric layer of IMS. Thermal analysis will be performed in FEM-based COMSOL MULTIPHYSICS [9] to compare the temperature in the steady state and select the most optimal dielectric layer thickness. The thermal impedance is obtained through transient analysis at an optimal thickness, and this will be implemented as a Foster thermal model. The thermal model created will be verified by designing a full-bridge inverter in Simulink.

II. Simulation

A. FEM & Extract thermal impedance

In this paper, two IMS power modules were compared and analyzed with Al_2O_3-based DBC power modules. In the IMS-based power module, the thickness of the dielectric layer is selected in five types (50μm, 75μm, 100μm, 125μm, 150μm). Fig. 1 shows the 3D model of the power module implemented in COMSOL, and Table I shows the information on each layer of the power module.

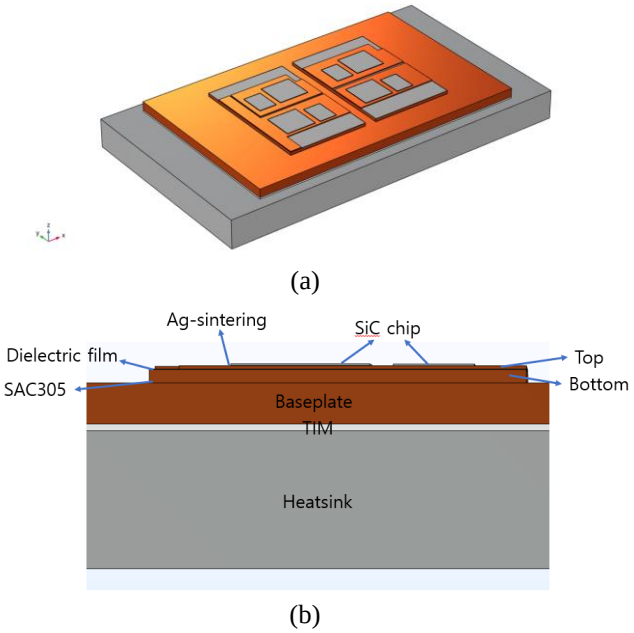


Fig. 1 3D model (a) Power module (b) Cross section (IMS).

Table I. Dimension of power module (IMS and DBC)

Item	Dimension(mm)		
	Width	Length	Thickness
MOSFET	10.43	10.23	0.13
Solder	10.43	10.23	0.05
Copper(Top)	28	43	0.3
Ceramic	28	43	0.635
Dielectric film	28	43	0.05
			0.075
			0.1
			0.125
			0.15
Copper(Bottom) 1)IMS type 2)Ceramic type	28	43	1) 1 2) 0.3

The implemented power module is interpreted through the FEM method. FEM is one of the numerical analysis methods, and it is an analysis method that divides the structure into finite-sized elements and interprets them as a collection of elements. Table II shows the material properties used in the simulation. Materials change their thermal properties depending on the temperature and the effects of free electrons and lattice vibrations [3]. The changing thermal properties are a factor that lowers the accuracy of the simulation. In this paper, the thermal conductivity of SiC chips is set to temperature-dependent.

Table II. Materials property

Item	Materials	Thermal conductivity
Chip	SiC	230 ~ 110
IMS	Dielectric film	3.5
Metal	Cu	401
	Al	238
Solder	Ag-singtering	200
	SAC305	58.7
Ceramic	Al_2O_3	24

Simulations compare IMS substrates to Al_2O_3-based DBC substrates in steady state. The FEM carried out as follows: 1) Sets the initial condition. As a step function, power loss (P_d) was applied to MOS and diodes at 100W and 80W, respectively. In addition, for cooling the power module, the temperature of the heat sink was fixed at 25°C. 2) Assume that all heat flows in the direction of the junction. 3) For optimal thickness, the temperature distribution at various dielectric thicknesses (50μm, 75μm, 100μm, 125μm, 150μm) of IMS was confirmed through parameter sweep and

compared with a DBC substrate. Fig. 2 shows the highest temperature of the IMS substrate MOS by dielectric layer thickness when the steady state is reached. According to the temperature results for the thickness of the dielectric layer, the maximum temperature is 40.65°C at 150μm and the minimum temperature is 36.16°C at 50μm. This shows that the temperature change per dielectric film thickness is 0.0449°C.

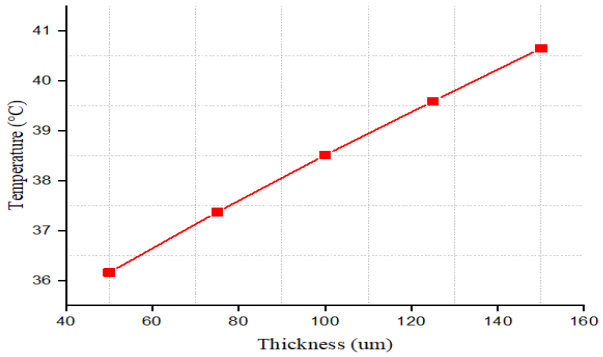
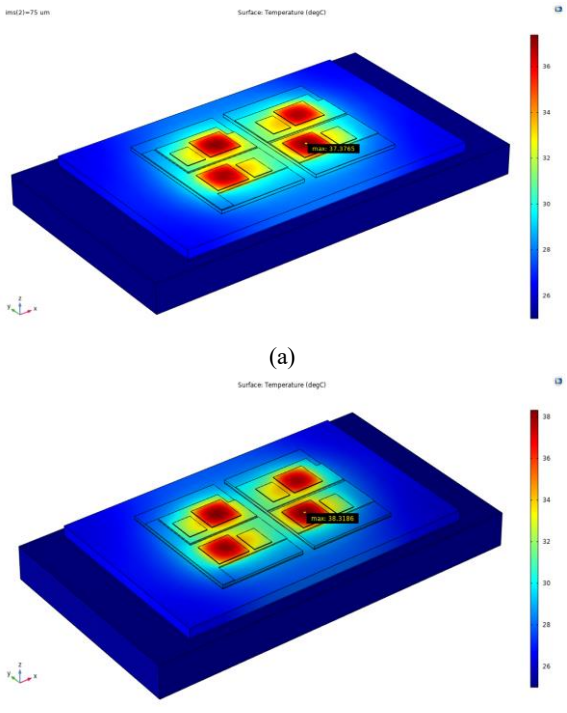


Fig. 2 SiC MOSFET temperature by IMS substrate thickness.

Fig. 3 shows the temperature distribution when steady state is reached for the IMS and DBC substrates. In the dielectric layer (75μm), the MOS temperature of the IMS substrate is 37.37°C and the MOS temperature of the DBC substrate is 38.31°C, with a difference of 0.94°C.



(a)

(b)

Fig. 3 Temperature distribution in steady state (a) IMS substrate (75μm) (b) DBC substrate

Through this, when the thickness of the dielectric layer is thinner than 75um, the heat dissipation characteristic is superior to that of the DBC substrate. If the thickness of the dielectric layer is 50μm, heat dissipation characteristics are good, but if the thickness is too thin, the breakdown voltage is not good, so 75μm (6KV at 75μm) was selected. The optimized IMS power module and DBC power module were analyzed as transient and thermal impedance was extracted. Thermal impedance can be obtained by equation 1.

$$Z_{(t)}^{th} = \frac{T_{j(t)} - T_{a(t)}}{P_d} \qquad (1)$$

To simulate temperature calculations on a circuit simulator (e.g., LTspice, Pspice, Simulink), the thermal impedance curve extracted by the FEM method must be made equivalent thermal resistance (R_{th}) and equivalent thermal capacity (C_{th}). To create an equivalent RC network, fit the thermal impedance curve using mathematical techniques. Equation 2 is the sum of the exponential functions to make the thermal impedance curve an equivalent RC network. Mathematical calculations are performed using the Curved-Fitting Tool (*cftool*) in MATLAB [10].

$$Z_{(t)}^{th} = \sum_{i}^{n} R_{thi} \cdot (1 - e^{-t/\tau_{thi}}) \qquad (2)$$

R_{th} is the equivalent thermal resistance and τ_{th} is the thermal time constant. The equivalent thermal capacity (C_{th}) can be obtained by equation 3.

$$C_{thi} = {}^{\tau_{thi}}/_{R_{thi}} \qquad (3)$$

We express equivalent RC networks using Foster networks. Fig. 4 is a circuit diagram of the Foster network. The range of the number of RC layers is generally 3 to 5 [8], which depends on the accuracy of the thermal impedance and the curved fitting. In this paper, it is composed of three RC layers.

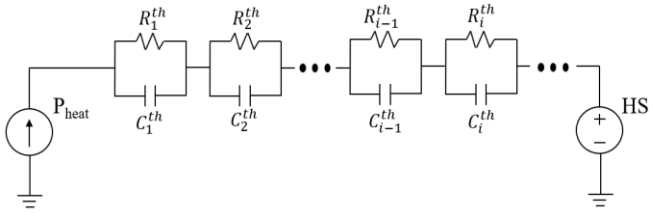


Fig. 4 Foster network

Table III shows the equivalent thermal resistance and time constant values in SiC MOSFET obtained through curved fitting.

Table III. thermal resistance and time constant values

Impedance		Z_{th}		
i		1	2	3
DBC	R_{thi}(K/W)	1.085e-2	0.0514	1.06e-5
	τ_{thi}(s)	0.3244	0.2121	0.1504
IMS	R_{thi}(K/W)	5.507e-2	3.753e-4	1.194e-5
	τ_{thi}(s)	0.1388	0.2595	0.1612

B. Verification

In this paper, Simulink is used to validate the Foster networks of DBC substrates and IMS substrates extracted from FEM. The circuit used for verification is a full-bridge inverter, Fig. 5 is a circuit diagram of the full-bridge inverter, and Table 4 shows the inverter specifications.

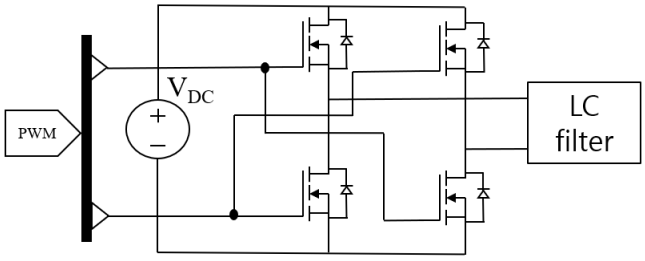


Fig. 5 full-bridge inverter circuit diagram

Table 4: Verification circuit specification

DC voltage (V_{dc})	1200 V
Output Voltage (V_{out})	565.6 V rms
Output Current (I_{out})	56.56 A rms
Power (P)	32 KW
Duty Cycle (D)	0.5
Switching frequency (fs)	5 KHz

Fig. 6 is a schematic diagram of Simulink for the entire system used for verification. To create the same boundary conditions as the FEM simulation, the external temperature (Ta) was set to 25 °C. The simulation time ran until the chip temperature reached a steady state. Fig. 7 shows the Simulink simulation results. When both substrates are in thermal equilibrium, the DBC substrates has a temperature of 375K (101.85°C) and the IMS substrates is 368K (94.85°C). From the circuit simulator results, it can be seen that the temperature decreased by about 7°C when the IMS substrates was applied. Finally, the Foster network obtained from FEM was compared with Simulink to check if it was accurate. An IMS substrates was used for verification, and a total power loss of 670W generated from a full-bridge inverter was applied as a heat source. Fig. 8 shows the temperature results of the FEM when thermal equilibrium is reached. In the results, there is a small difference of about 0.15 °C between the two simulations.

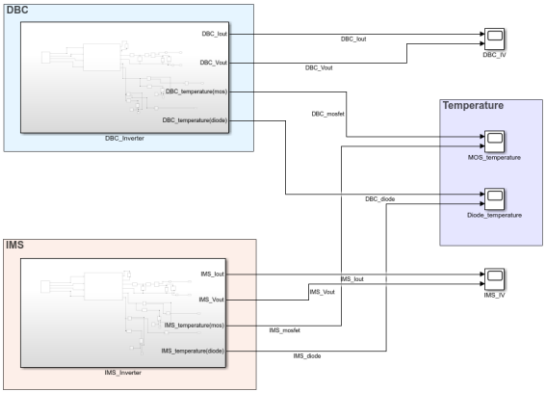


Fig. 6 Diagram of Simulink for the entire system.

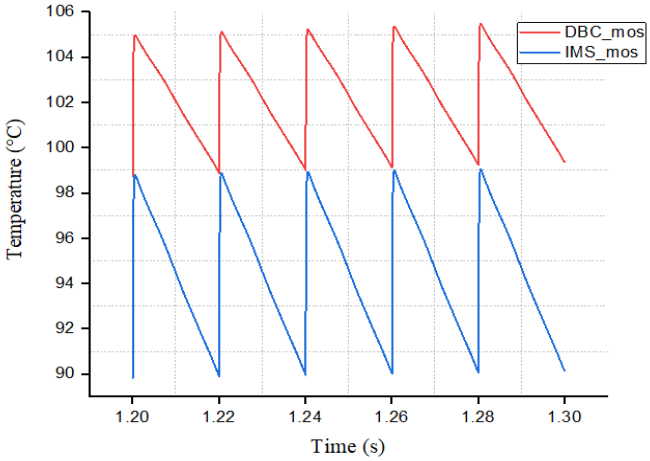


Fig. 7 Simulink simulation results.

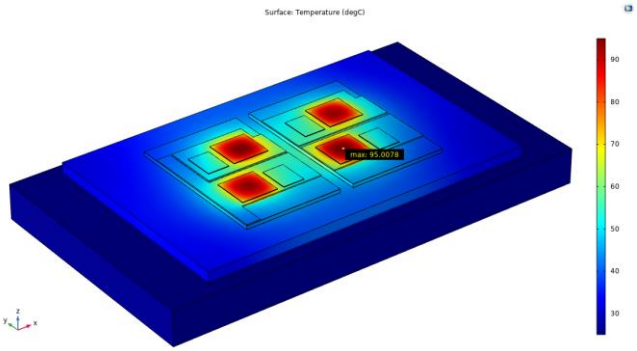


Fig. 8 The FEM simulation result for Foster network verification is 95°C.

III. Conclusion

In this paper, we propose a power module based on IMS substrates rather than a power module based on DBC substrates that are generally used. IMS substrates are highly

resistant to CTE mismatch caused by DBC substrates by using dielectric films as insulating layers. In addition, it is possible to process with a very thin thickness compared to ceramics through easy process difficulty. By varying the thickness of the dielectric film in the FEM simulation, a dielectric film thickness with similar heat dissipation characteristics compared to Al_2O_3-based DBC substrates was selected. After that, the thermal impedance curve was obtained and the Foster network was implemented through the curved-fitting process in MATLAB *cftool*. The temperature difference between DBC substrates and IMS substrates was verified by implementing a full-bridge inverter in Simulink. As a result, it was confirmed that the IMS substrates presented in this paper had a lower temperature of 7°C compared to DBC substrates when the dielectric film thickness was 75um. Additionally, by comparing the results of Simulink and FEM, it was confirmed that the Foster network extracted from FEM was properly extracted, and almost the same result was obtained with a low temperature difference of about 0.15°C. In conclusion, the IMS substrates-based power module proposed in this paper has good heat dissipation characteristics compared to the DBC substrates-based power module.

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References

[1] José. M, “A survey of wide bandgap power semiconductor devices”, *IEEE Trans Power Electron*., 29(5), 2155-2163, May 2014.
[2] Xu. S, “Review of silicon carbide power devices and their applications”, *IEEE Transactions on Industrial Electronics*., 64(10), 8193-8205, October 2017.
[3] Mengxing. C, “Thermal characterization of silicon carbide MOSFET module suitable of high-temperature computationally efficient thermal-profile prediction”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*., 9(4), 3947-3958, August 2021.
[4] Jacek. R, “Silicon carbide power transistors: A new era in power electronics is initiated,*” IEEE Ind. Electron. Mag*., 6(2), 17–26, Jun. 2012.
[5] A. O. Adan, “The current status and trends of 1,200-V commercial silicon-carbide MOSFETs: Deep physical analysis of power transistors from a Designer’s perspective,” *IEEE Power Electron. Mag*., 6(2), 36–47, Jun. 2019.
[6] Emre. G, “Graphite-embedded high-performance insulated metal substrate for wide-bandgap power modules”, *IEEE Transactions on Power Electronics*., 36(1), 114-128, January 2021.
[7] Lutz. J, “Semiconductor Power Devices: Physics, Characteristics, Reliability”, Springer, Berlin/Heidelberg.
[8] Krzysztof. G, “Compact Thermal Models of Semiconductor Devices – a Review”, INTL Journal of Electronics and Telecommunications., 2019, VOL. 65, NO.2 , PP. 151-158
[9] COMSOL Multiphysics (altsoft.co.kr)
[10] www.mathworks.com