High temperature operation of β-Ga_2O_3 transistors

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Abstract

We studied the application of β-Ga_2O_3 for high temperature operation up to 500 ºC. Field effect transistors were fabricated using epitaxial films grown on insulating β-Ga_2O_3 substrates. Variable temperature DC measurements were performed in vacuum and air ambient. Measurements revealed a reduction in on/off ratio for the devices due to increase in thermionic emission over the gate/dielectric barrier of MOSFET and over the gate/semiconductor barrier of MESFET. Devices also exhibited detrapping of electrons from interface traps with the increase in temperature. After the devices were tested intermittently at different high temperatures in vacuum or in air ambient, suggesting no change in semiconductor and contact properties.

Key words

β-Ga_2O_3, MOSFET, temperature, vacuum, air.

I. Introduction

High temperature (HT) electronics capability is desirable for extreme environment operations, where minimal active cooling impacts size, weight, power, and cost (SWaP-C) design considerations immensely. Conventional Si-based technology cannot operate at temperatures above 200 ºC. Therefore, Si-based electronics are either operated remotely by placing them away from the hot-sections of a system or by cooling the electronic components using air or liquid – both these thermal management solutions introduce additional overhead. Moreover, intrinsic carrier concentration in silicon is very high at high temperature (Fig. 1), which makes it difficult to modulate the semiconductor material in a transistor configuration. These motivated researchers to explore the usefulness of wide bandgap semiconductor materials (such as SiC [1], III-N compounds [2-3], β-Ga_2O_3 [4], diamond [5]) at HT.

II. Ga_2O_3 as a HT electronic option

Devices for HT electronics need to use materials (semiconductors, dielectrics, metals) that have high melting point and no phase transitions. There also needs to be no inter-mixing between different materials when devices are operated at a high temperature. Semiconductor material used in HT electronics should also have low intrinsic carrier density, low activation energy for dopants, which makes the transistor easier to modulate at high temperature. In addition, the devices will need to operate maintaining a stable performance over time and will need to be robust against harsh environments.

Table 1 lists different HT relevant parameters for different semiconductors. Among them, SiC offers the most matured HT electronic device technology [1]. Advancement technologies are however desirable using ultra-wider bandgap (UWBG) semiconductors like Ga_2O_3, diamond, AlN that will enable a higher voltage operation. Among these option, β-Ga_2O_3 is preferred as it offers a high melting point, a large bandgap, a low intrinsic carrier concentration, a large experimentally demonstrated breakdown voltage, a low activation energy for donors, and a reasonable mobility. The low thermal conductivity of β-Ga_2O_3 is not concern for power switching applications. Even for higher power applications, heat extraction is a general engineering problem for any UWBG semiconductor and can be solved by wafer thinning or by localized heat extraction on which many groups are working on [6]. *Most importantly,* β-Ga_2O_3 is the only UWBG material that can be grown from melt and processed into 2-4" wafers. The availability of melt-growth process at a very high purity is expected to reduce the wafer cost significantly to almost one-fifth of SiC [7].

Therefore, when compared with GaN on SiC, the cost advantage is even higher. Other than this cost advantage, availability of large size wafers have already enabled demonstration of transistors and diodes in wafer scale and allowed very rapid advancement in device performances within the last decade [8-11].

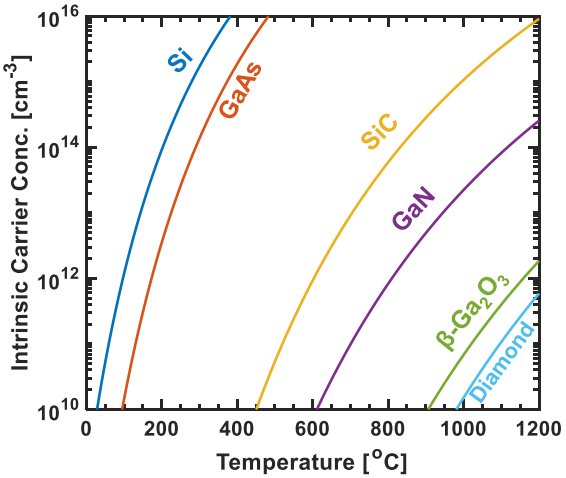

Fig. 1: Calculated intrinsic carrier concentration at different temperature for different semiconductors.

TABLE 1: SUMMARY OF MATERIALS PARAMETERS RELEVANT FOR HT ELECTRONICS FOR DIFFERENT SEMICONDUCTORS

Materials	T_{melt} [°C]	E_G [eV]	E_{BD} [MV/cm]	$E_{D,ac}$ [meV]	μ @RT (cm^2/Vs)	κ [W/cm/K]
Si	1410	1.1	0.3	45	1400	1.5
GaAs	1238	1.4	0.4	6	8000	0.5
4H-SiC	2730	3.3	2.5	60	1000	2.7
GaN	2500	3.4	3	20	2000	2.1
Ga_2O_3	**1900**	**4.8**	**5.5**	**30**	**150**	**0.1-0.3**
Diamond	4027	5.5	1.7	370	200	23-35
AlN	2200	6.2	2.1	280	245	3.4

Note: The table lists measured values

III. Device details

We fabricated two types of devices for studying the HT compatibility of β-Ga_2O_3. The first type of device was a MOSFET (see Fig. 2a for a cross-sectional schematic) fabricated on a (010) Fe-doped Ga_2O_3 substrate using 65 nm, Si-doped Ga_2O_3 channel (doping density ~ 10^{18} cm^{-3}) layer grown by molecular beam epitaxy (MBE) located at the Materials and Manufacturing Directorate of the Air Force Research Laboratory (AFRL). The device had ~26 nm Al_2O_3 gate dielectric deposited using plasma enhanced atomic layer deposition (PE-ALD), Ni/Au gate, ~80 nm of PE-ALD Al_2O_3 passivation. The device dimensions were as follows: gate width W_G ~ 150 μm, gate length L_G ~ 0.7 μm, source-drain length L_{SD} ~7.5 μm, gate-source length L_{GS} ~ 1.4 μm, and gate-drain length L_{GD} ~ 5.4 μm.

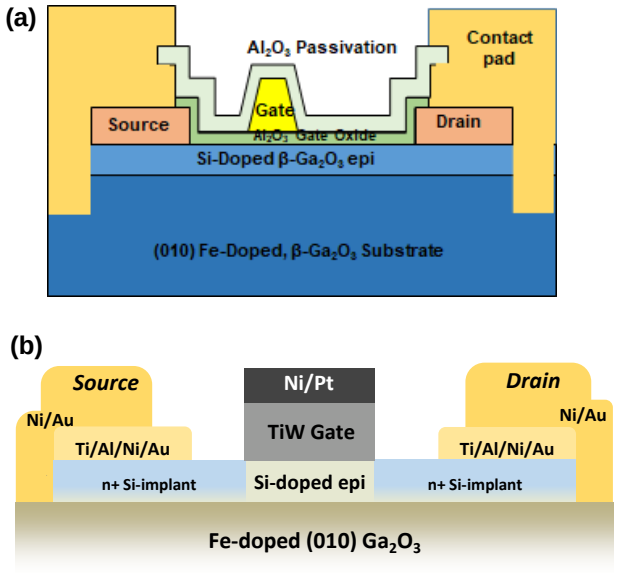

Fig. 2: (a) A cross-sectional schematic of the β-Ga_2O_3 MOSFET. The device is fabricated on a (010) Fe-doped Ga_2O_3 substrate using a Si-doped Ga_2O_3 channel layer grown by MBE. The device used Al_2O_3 as gate oxide, Ni/Au as gate and annealed Ti/Al/Ni/Au as source/drain. (b) A cross-sectional schematic of the β-Ga_2O_3 MESFET fabricated on a (010) Fe-doped Ga_2O_3 substrate using 125 nm Si-doped ($2x10^{17}$ cm^{-3}) Ga_2O_3 channel layer grown using metalorganic vapor phase epitaxy. The device used TiW as gate and annealed Ti/Al/Ni/Au formed on an ion implanted region as source/drain.

The second type of device was a MESFET (see Fig. 2b for a cross-sectional schematic) which was also fabricated on a (010) Fe-doped Ga_2O_3 substrate using 125 nm, $2x10^{17}$ cm^{-3} Si-doped Ga_2O_3 channel grown by metal-organic vapor-phase epitaxy (MOVPE) at Leibniz-Institut für Kristallzüchtung, Berlin, Germany. The device used a TiW gate metal defined with RIE by using Ni/Pt as the hard mask. Self-aligned source/drain regions were implanted with 5 x 10^{19} cm^{-3} Si. Metal interconnects were later formed in the source/drain regions to complete device fabrication. The device parameters were: W_G ~ 50 μm and L_G ~ 1.6 μm.

IV. HT test setup

Devices were tested using two types of systems. One was a vacuum probe station, which was purchased from microXact, Inc. and located at the University of Illinois. The other one was a custom-made system at AFRL, where devices are tested in an air ambient by first packaging a sample containing multiple device on

an alumina substrate with Au contact pads and then wire bonding one device from the sample to Au pads (see Fig. 3b). The device was then placed inside a box furnace that permits electrical connection capabilities using externally accessible, electromagnetically shielded wires (see Fig. 3a). Test temperature was measured using a 100 Ω Pt resistance temperature detector (RTD). During both vacuum and air ambient testing, devices were tested from RT to 500 °C using 50-100 °C temperature intervals.

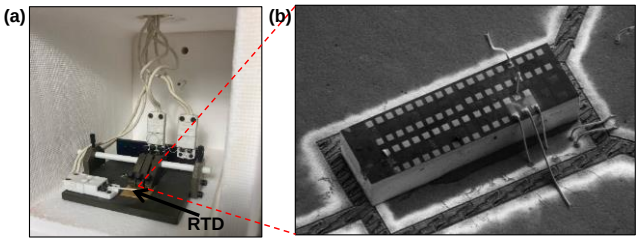

Fig. 3: (a) An image of the HT air ambient setup showing the resistance temperature detector (RTD) used for measuring temperature. **(c)** A scanning electron microscopy (SEM) image of the packaged chip where source, drain and gate of a transistor were connected to three Au contact pads.

V. HT test results

Figs. 4a-d show output (I_{DS}-V_{DS}) characteristics of a MOSFET measured at RT and at 500 °C in vacuum and air ambient. The current in the device increases from its RT value when device was test at 500 °C. This is due to activation carriers from interface traps present within the device [4]. The detrapping of electrons from interface traps resulted in a reduction in the threshold voltage and an increase in the drain current as the devices were tested at higher temperatures.

For the 500 °C data collected in air ambient (Fig. 4d), the device lost its modulation because of the diffusion of Ni into Au and Al_2O_3. Extracted on-resistance (R_{on}) from the output characteristics allowed calculation of series resistance (R_{sr}) for the device at different temperatures (data not shown). The data suggested an ease of conduction through the S/D Schottky contact up to 300 °C; at higher temperatures, R_{st} slightly increase potentially because of the diffusion of Ni mentioned before.

The MESFET devices also showed similar behavior when test was performed in vacuum. However, when HT test was performed in air, the MESFET showed stable operation up to 450 °C. Beyond that temperature, the device properties degraded potentially because of the lack of passivation for the MESFET (see Fig. 2b). In comparison, MOSFET had Al_2O_3 passivation (see Fig. 2a) and showed stable device operation at 500 °C in air (see Fig. 4d).

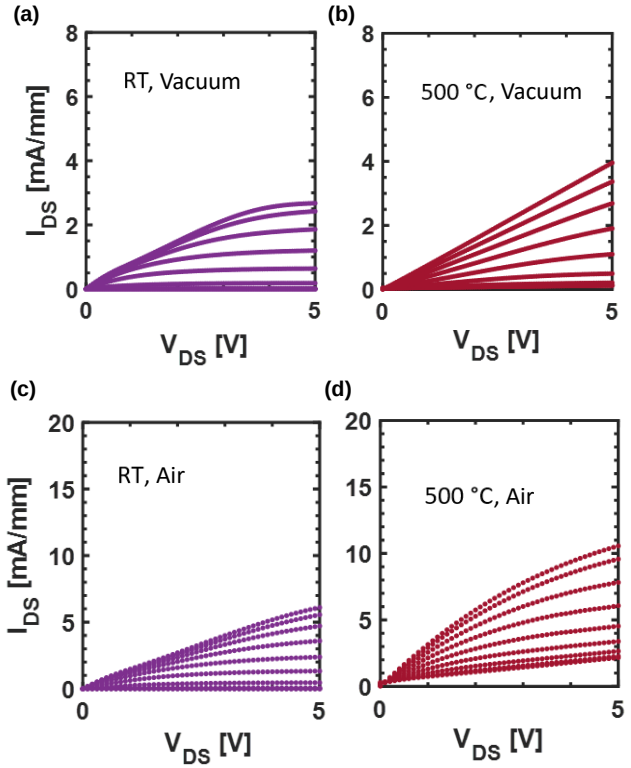

Fig. 4: I_{DS}-V_{DS} characteristics of a MOSFET measured using V_{GS} = -10 to 0V at – (a) room temperature (RT) in vacuum, (b) 500 °C in vacuum, (c) RT in air ambient, (b) 500 °C in air ambient.

After the completion of HT performed for 8-20 hours, both MESFETs and MOSFETs device characteristics recovered. MESFET parameters remained unchanged, while MOSFETs showed slight reduction in its threshold voltage and reduction in gate modulation due to Ni diffusion.

VI. Conclusion

High temperature operation of β-Ga_2O_3 MOSFET and MESFET devices were studied from room temperature up to 500 °C in vacuum and in air ambient. Variable temperature measurements revealed a reduction gate control of the device due to increase in thermionic emission and increase in current due to detrapping of electrons from interface traps with the increase in temperature. Devices characteristics recovered after extended period of high temperature testing both in vacuum and in air, suggesting no change in semiconductor and contact properties. Our results suggest that with appropriate choice of metals, gate dielectrics and passivation the 500 °C operation using β-Ga_2O_3 has no bottlenecks.

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References

[1] P. G. Neudeck, L. Chen, R. D. Meredith, D. Lukco, D. J. Spry, L. M. Nakley and G. W. Hunter, "Operational Testing of 4H-SiC JFET ICs for 60 Days Directly Exposed to Venus Surface Atmospheric Conditions", IEEE Journal of the Electron Devices Society **7**, 100-110 (2019).

[2] P. H. Carey, F. Ren, A. G. Baca, B. A. Klein, A. A. Allerman, A. M. Armstrong, E. A. Douglas, R. J. Kaplar, P. G. Kotula and S. J. Pearton, "Operation Up to 500 °C of Al0.85Ga0.15N/Al0.7Ga0.3N High Electron Mobility Transistors", IEEE Journal of the Electron Devices Society 7, 444-452 (2019);

[3] M. Hiroki, Y. Taniyasu and K. Kumakura, "High-Temperature Performance of AlN MESFETs With Epitaxially Grown n-Type AlN Channel Layers", IEEE Electron Device Letters 43 (3), 350-353 (2022).

[4] H. Bae, T. J. Park, J. Noh, W. Chung, M. Si, S. Ramanathan and P. D. Ye, "First demonstration of robust tri-gate β-Ga_2O_3 nano-membrane field-effect transistors", Nanotechnology **33** (12), 125201 (2021).

[5] T. Iwasaki, Y. Hoshino, K. Tsuzuki, H. Kato, T. Makino, M. Ogura, D. Takeuchi, H. Okushi, S. Yamasaki and M. Hatano, "High-Temperature Operation of Diamond Junction Field-Effect Transistors With Lateral p-n Junctions", IEEE Electron Device Letters **34** (9), 1175-1177 (2013).

[6] Z. Cheng, J. Shi, C. Yuan, S. Kim and S. Graham, "Chapter Four - Thermal science and engineering of β-Ga2O3 materials and devices", in *Semiconductors and Semimetals*, edited by Y. Zhao and Z. Mi (Elsevier, 2021), Vol. 107, pp. 77-99.

[7] S. B. Reese, T. Remo, J. Green and A. Zakutayev, "How Much Will Gallium Oxide Power Electronics Cost?", Joule **3** (4), 903-907 (2019).

[8] G. Jessen, "Gallium Oxide: The Supercharged Semiconductor", IEEE Spectrum, 24 Mar 2021.

[9] A. J. Green, J. Speck, G. Xing, P. Moens, F. Allerstam, K. Gumaelius, T. Neyer, A. Arias-Purdue, V. Mehrotra, A. Kuramata, K. Sasaki, S. Watanabe, K. Koshi, J. Blevins, O. Bierwagen, S. Krishnamoorthy, K. Leedy, A. R. Arehart, A. T. Neal, S. Mou, S. A. Ringel, A. Kumar, A. Sharma, K. Ghosh, U. Singisetti, W. Li, K. Chabak, K. Liddy, A. Islam, S. Rajan, S. Graham, S. Choi, Z. Cheng and M. Higashiwaki, "β-Gallium oxide power electronics", APL Materials **10** (2), 029201 (2022).

[10] K. D. Chabak, K. D. Leedy, A. J. Green, S. Mou, A. T. Neal, T. Asel, E. R. Heller, N. Hendricks, K. J. Liddy, A. Crespo, N. C. Miller, M. T. Lindquist, N. A. Moser, R. C. Fitch, D. E. Walker, D. L. Dorsey, G. H. Jessen, "Lateral β-Ga_2O_3 field effect transistors", Semiconductor Science and Technology, 2019, p. 013002;

[11] M. Higashiwaki, "β-Gallium oxide devices: Progress and outlook", physica status solidi (RRL) – Rapid Research Letters **15**, 2100357 (2021).