High temperature operation of $\beta$-Ga$_2$O$_3$ transistors

Ahmad E. Islam, Nicholas P. Sepelak, Kyle J. Liddy, Rachel Kahler, Jeremiah Williams, Daniel M. Dryden, Andrew J. Green, and Kelson D. Chabak

1 Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, Dayton, OH 45433, United States
2 KBR, Inc., Beavercreek, OH 45431, United States

Email: ahmad.islam.2@af.mil, ahmad.islam.2@afrl.af.mil

Abstract

We studied the application of $\beta$-Ga$_2$O$_3$ for high temperature operation up to 500 °C. Field effect transistors were fabricated using epitaxial films grown on insulating $\beta$-Ga$_2$O$_3$ substrates. Variable temperature DC measurements were performed in vacuum and air ambient. Measurements revealed a reduction in on/off ratio for the devices due to increase in thermionic emission over the gate/dielectric barrier of MOSFET and over the gate/semiconductor barrier of MESFET. Devices also exhibited detrapping of electrons from interface traps with the increase in temperature. After the devices were tested intermittently at different high temperatures in vacuum or in air ambient, suggesting no change in semiconductor and contact properties.

Key words
$\beta$-Ga$_2$O$_3$, MOSFET, temperature, vacuum, air.

I. Introduction

High temperature (HT) electronics capability is desirable for extreme environment operations, where minimal active cooling impacts size, weight, power, and cost (SWaP-C) design considerations immensely. Conventional Si-based technology cannot operate at temperatures above 200 °C. Therefore, Si-based electronics are either operated remotely by placing them away from the hot-sections of a system or by cooling the electronic components using air or liquid – both these thermal management solutions introduce additional overhead. Moreover, intrinsic carrier concentration in silicon is very high at high temperature (Fig. 1), which makes it difficult to modulate the semiconductor material in a transistor configuration. These motivated researchers to explore the usefulness of wide bandgap semiconductor materials (such as SiC [1], III-N compounds [2-3], $\beta$-Ga$_2$O$_3$ [4], diamond [5]) at HT.

II. Ga$_2$O$_3$ as a HT electronic option

Devices for HT electronics need to use materials (semiconductors, dielectrics, metals) that have high melting point and no phase transitions. There also needs to be no inter-mixing between different materials when devices are operated at a high temperature. Semiconductor material used in HT electronics should also have low intrinsic carrier density, low activation energy for dopants, which makes the transistor easier to modulate at high temperature. In addition, the devices will need to operate maintaining a stable performance over time and will need to be robust against harsh environments.

Table 1 lists different HT relevant parameters for different semiconductors. Among them, SiC offers the most matured HT electronic device technology [1]. Advancement technologies are however desirable using ultra-wider bandgap (UWBG) semiconductors like Ga$_2$O$_3$, diamond, AlN that will enable a higher voltage operation. Among these option, $\beta$-Ga$_2$O$_3$ is preferred as it offers a high melting point, a large bandgap, a low intrinsic carrier concentration, a large experimentally demonstrated breakdown voltage, a low activation energy for donors, and a reasonable mobility. The low thermal conductivity of $\beta$-Ga$_2$O$_3$ is not concern for power switching applications. Even for higher power applications, heat extraction is a general engineering problem for any UWBG semiconductor and can be solved by wafer thinning or by localized heat extraction on which many groups are working on [6]. Most importantly, $\beta$-Ga$_2$O$_3$ is the only UWBG material that can be grown from melt and processed into 2-4” wafers. The availability of melt-growth process at a very high purity is expected to reduce the wafer cost significantly to almost one-fifth of SiC [7].
Therefore, when compared with GaN on SiC, the cost advantage is even higher. Other than this cost advantage, availability of large size wafers have already enabled demonstration of transistors and diodes in wafer scale and allowed very rapid advancement in device performances within the last decade [8-11].

Fig. 1: Calculated intrinsic carrier concentration at different temperature for different semiconductors.

![Graph showing intrinsic carrier concentration vs. temperature for different semiconductors](image)

**Table 1: Summary of Materials Parameters Relevant for HT Electronics for Different Semiconductors**

<table>
<thead>
<tr>
<th>Materials</th>
<th>$T_{mel}$ [°C]</th>
<th>$E_g$ [eV]</th>
<th>$E_{gap}$ [MV/cm]</th>
<th>$E_{001}$ [meV]</th>
<th>$\mu$ [cm²/Vs]</th>
<th>$\kappa$ [W/cm•K]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1410</td>
<td>1.1</td>
<td>0.3</td>
<td>45</td>
<td>1400</td>
<td>1.5</td>
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<tr>
<td>GaAs</td>
<td>1238</td>
<td>1.4</td>
<td>0.4</td>
<td>6</td>
<td>8000</td>
<td>0.5</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>2730</td>
<td>3.3</td>
<td>2.5</td>
<td>60</td>
<td>1000</td>
<td>2.7</td>
</tr>
<tr>
<td>GaN</td>
<td>2500</td>
<td>3.4</td>
<td>3</td>
<td>20</td>
<td>2000</td>
<td>2.1</td>
</tr>
<tr>
<td>Ga$_2$O$_3$</td>
<td>1900</td>
<td>4.8</td>
<td>5.5</td>
<td>30</td>
<td>150</td>
<td>0.1-0.3</td>
</tr>
<tr>
<td>Diamond</td>
<td>4027</td>
<td>5.5</td>
<td>1.7</td>
<td>370</td>
<td>200</td>
<td>23-35</td>
</tr>
<tr>
<td>AlN</td>
<td>2000</td>
<td>6.2</td>
<td>2.1</td>
<td>280</td>
<td>245</td>
<td>3.4</td>
</tr>
</tbody>
</table>

Note: The table lists measured values.

**III. Device Details**

We fabricated two types of devices for studying the HT compatibility of β-Ga$_2$O$_3$. The first type of device was a MOSFET (see Fig. 2a for a cross-sectional schematic) fabricated on a (010) Fe-doped Ga$_2$O$_3$ substrate using 65 nm, Si-doped Ga$_2$O$_3$ channel (doping density ~ $10^{18}$ cm$^{-3}$) layer grown by molecular beam epitaxy (MBE) located at the Materials and Manufacturing Directorate of the Air Force Research Laboratory (AFRL). The device had ~26 nm Al$_2$O$_3$ gate dielectric deposited using plasma enhanced atomic layer deposition (PE-ALD), Ni/Au gate, ~80 nm of PE-ALD Al$_2$O$_3$ passivation. The device dimensions were as follows: gate width $W_G$ ~ 150 µm, gate length $L_G$ ~ 0.7 µm, source-drain length $L_{SD}$ ~ 7.5 µm, gate-source length $L_{GS}$ ~ 1.4 µm, and gate-drain length $L_{GD}$ ~ 5.4 µm.

![Cross-sectional schematic of the β-Ga$_2$O$_3$ MOSFET.](image)

**Fig. 2:** (a) A cross-sectional schematic of the β-Ga$_2$O$_3$ MOSFET. The device is fabricated on a (010) Fe-doped Ga$_2$O$_3$ substrate using a Si-doped Ga$_2$O$_3$ channel layer grown by MBE. The device used Al$_2$O$_3$ as gate oxide, Ni/Au as gate and annealed Ti/Al/Ni/Au as source/drain. (b) A cross-sectional schematic of the β-Ga$_2$O$_3$ MESFET fabricated on a (010) Fe-doped Ga$_2$O$_3$ substrate using 125 nm Si-doped (2x10$^{17}$ cm$^{-3}$) Ga$_2$O$_3$ channel layer grown using metalorganic vapor phase epitaxy. The device used TiW as gate and annealed Ti/Al/Ni/Au formed on an ion implanted region as source/drain.

The second type of device was a MESFET (see Fig. 2b for a cross-sectional schematic) which was also fabricated on a (010) Fe-doped Ga$_2$O$_3$ substrate using 125 nm, 2x10$^{17}$ cm$^{-3}$ Si-doped Ga$_2$O$_3$ channel grown by metal-organic vapor-phase epitaxy (MOVPE) at Leibniz-Institut für Kristallzüchtung, Berlin, Germany. The device used a TiW gate metal defined with RIE by using Ni/Pt as the hard mask. Self-aligned source/drain regions were implanted with 5 x $10^{19}$ cm$^{-3}$ Si. Metal interconnects were later formed in the source/drain regions to complete device fabrication. The device parameters were: $W_G$ ~ 50 µm and $L_G$ ~ 1.6 µm.

**IV. HT Test Setup**

Devices were tested using two types of systems. One was a vacuum probe station, which was purchased from microXact, Inc. and located at the University of Illinois. The other one was a custom-made system at AFRL, where devices are tested in an air ambient by first packaging a sample containing multiple device on
an alumina substrate with Au contact pads and then wire bonding one device from the sample to Au pads (see Fig. 3b). The device was then placed inside a box furnace that permits electrical connection capabilities using externally accessible, electromagnetically shielded wires (see Fig. 3a). Test temperature was measured using a 100 Ω Pt resistance temperature detector (RTD). During both vacuum and air ambient testing, devices were tested from RT to 500 °C using 50-100 °C temperature intervals.

**V. HT test results**

Figs. 4a-d show output (I DS-V DS) characteristics of a MOSFET measured at RT and at 500 °C in vacuum and air ambient. The current in the device increases from its RT value when device was test at 500 °C. This is due to activation carriers from interface traps present within the device [4]. The detrapping of electrons from interface traps resulted in a reduction in the threshold voltage and an increase in the drain current as the devices were tested at higher temperatures.

For the 500 °C data collected in air ambient (Fig. 4d), the device lost its modulation because of the diffusion of Ni into Au and Al2O3. Extracted on-resistance (R on) from the output characteristics allowed calculation of series resistance (R s) for the device at different temperatures (data not shown). The data suggested an ease of conduction through the S/D Schottky contact up to 300 °C; at higher temperatures, R s slightly increase potentially because of the diffusion of Ni mentioned before.

The MESFET devices also showed similar behavior when test was performed in vacuum. However, when HT test was performed in air, the MESFET showed stable operation up to 450 °C. Beyond that temperature, the device properties degraded potentially because of the lack of passivation for the MESFET (see Fig. 2b). In comparison, MOSFET had Al2O3 passivation (see Fig. 2a) and showed stable device operation at 500 °C in air (see Fig. 4d).

After the completion of HT performed for 8-20 hours, both MESFETs and MOSFETs device characteristics recovered. MESFET parameters remained unchanged, while MOSFETs showed slight reduction in its threshold voltage and reduction in gate modulation due to Ni diffusion.

**VI. Conclusion**

High temperature operation of β-Ga2O3 MOSFET and MESFET devices were studied from room temperature up to 500 °C in vacuum and in air ambient. Variable temperature measurements revealed a reduction gate control of the device due to increase in thermionic emission and increase in current due to detrapping of electrons from interface traps with the increase in temperature. Devices characteristics recovered after extended period of high temperature testing both in vacuum and in air, suggesting no change in semiconductor and contact properties. Our results suggest that with appropriate choice of metals, gate dielectrics and passivation the 500 °C operation using β-Ga2O3 has no bottlenecks.
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References


