Direct Write Extreme Environment Packaging

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Abstract

There is growing interest in extreme temperature electronics to support instrumentation for sensors at temperatures beyond the normal range of electronics. Reliable packaging in the temperature range of more than 300°C has been demonstrated using ceramic multi-chip modules using conventional hybrid circuit technology. This approach typically requires high NRE costs and lead time. Additive manufacturing processes of metals, ceramics, conductors, and dielectrics provides a digital transformation of hybrid circuit manufacturing technology that reduces time and cost for packaging with the added benefits of novel 3D structures and embedded features. Silicon carbide devices have been demonstrated to operate above 300C which requires capable interconnects. This report presents the results of testing to characterize important electrical and mechanical properties of additively manufactured packaging materials (substrates, conductor, dielectrics) and die interconnect methods capable for operation above 300 °C. Characterization of thick film materials were tested for resistance, SIR, and adhesion stability on 96% alumina, 98.4% additively printed alumina, and Corning alumina ribbon ceramic at 300, 500, and 750°C. Methods for direct write interconnects were developed and tested at 300 and 500C for resistance stability and thermal shock. The methods are direct write surface interconnects, embedded interconnects using additive alumina substrates, and flip chip. Reliability testing results, a test method for insitu measurement, and demonstrations using the materials are presented.

Key words

Additive electronics, high temperature packaging, reliability

I. Introduction

There is growing interest in extreme temperature electronics to support instrumentation for sensors at temperatures beyond the normal range of electronics. Reliable high temperature packaging for 300°C has been demonstrated using ceramic multi-chip modules using conventional screen printed hybrid circuit technology [1,2]. This approach typically requires high NRE costs and lead time. Additive manufacturing processes of ceramics, conductors, and dielectrics provides a digital transformation of hybrid circuit manufacturing technology that reduces time, waste, and cost packaging for prototypes with the added benefits of novel 3D structures and embedded features.

GE Research and Binghamton University have demonstrated additive materials and processes for packaging and direct die interconnects for extreme temperatures under funding from NextFlex [3,4,5,6]. This paper will present additional results from this program.

II. Materials Rationale

Alumina is selected because its capability for high reliability electronics packaging and has the materials infrastructure for high temperature applications used in hybrid electronics. Alumina is capable to withstand over 1000°C with corrosion resistance, and strength. Additive alumina has recently been available but was not characterized for high temperature electronic applications. The program was designed to fill this gap.

Table 1 is a comparison of properties for alumina materials used in hybrid electronics. The alumina used in this study were 96% alumina, Lithoz 350D and Corning Flexible Ribbon alumina. Corning alumina ribbon has a lower dissipation factor and much higher breakdown voltage in addition to its flexibility.

Table 1 Comparison of alumina material properties

Vendor	Lithoz	Corning	CoorsTek
Trade Name	LithaLox 350 D	Flexible Alumina	AD-96
Description	alumina slurry	40um, 80um	Thick film alumina
Purity (%)	99.80%	99%	96.0%
Grain size (um)	NA	1	6
Density (g/cc)	3.985	NA	3.72
CTE (ppm/C)	NA	6.7	8.2
Dielectric Const	9.8-10	9.4	9
Dissipation Factor	0.002-0.004	0.00007	0.0002
Resistivity (Ω-cm)	1.0E+14	3.0E+15	1.0E+14
Breakdown Voltage (kV/mm)	17	270	8.3
Thermal Cond (W/mK)	40	36.7	24.7
Flexural Strength (MPa)	180 (4pt bend)	630	358
Fracture Toughness (MPa-$m^{1/2}$)	3	3-5	4-5
Hardness	1450 (HV10)	25 GPa (nIndent.)	78 (R45N)
Roughness, Ra (um)	0.9	0.040-0.060	0.89

The conductors and dielectrics are selected for high temperature capability and capability to be printed with the nScrypt microdispense printer.
Table 2
lists properties of for materials used in this report. The materials selected in this study include thick films were reported in previous publications for 300C [1,2] that used similar test methods contained in this report. These materials are provided with rheology suitable for nScrypt microdispense printing. Au1 has a small particle size (<1 µm) that lends it to be diluted and atomized for AeroJet printing. Details regarding the performance and testing of this material and other Aerojet printed materials can be found in [5]. The gold and platinum conductors were selected for their low resistivity, electromigration, corrosion and oxidation at high temperature. The dielectric has a crystallizing glass that raises softening temperature with firing temperature. Caution is needed when selecting thick films since some are found to contain sodium glass and bismuth that resulted in dendritic growth and loss of adhesion when placed under bias at 300°C [7]. Pt1 was selected because it has been used for automotive exhaust sensing and in applications greater than 850°C and does not contain sodium or bismuth.

Table 2 Thick Film Properties

Type	**Conductor**	**Conductor**	**Dielectric**
Material ID	Au1	Pt1	D1
Description	Au conductor	Pt conductor	Dielectric
Particle Size (um)	<1 um	10	<5 um
Viscosity (Pa-S, Kcps)	300-400	65-100	80-120
Resistivity (Ohm-cm)	5.00E-06	1.00E-04	NA
Dielectric Constant (@ 1MHz)	NA	NA	8-10
Dissipation Factor (@ 1MHz)	NA	NA	<0.002

III. Characterization testing at 300 to 750°C

Characterization testing was performed on the materials to evaluate their capability for electronics packaging at 300 to 750 °C. Characterization tests includes printability, electrical resistance stability for conductors, electromigration, and adhesion stability testing. Test structures for the tests were designed and printed once printability design rules were determined.

A. Printability

The printability of the thick film materials printed with the nScrypt printed well once printing parameters were determined. A test pattern and printing machine code was created to measure the printed line width for each paste based on the tip diameter, dispense pressure, printing speed, and dispense valve open/close timing parameters. The test pattern is shown in Figure 1 along with the line width results. Three groups of rows with long, medium, and short lines are printed at decreasing speed of 25, 20, 15, 10, and 5 mm/second. The pattern will provide a means to determine line width but also any adjustments needed to the valve open and close wait times. This time is a delay between opening or closing the valve and the stage movement. A large dot at the start of a line indicates the open wait time needs to be decreased and a gap means it needs to increase. Line width was measured using a Leica microscope and LASX software before and after firing. The line width decreases with increased speed and decreased tip diameter. It also varies with the material printed. The materials and machine parameters were found to print the feature sizes needed for the other project tasks that need line width of 150 microns.

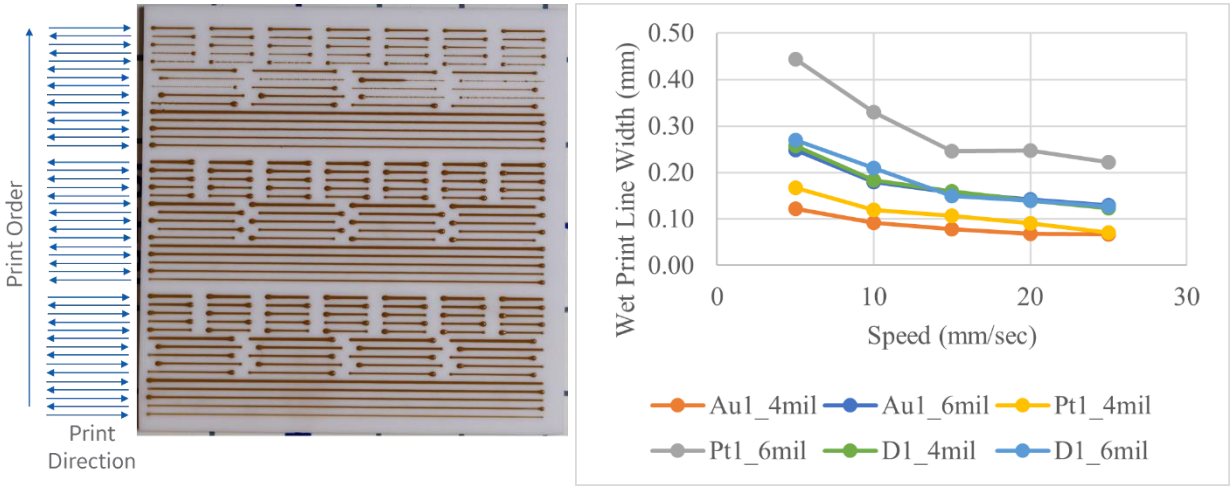
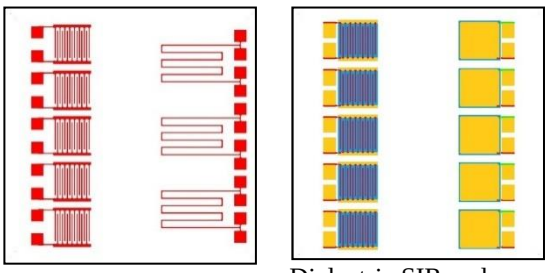


Figure 1 Line Width Test Pattern and Line Width Measurements

B. Electrical Testing

Test patterns for electrical tests are shown in Figure 2. The test patterns are designed to make measurements at 300°, 500°, and 750°C.



Conductor SIR and Resistance Test

Dielectric SIR and Leakage Test

Figure 2 Electrical Test Patterns

The conductor SIR (Surface Insulation Resistance) and resistance test pattern are used to measure conductor electromigration by measuring resistance between the comb pattern under 100V bias. It is based on the IPC SIR test pattern used for circuit boards. The test method is adapted from MIL-PRF-123D 4.6.6.2.1, used for measuring capacitor leakage current. The SIR pattern was measured with and without D1 dielectric over printed to measure electromigration and dielectric leakage. The resistance pattern measures resistance stability using 4 point probe measurement during high temperature aging. The resistance pattern is used to make 4-point resistance measurements that was recorded at

temperature by a DAC (Agilent 34972A and 34901A 20 channel multiplexer card). The test pattern has a meander line with a total length of 91mm and 254µm wide and four pads for measuring the 4-wire resistance instrumentation. The measurement will also provide information on the temperature coefficient of the conductors.

The electrical tests electrically recorded the test samples while at the test temperatures. This requires wiring, fixtures, and a method to make connection to the test pads on the test samples. The ovens and a wired sample used at GE are shown in Figure 3. Test instruments are located on the shelf above the furnaces with wires exiting the vent in the furnace top and back to the instrumentation.

Type K thermocouple wires with Nextel insulation were selected for this testing. Tests using silver plated copper furnace wire were not stable at 700°C due to conductor and insulation limitations. Nickel clad copper wires were found to be limited to about 150 hours at 800°C. The Type K wires were selected to reduce risk of wire failure for longer tests at 750°C and lower cost than platinum wires.

Figure 4 shows the process used to connect wires to samples. Wires were attached for 4 wire resistance test samples by welding a bead at the wire ends of the Type K thermocouple pair to keep the two wires together during attachment and provide the source and sense pairs. Wire pairs were connected for the source (chromel to chromel) wires and sense (alumel to alumel) connections to minimize Seebeck effect. Wires are cut to 6 inch lengths to minimize movement of wires during assembly and connected to ceramic terminal blocks. Connection to the sample is made by dispensing a drop of Au1 thick film to bridge the wire and the test pad and firing at the 850°C, 60 minute profile in air. A strain relief bar is tightened down onto the Nextel insulation to minimize stress on the connection during handling. The wires are attached to instrument wires in the furnaces from the ceramic terminal blocks.

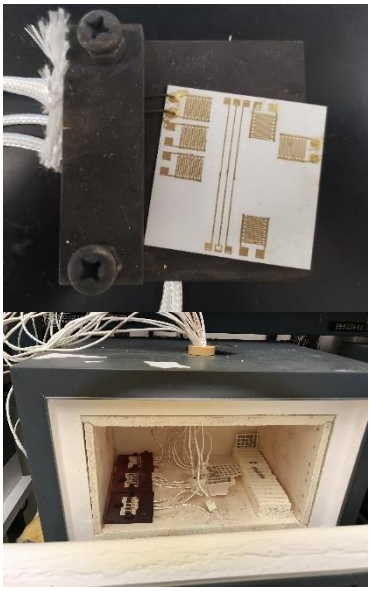
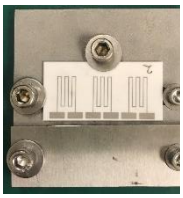
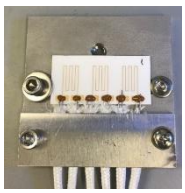


Figure 3 Sample wire attach fixture after 24 hours at 750°C and high temperature storage test furnaces



a. Place and align substrate into fixture

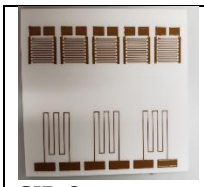


b. Insert and align wires to test pads. Apply Au1.

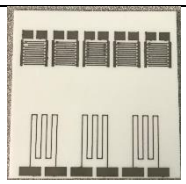
c. Fire at 850°C, 60 min

Figure 4 Wire attach method used by GE

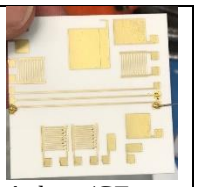
Resistance stability screening test of Au1 gold and Pt1 platinum thick film paste test patterns printed by the nScrypt was measured at room temperature at intervals of high temperature aging to get a forward look at the targeted conductors for capability at 300, 500, and 750°C for 1000 hours. Examples of the test patterns used in the test are shown in Figure 5. The serpentine pattern of the SIR&Resistance design and the 3 straight lines in the Auburn Electrical Line test pattern were measured.



SIR & Resistance Test Pattern: Au1



SIR & Resistance Test Pattern: Pt1



Auburn/GE Electrical Line: Au1

Figure 5 Examples of test patterns for resistance stability testing at 300°C, 500°C, and 750°C

Resistance stability plots are shown in Figure 6 for 300°C, 500°C, and 750°C for Au1 and Pt1 measured at room temperature at intervals of aging. The Au1 paste has a lower resistance than the Pt1 paste overall. Measurements were taken after 120, 250, 500, and 1000 hours using a Fluke multimeter using a 2-wire method.

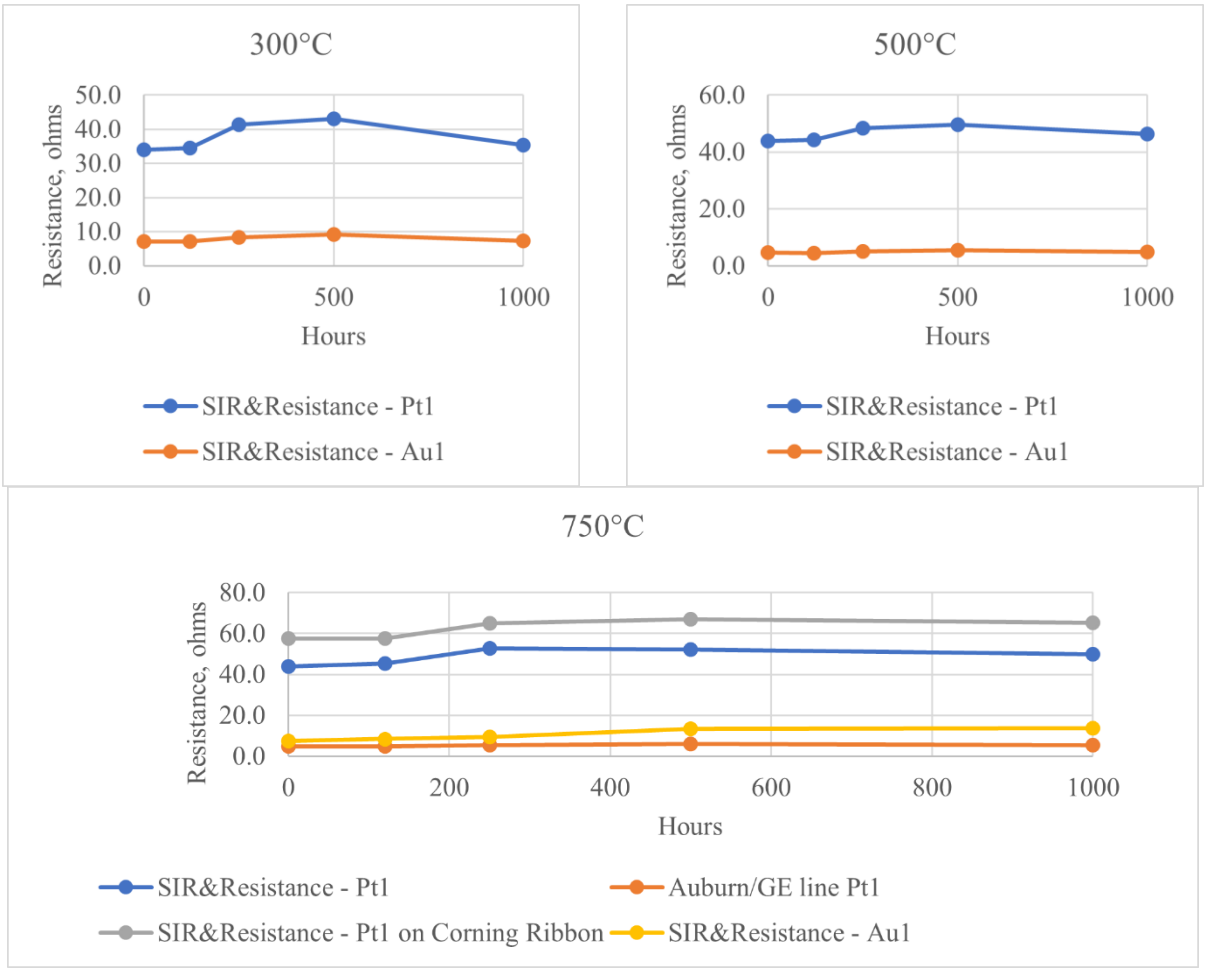


Figure 6 Interval Resistance Stability

Resistance stability of Au1 and Pt1 was then measured at the test temperatures using 4 wire measurement and the fixtures described previously. The results are shown in Figure 7. The Au1 thick film shows an initial rise in resistance proportional to the furnace temperature as the sample heats and stabilizes during the test period. Sample 300_2 had intermittent connection problems which show as spikes in the resistance and stabilize when stress on the instrument wires was minimized. On other tests, shorter wires (6 inch) with ceramic terminal blocks resolved this type of issue. The Pt1 thick film also shows the rise in resistances as the sample heats and stable resistance at 300° and 500°C during the test period. There is a gradual increase in resistance at 750°C during the test period that as also seen in the interval resistance test within the first 300 hours. They had a gradual increase in resistance between 100 and 300 hours that stabilized thereafter.

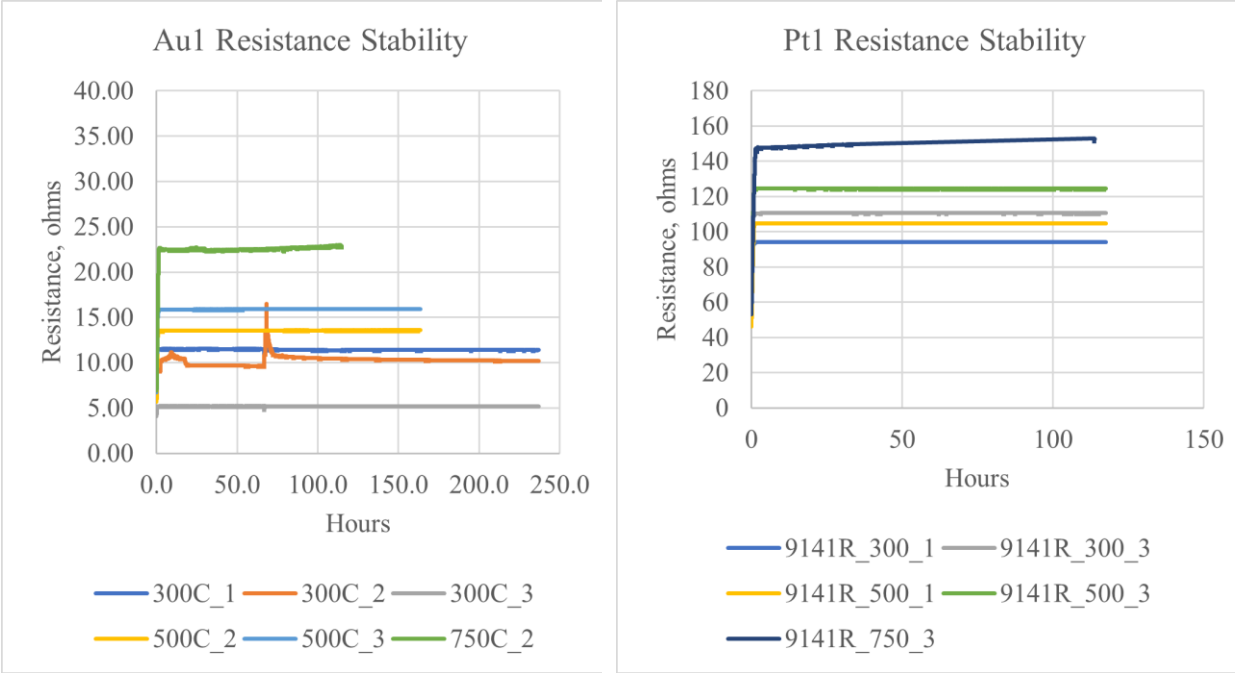


Figure 7 Resistance Stability at 300°, 500°, and 750°C for >100 hours

Electromigration of the conductors and leakage current of dielectrics is evaluated by measuring the leakage current using a surface insulation resistance test pattern as shown in Figure 8. The test pattern has interdigitated fingers (nominal 10 mils) connected to a 100 V bias across gaps (nominal 10 mils) to create an electric field to drive electromigration.

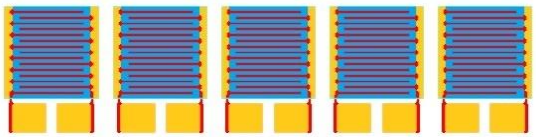


Figure 8 Surface Insulation Resistance Test Pattern

This test uses the high temperature fixtures described earlier and shown in Figure 4 since the mechanisms are temperature dependent. The voltage across the SIR pattern is continuously measured with a DAC (Agilent 34972A with one 34908A 40 channel multiplexer card, two 34903A 20 channel actuator cards) while under a 100V bias and monitored by a LabView VI that monitors the voltage drop, stores into a log file with a time stamp, and removes a failed test pattern from the circuit when the voltage drops below a threshold (1 microamp) indicating excessive leakage caused by dendritic growth.

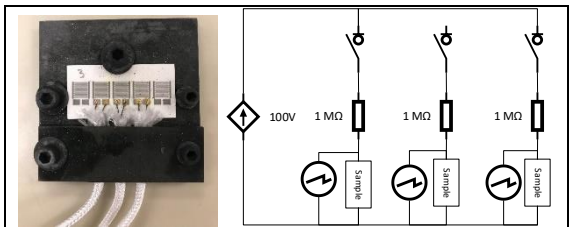


Figure 9 GE SIR Test Circuit (MIL-PRF-123D)

SIR testing was performed on Au1 and Pt1 with and without D1 dielectric. The test results for Au1, Pt1, and D1 applied over Au1 are shown in Figure 10. The leakage current results are measured in microamps and plotted for 100 hours or more. There are spikes in the data that represent times when there are interrupts in data collection when zero voltage is logged. This would happen when the computer hosting the LabVIEW application would have a software update. The results for Au1 are stable for 300°C, 500°C, and 750°C. A decrease in leakage current was observed in the 750°C results when the voltage is first applied and levels off at a stable value. This has been observed in other thick films. The results for Pt1 shows stable results with a decrease at the start of the 750°C samples as seen with Au1. Similar results are seen with the D1 samples.

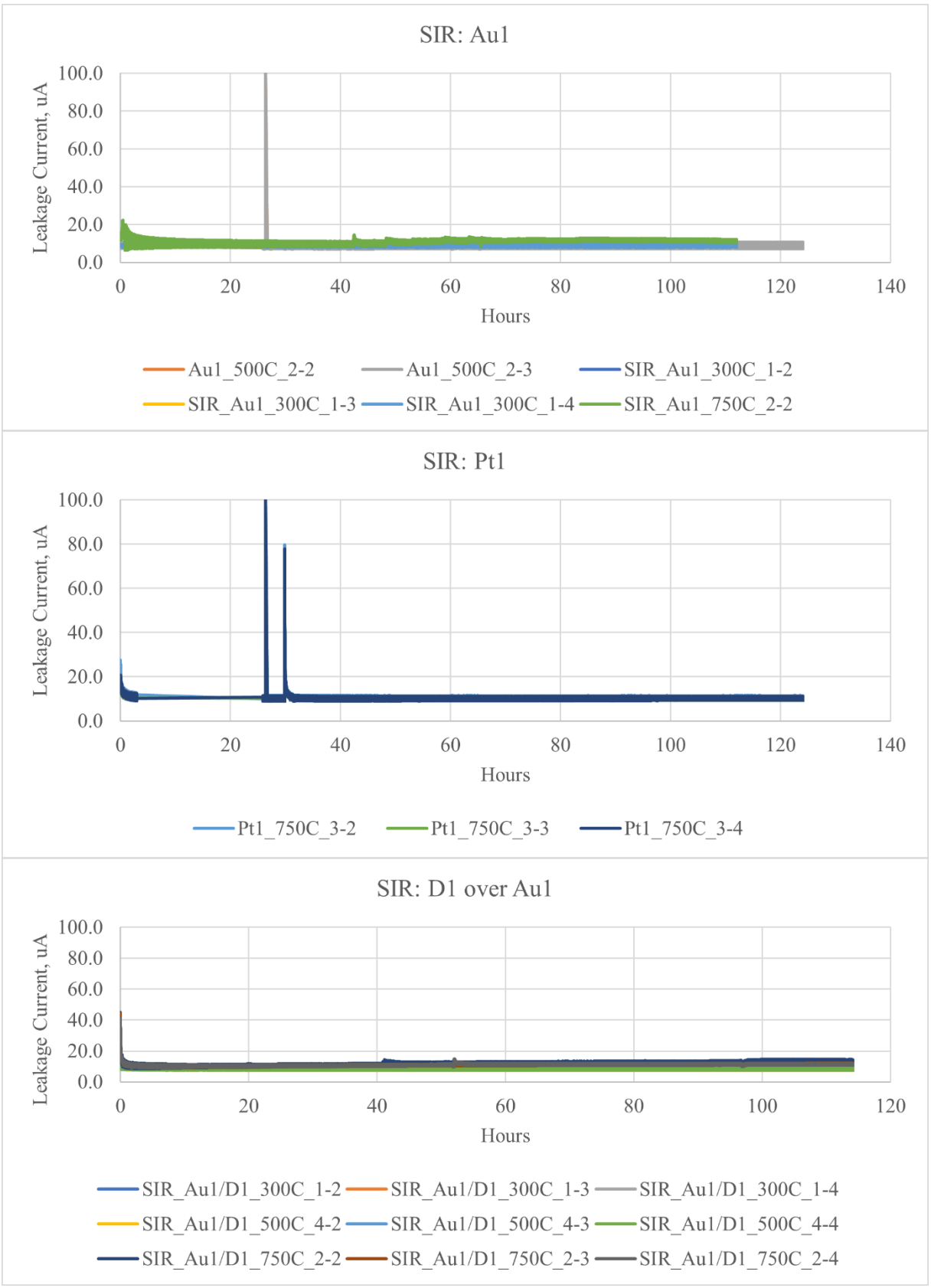
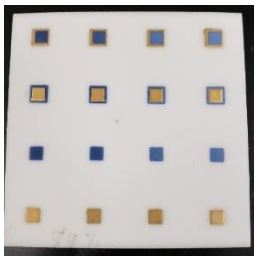
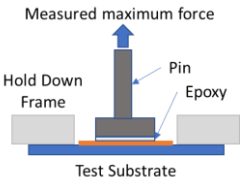


Figure 10 SIR Results: 300°C, 500°C, 750°C

Adhesion of the films is dependent on the substrate and the material printed on it. Adhesion strength stability was tested on 96% alumina, Lithoz 350D 99.8% additive alumina, and 80 µm Corning Alumina Ribbon. The results for 96% alumina can be found in Shaddock [4]. The adhesion test pattern measures the bond strength of the conductor and dielectric to the substrates and between the conductor and dielectric pastes after high temperature aging at 300, 500, and 750°C for at least 100 hours. The bond strength is measured using the ASTM stud pull testing method (ASTM D4541-17). The test pattern consists of squares that are 0.110 inch (2.8 mm) square for the top layer and 0.150 inch (3.8 mm) square for the bottom layer were used for conductor to dielectric tests in Figure 11 for both substrates. Four pads each of dielectric over the conductor and the conductor over the dielectric were also printed to represent design conditions needing cross overs. The Corning Ribbon ceramic was printed and then sawed into strips for testing. Epoxy bond standard stud pull pins (Quad Group PN 901106 0.106" diameter epoxy coated aluminum pull studs) are attached to each square and force is measured to remove the pin. A stainless steel shim was attached to the back of the ceramic substrate using EpoxyBond 110 from Allied High Tech to prevent fracture of the ceramic during pull testing.



Conductor and Dielectric Adhesion Test Pattern



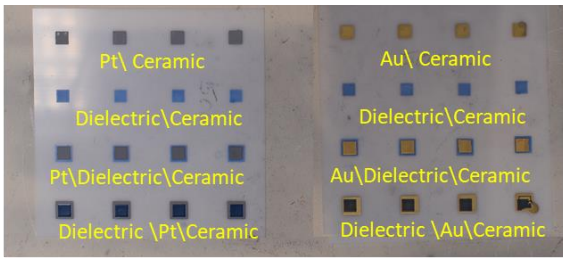


Figure 11 Stud Pull Test Pattern and schematic

Adhesion testing was measured for Au1, Pt1, and D1 dielectric on the two substrates. One sample was adhesion tested after printing and used as the reference. Other substrates were placed into ovens set at 300°C, 500°C, and 750°C for aging up to at least 100 hours and adhesion tested at intervals.

C. Adhesion Testing

Adhesion testing was made using Lithoz 350 additive alumina substrates with Au1, Pt1, and D1. Test results are plotted for 300°C, 500°C, and 750°C aging in Figure 13 for D1 and Figure 14 for Au1 and Pt1 alone and with D1. The test groups with combinations are listed as top layer/bottom layer notation. Four measurements were taken for each condition in most conditions and plotted as box plots in the figures to show the range of values. Some measurements were not included when the Lithoz substrate would crack. Some substrates contained voids which compromise strength as shown in Figure 12. Au1 maintained stable adhesion at all temperatures for 100 hours with and without D1 dielectric. There is a decreasing strength over time with the Pt1 at all temperatures and mixed results with D1. D1 has a general decrease in strength over time at the three temperatures as seen with 96% alumina substrates.

Figure 12 Lithoz 350D adhesion test sample with voids

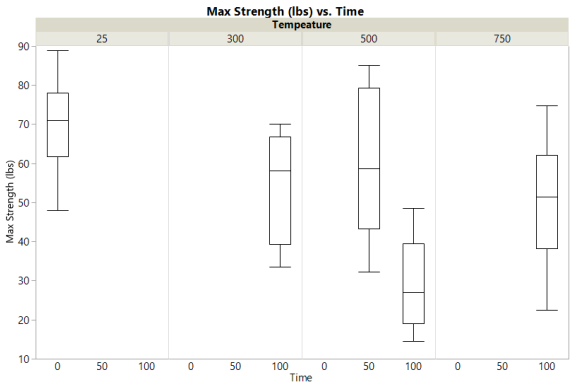


Figure 13 Adhesion Strength of D1 on Lithoz 350D

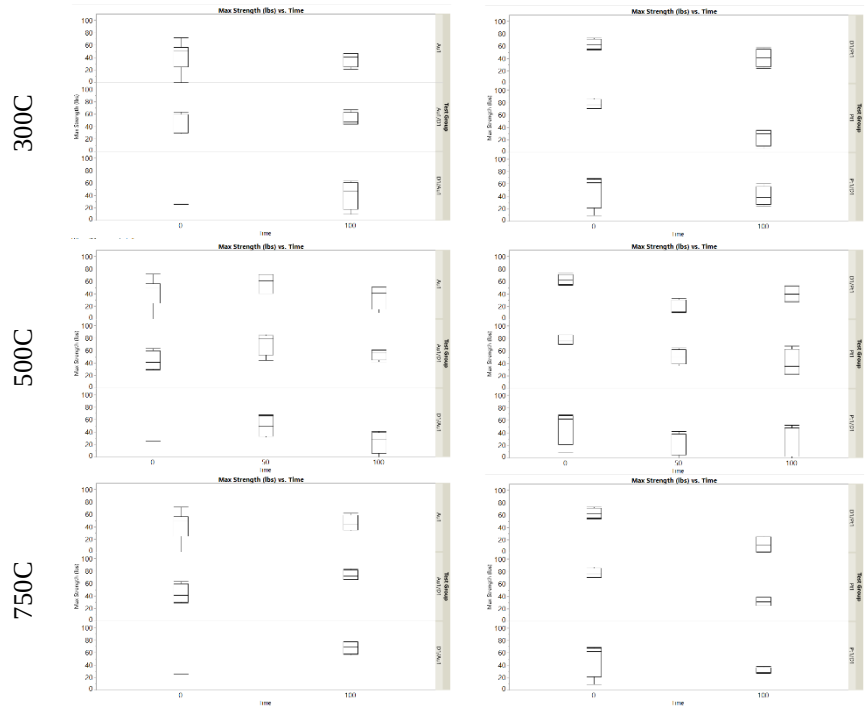


Figure 14 Adhesion Stregth on Lithoz 350D

Adhesion testing was also made on Corning Alumina Ribbon. Adhesion was stable for the Au1 and D1 pastes as shown in Figure 15. Adhesion was also found to be stable Pt1 and D1 dielectric as shown in Figure 16. The 300°C condition of D1 alone in this group did not follow that in the Au1 group. The adhesion between conductors and dielectric show potential for multilayer circuitry.

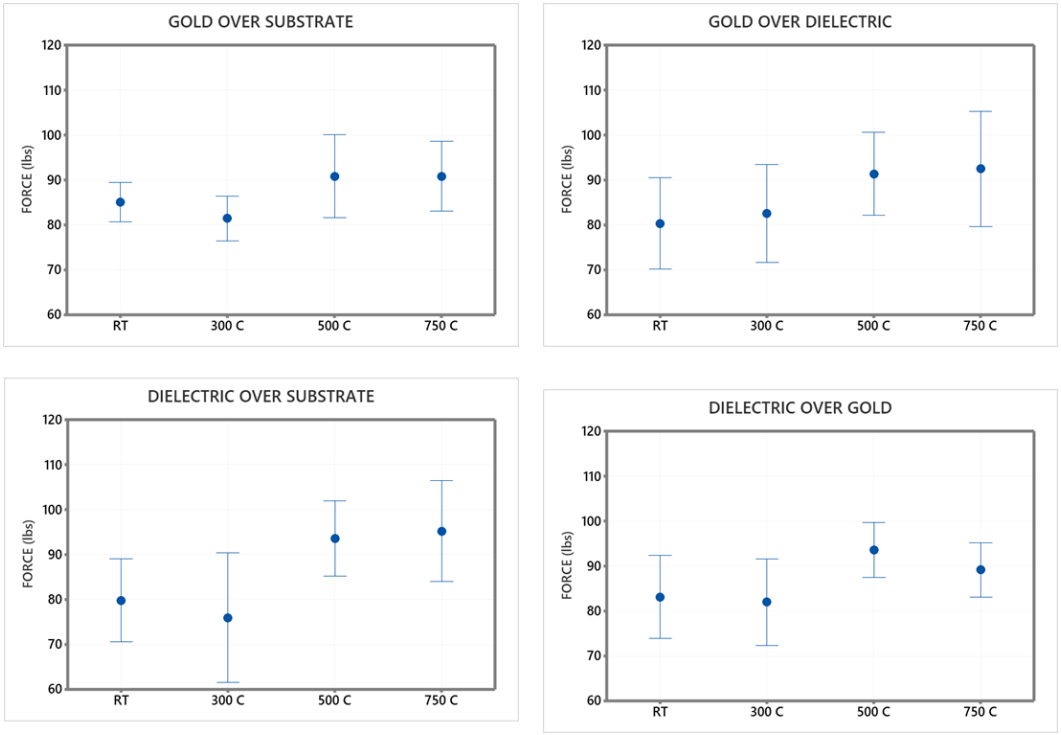


Figure 15: Adhesion strength of Au1and D1 dielectric on Alumina Ribbon Ceramic

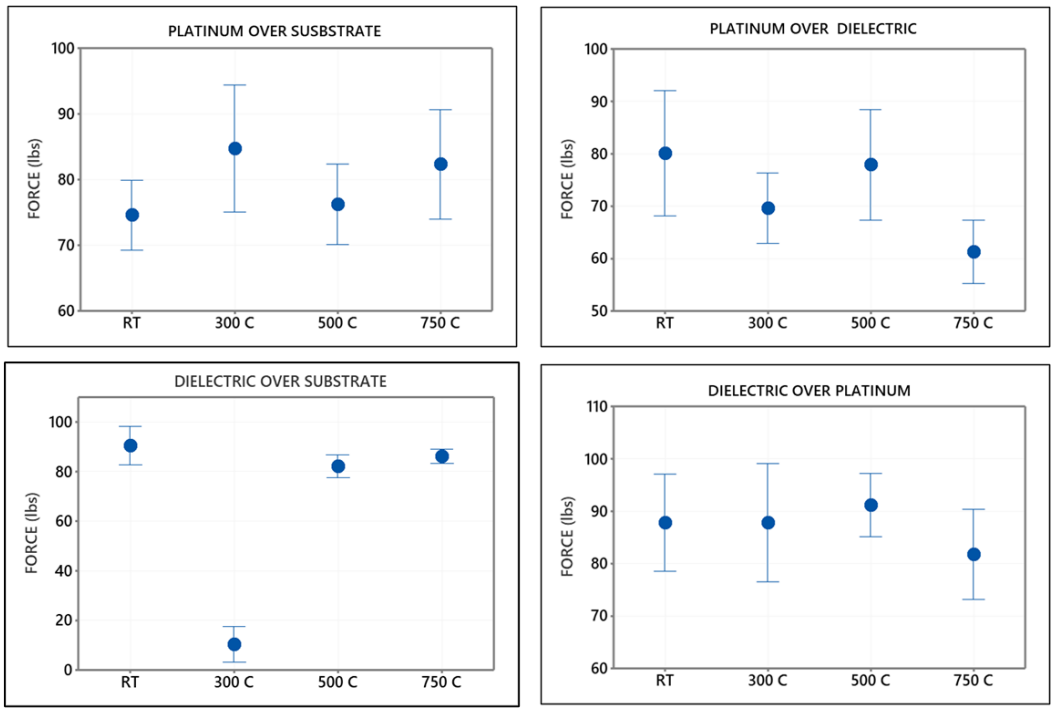


Figure 16: Adhesion strength of Pt1 and D1 dielectric on Alumina Ribbon Ceramic

D. Bend Testing

Bend testing was performed on 40 µm Corning Alumina Ribbon with the test patterns shown in Figure 17 printed with Au1 using the bend tester at Binghamton University. The test pattern has straight and serpentine lines with total effective length of 1 and 2 inches, respectively. The test leads are connected to four 2 mm by 1 mm rectangular pads for four-wire resistance measurement during the test.

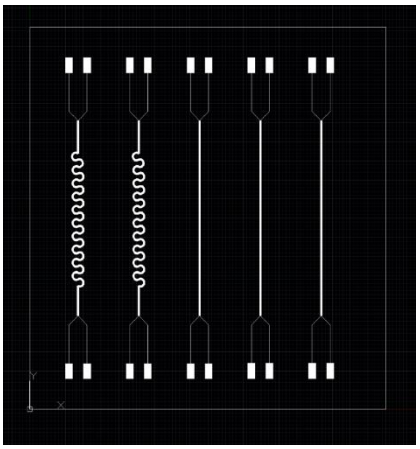


Figure 17: Test Structure for bending tests

Figure 18 shows test samples printed with the nScrypt. The samples were fired and sawed into strips. The Pt1 samples were not tested because they were sawed conductor side down to the dicing down because of the substrate transparency and were not able to be removed without damaging the traces. The strips were divided into groups with some samples bend tested after firing and some samples after aging at 300°C, 500°C, and 750°C for 100hr.

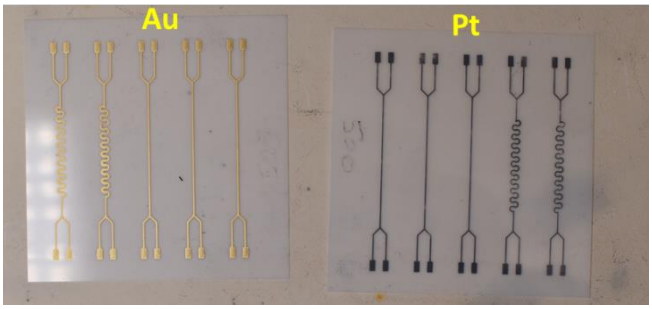


Figure 18 nScrypt printed test structures on Alumina Ribbon Ceramic using gold and platinum

Lead wires were attached to the sample pads using four small diameter copper wires of an inch length using Ag-based conductive paste. After curing, the pad-ends of the test vehicle are supported using long paper strips of about 12 in are using strong double-sided tape. This helps to reinforce and provide better handling capability for these fragile and brittle samples. It also provides essential length needed to

mount on the mandrel bend test set-up as shown in Figure 19.

Figure 19: Sample after preparation

The bend tester shown in Figure 20 consists of a moving mandrel to bend the sample in tension and compression. The test were performed using four mandrels of different radiuses: 1 in, 2 in, 3 in, and 4 in. The tests were run at a speed setting of approximately. 0.25Hz to avoid shuddering of the sample off the set-up due to the impact of the mandrel. Each sample is tested for 1000 cycles while continuously monitoring resistance.

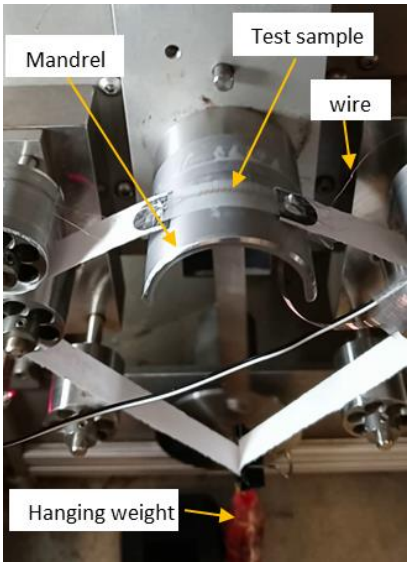


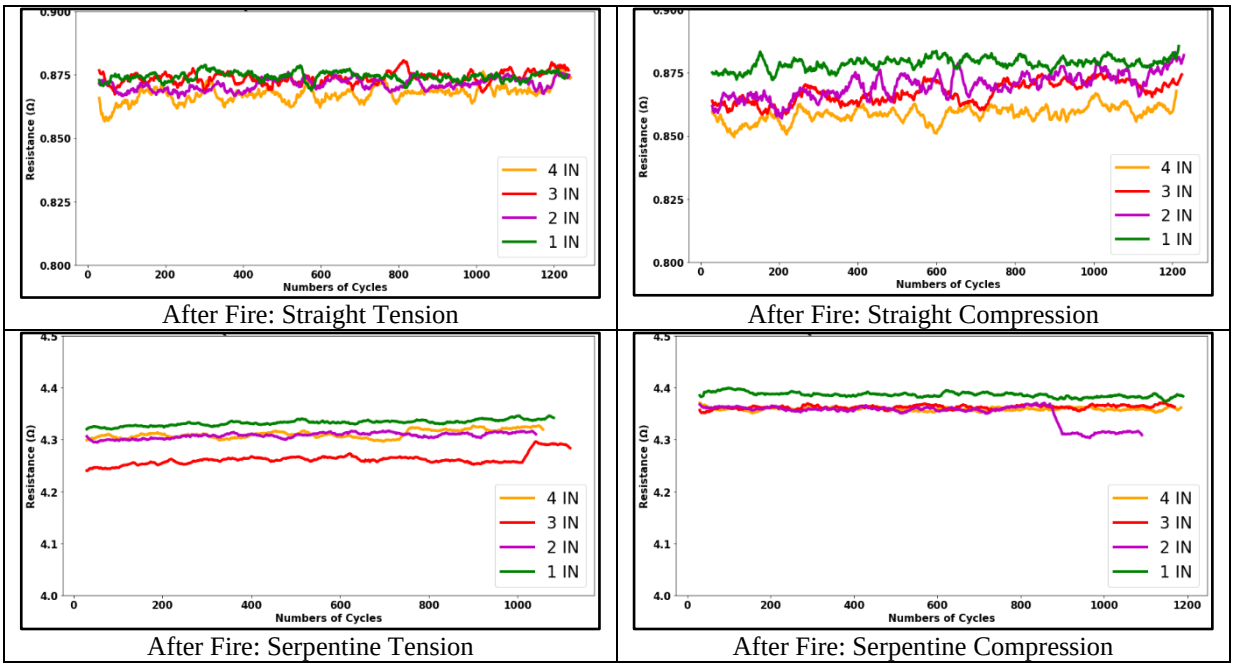
Figure 20: Testing Setup

Figure 21 shows the plot of resistance in tension and compression of Au1 after firing for the straight and serpentine lines at increasing stress levels (4 inch to 1 inch). Peak resistances of straight and serpentine traces in tensile and compression bending shows that the resistance with cycles mostly remains the same. However, the average peak resistance for a straight trace increases ever so slightly for tensile bending and in the subsequent compression bending the increase in average peak resistance is more pronounced with decrease in bending radii. Such observations with the bending radii could not be found in the case of serpentine traces. The straight trace could be found to be noisier than a serpentine trace as the trace resistance is lower (close to the lower measurable range of the data logger used). We observe a variance in peak resistance of about 0.05Ω in case of straight line and 0.2Ω in case of serpentine line.

The resistance during bending of the samples after aging at 300°C is shown in Figure 22. The graphs show that resistance is very stable and nearly constant in case of straight line, although in case of serpentine line at highest stress (1 in bending radii) in both tensile and compressive bending the peak resistance increases with cycles.

Peak resistance of bending tests of samples aged at 500°C and 750°C are presented Figure 23 and Figure 24, respectively. The resistance variation is very similar which is about 1Ω in case of straight line and 3Ω in case of serpentine line. As opposed to the unaged test structures the peak resistance is not constant with cycles. We can observe, while very small and unsteady, increase in resistance. Nevertheless, the resistance returns (quickly) to its initial value (prior to bending) after the test.

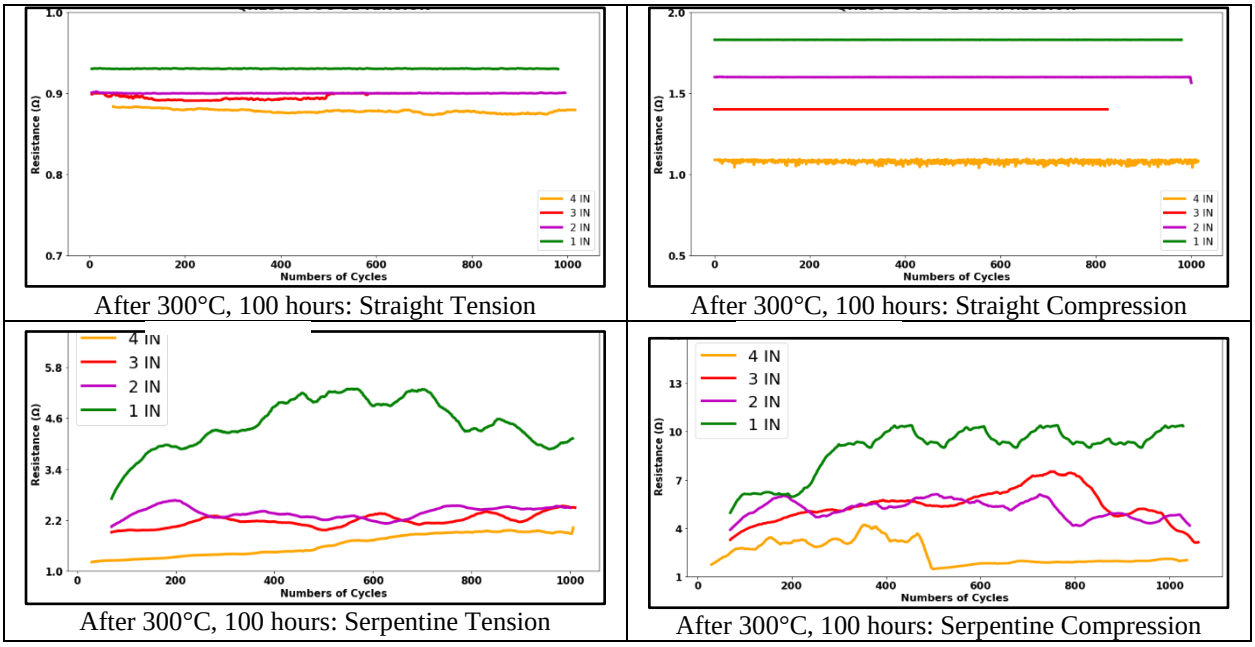
Practically, the bending of these test structures shows that even after exposure to high temperature for a very long time (100 h), the correlation to major parameters under consideration is found to be weak. The nature of these substrates lends itself easily bend and failure due to bending (hence the reason for testing in the harsh possible loading mode). Above results indicates that, depending on the application, the printed test structures on the thin Corning Flexible Alumina Ribbon Ceramic substrates are very robust within the stress ranges we tested these samples.



After Fire: Straight Tension | After Fire: Straight Compression

After Fire: Serpentine Tension | After Fire: Serpentine Compression

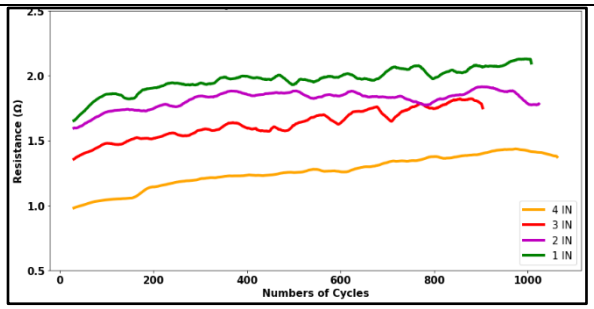
Figure 21: Peak resistance vs. number of cycles for both straight and serpentine gold (Au1) lines tested at 4 bending radii and 2 test configurations after firing



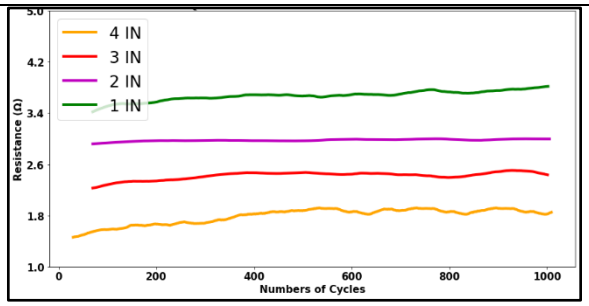
After 300°C, 100 hours: Straight Tension | After 300°C, 100 hours: Straight Compression

After 300°C, 100 hours: Serpentine Tension | After 300°C, 100 hours: Serpentine Compression

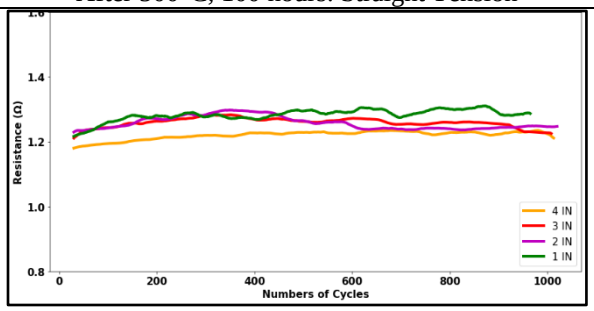
Figure 22: Peak resistance vs. number of cycles for both straight and serpentine gold (QR150) lines tested at 4 bending radii and 2 test after aging at 300 °C for 100 hours



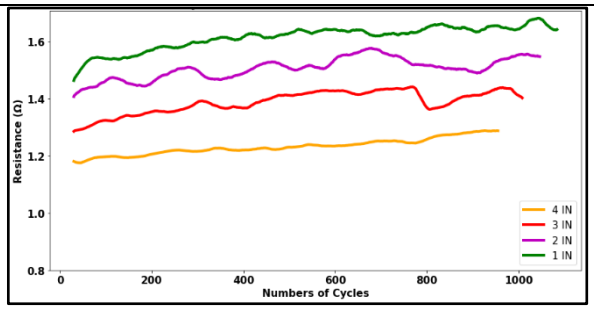
After 500°C, 100 hours: Straight Tension



After 500°C, 100 hours: Straight Compression

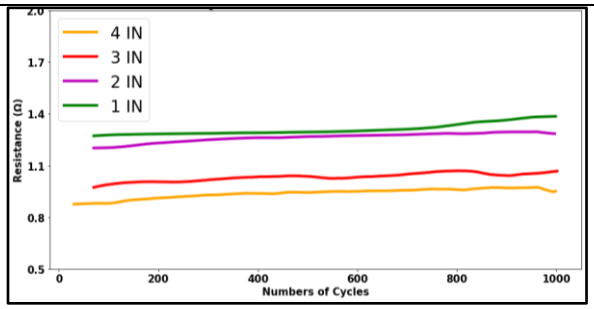


After 500°C, 100 hours: Serpentine Tension

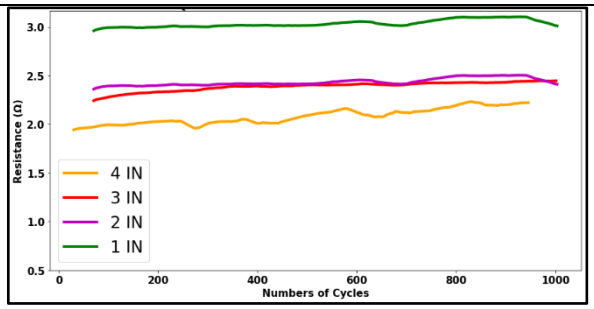


After 500°C, 100 hours: Serpentine Compression

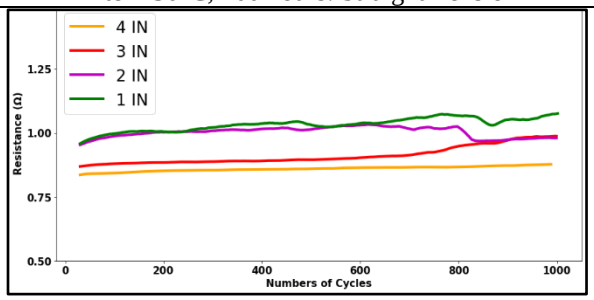
Figure 23: Peak resistance vs. number of cycles for both straight and serpentine gold (QR150) lines tested after aging at 500°C for 100hours



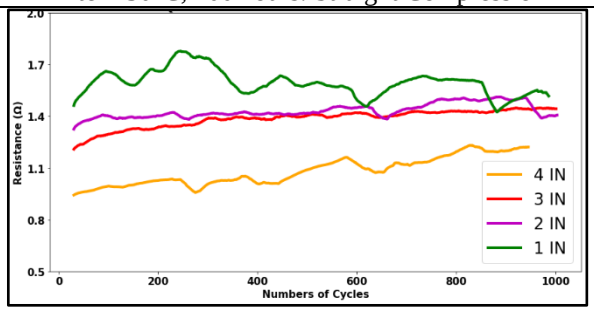
After 750°C, 100 hours: Straight Tension



After 750°C, 100 hours: Straight Compression



After 750°C, 100 hours: Serpentine Tension



After 750°C, 100 hours: Serpentine Compression

Figure 24: Peak resistance vs. number of cycles for both straight and serpentine gold (QR150) lines tested after aging at 750°C for 100hr

IV. Direct Die Interconnect

Direct die interconnect was evaluated as a method to interconnect high temperature capable devices, such as SiC, for high temperature operation. The direct write interconnect methods evaluated are surface interconnect and embedded interconnect. The surface interconnect method uses a ramp so that a conductor can be printed up the ramp from the substrate to the die pad. The embedded approach has the die place into a pocket of an additively printed substrate so that the surface is even with the substrate and the conductor printed direct printed from the substrate to

the die pad. Both methods require a suitable die, die attach, and interconnect material.

Daisy chain silicon die were fabricated in the GE fab using gold conductor metallization stacks and backside metal suitable for 500C. Figure 25 shows one of the 4.5 mm x 4.5 mm x 500 micron silicon die with Au metallization used for direct write interconnect testing after 100 hours at 500°C.

Figure 25 Au Daisy Chain Test Die after 100 hours at 500°C

Two die attach materials were evaluated for die attach: NanoAu sintering paste and CuSn TLP paste. The CuSn TLP was found after shear testing after aging at the temperatures to be incompatible with the backside metallization selected and will not be included in this report. The NanoAu paste requires pure gold surfaces to perform best so a pure gold thick film paste was used with this material. Figure 26 shows the shear strength of the NanoAu sintering paste after high temperature storage testing for 100 hours and high temperature thermal shock testing for 100 cycles on A1 and Pt1 over printed with PureAu paste. The shear strength was above the Mil-Std-883 requirements for 300 and 500C. The strength decreased at 750C and has some samples below specification for room temperature to 750°C thermal shock testing.

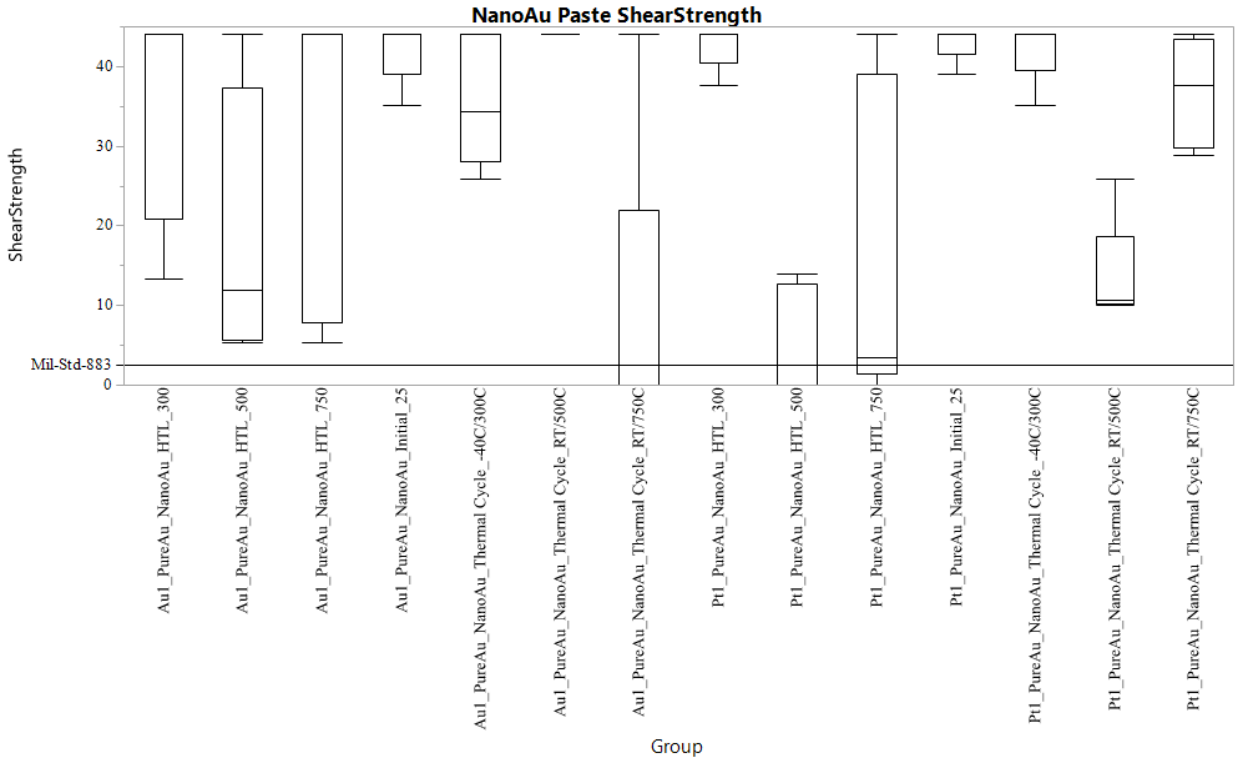


Figure 26 NanoAu Paste Shear Strength Testing Results

Methods and materials for making high temperature direct die interconnects had to be created since this was not performed before for this temperature range. The methods were inspired by earlier methods found in publications. The temperature exposure of the die during processing was limited so not to damage the die yet be capable of reliability testing at 500°C. The method used was inspired by the result shown in Figure 27. Au1 may be fired at a lower temperature to achieve similar resistance but not equivalent

adhesion. The approach is to print Au1 up to the ramp with full firing for adhesion then print Au1 to the die pad and fire at 450C to make the final connection.

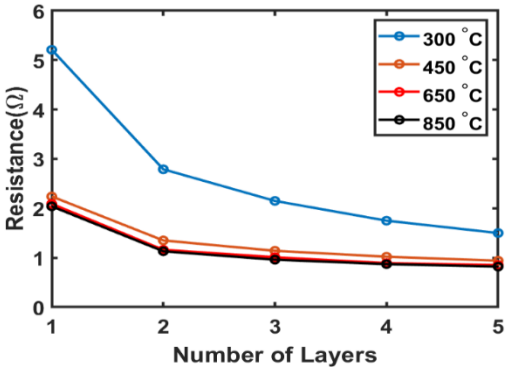
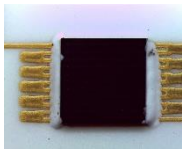
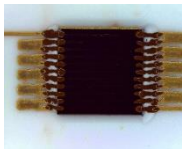


Figure 27 Au1 Firing Temperatures

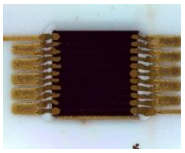
Surface interconnected die were fabricated by printing the conductor test pattern on an alumina substrate, attaching the die with NanoAu, printing a ramp up to the die surface with alumina ceramic adhesive, then direct write Au1 from the substrate to the die pad.



1. After ceramic adhesive ramp



2. After Au1 dispensing



3. After 450°C 20 min fire

The resistance of each connection is shown in Figure 28.

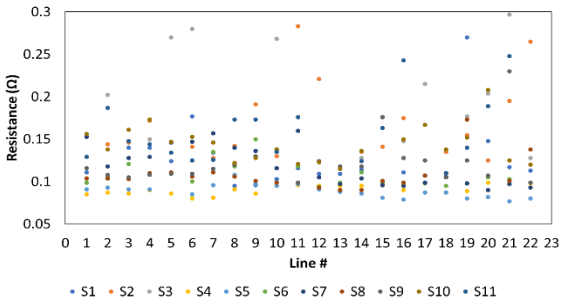


Figure 28 Surface Interconnect Connection Resistance after firing.

Figure 29 shows three samples each were aged at 300C and 500C for 100 hours with resistance measured before and after testing. The results are shown in Figure 29 before and after aging. The resistance distributions increased about 50 milliohms after aging at 300C. The resistance and variance increased after 500C aging by 50 to 100 milliohms.

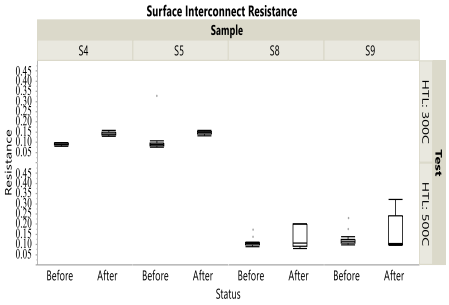


Figure 29 Surface Interconnect Diasy Chain Resistance after aging at 300C and 500C for 100 hours

Figure 30 shows three samples each were thermal shock tested at -40C to 300C and room temperature to 500C for 100 cycles with resistance measured before and after testing. One sample had all connections fail, and the other two increased by 2 to 7 ohms. The three room temperature to 500C samples survived with an increase of 3-5 ohms with an increase in variance.

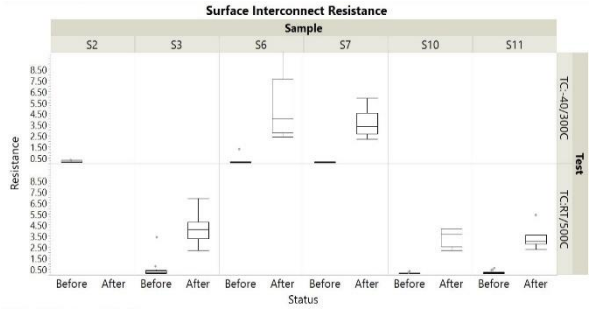


Figure 30 Surface Interconnect Daisy Chain Resistance after Thermal Shock for 100 cycles

The embedded die interconnect approach uses an additively printed substrate with near net shape pockets that the die fit into with a clearance of 165 microns. The die attach pads and interconnect lines are printed onto the substrate, die attached using NanoAu paste, ceramic adhesive was used to fill the gap, and the interconnect was made by dispensing Au1 and firing at 450C for 20 minutes. Figure 31 shows examples of the substrate with die inserted and a die interconnected.

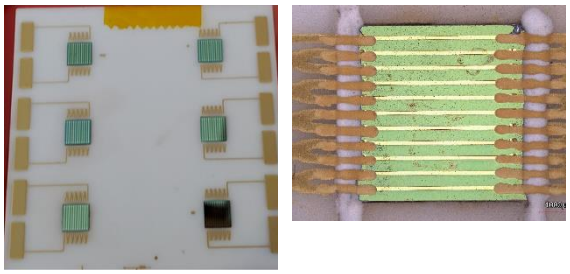


Figure 31 Embedded Die Interconnect Substrate and Sample

Resistance was measured across each interconnect from the substrate to the die and shown in Figure 32. The interconnect resistance variance is smaller than for the surface interconnect.

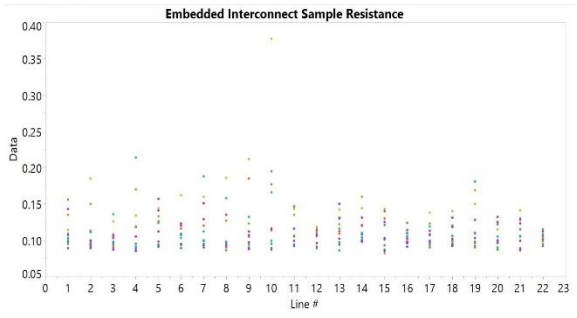


Figure 32 Embedded Interconnect Resistance after Firiing

Three samples each were aged at 300C and 500C for 100 hours with resistance measured before and after testing. The results are shown in Figure 33 before and after aging. The resistance distributions have some overlap with the resistance raised slightly at 300C and 500C.

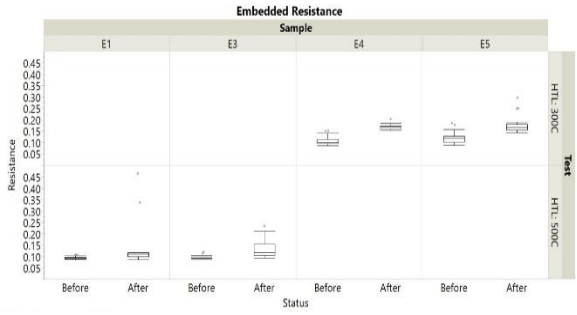


Figure 33 Embedded Interconnect Diasy Chain Resistance after aging at 300C and 500C for 100 hours

Three samples each were thermal shock tested at -40C to 300C and room temperature to 500C for 100 cycles with resistance measured before and after testing. A rise in resistance is seen for the -40C to 300C samples of about 1-2 ohms and for the room temperature to 500C of 2-3 ohms with an increase in variance. This performed better than the surface interconnect samples.

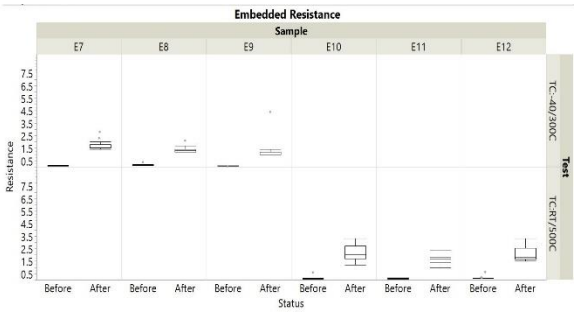


Figure 34 Embedded Interconnect Daisy Chain Resistance after Thermal Shock for 100 cycles

V. Conclusion

This paper has presented the capability of three thick film pastes (Au1 gold, Pt1 platinum, D1 dielectric) to be additively printed using a nScrypt Microdispense printer onto 96% alumina, Lithoz 350D additive alumina, and Corning Ribbon Alumina Ceramic. The electrical and adhesion stability at 300, 500, and 750C was found to be stable on these substrates for at least 100 hours. The pastes can be printed with feature sizes similar to screen printing but without the needed tooling and material loss using that process. Au1 and Pt1 had stable electrical resistance over the temperature range with Au1 having a lower resistance. Au1, Pt1, and D1 dielectric had stable leakage current and adhesion over the temperature range. D1 shows decreased adhesion strength when compared to the conductors and when the base layer in stacked samples but adhesion improved with time and temperature during the test that indicates an improvement may be found with higher firing temperature. Bending tests of Au1 on 40 micron Corning Ribbon ceramic before and after aging at 300C, 500C, and 750C demonstrated elasticity even after aging.

This paper also presented a method and capability for direct write interconnection of devices up to 500C. Surface interconnects and embedded interconnects, using additive alumina substrates shows the capability of the process. The samples were tested at 300 and 500C aging for 100 hours and thermal shocked at -40C to 300C and room temperature to 500C for 100 cycles. The embedded interconnect was found to have better performance.

Acknowledgment

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