AlGaN High Electron Mobility Transistor for High Temperature Logic

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Abstract

We report on AlGaN HEMT-based logic development, using combined enhancement- and depletion-mode transistors to fabricate inverters with operation from room temperature up to 500°C. Our development approach included: (a) characterizing temperature dependent carrier transport for different AlGaN HEMT heterostructures, (b) developing a suitable gate metal scheme for use in high temperatures, and (c) over-temperature testing of discrete devices and inverters. Hall mobility data revealed the GaN-channel HEMT experienced a 6.9× reduction in mobility, whereas the AlGaN channel HEMTs experienced about a 3.1x reduction. Furthermore, a greater aluminum contrast between the barrier and channel enabled higher carrier densities in the two-dimensional electron gas for all temperatures. The combination of reduced variation in mobility with temperature and high sheet carrier concentration showed that an Al-rich AlGaN-channel HEMT with a high barrier-to-channel aluminum contrast is the best option for an extreme temperature HEMT design. Three gate metal stacks were selected for low resistivity, high melting point, low thermal expansion coefficient, and high expected barrier height. The impact of thermal cycling was examined through electrical characterization of samples measured before and after rapid thermal anneal. The 200 nm tungsten gate metallization was the top performer with minimal reduction in drain current, a slightly positive threshold voltage shift, and about an order of magnitude advantage over the other gates in on-to-off current ratio. After incorporating the tungsten gate metal stack in device fabrication, characterization of transistors and inverters from room temperature up to 500°C was performed. The enhancement-mode (e-mode) devices' resistance started increasing at about 200°C, resulting in drain current degradation. This phenomenon was not observed in depletion-mode (d-mode) devices but highlights a challenge for inverters in an e-mode driver and d-mode load configuration.

Key words

AlGaN, III-N, HEMT, High-temperature electronics

I. Introduction and Background

High temperature electronics are needed for automotive, aerospace, military, petroleum and geothermal well applications, as well as for high temperature manufacturing. Compared to conventional materials such as silicon, which has a practical operating limit at temperatures of about 250°C, wide and ultra-wide bandgap materials have superior suppression of intrinsic carrier effects and thermionic emission-induced leakage [1], making them prime candidates for high temperature electronics. Wide band gap materials such as SiC [2] and GaN [3] have been previously investigated for high temperature device operability, yet Al-rich AlGaN [4] has an even wider bandgap than SiC and GaN, potentially making it even more suitable for high temperature applications.

Ultra-wide bandgap aluminum-rich AlGaN transistors and logic gates were explored as candidates for use in high temperature environments, up to 500°C. Because of the ultra-wide bandgap of AlGaN, these semiconductors offer potential technological advances to environmentally harsh conditions in which conventional semiconductors cannot operate [1]. Previously, AlGaN has been investigated as a candidate material for use as next-generation power switches and radio frequency (RF) devices [2-18], but in ordinary settings its more mature competitors such as GaAs, SiC, and GaN are difficult to outperform. However, AlGaN has some unique strengths derived from its bandgap, durability, and substrates that could be advantageous when used in non-standard applications. By playing on its strengths, AlGaN has the potential to expand the capabilities and environmental limitations beyond those of more established materials.

We report on the development and initial demonstration of

AlGaN HEMTs for digital logic for operation from 25°C to 400°C. Material and design choices that normally work at room temperature had to be re-evaluated and substituted with choices tailored towards high temperature operation. A mask set was designed for testing digital logic at high temperatures, which utilized local threshold voltage control and combined enhancement and depletion mode devices to make inverters. The resulting inverters, tested from room temperature to 491°C, had stable operation over the entire temperature range. This work represents a first demonstration of the high temperature capability of AlGaN high electron mobility transistor (HEMT) inverter circuits.

II. Experimental Methods

A. Epitaxial Growth and Device Fabrication

All AlGaN epilayers were grown by metal-organic vapor phase epitaxy (MOVPE) in a Veeco D-125 system at 75 torr using conventional precursors, including trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia. Nitrogen was used as a carrier gas along with a balance of hydrogen and the growth temperature was 1050°C as measured by a pyrometer. Silane was used to dope AlGaN epilayers n-type. Initially, a 1 to 2 µm-thick AlN epilayer was grown on (0001) c-plane sapphire substrates mis-oriented 0.2° toward the m-plane to serve as templates for subsequent growth of AlGaN channel HEMTs. After growth, samples were characterized with contactless sheet resistance measurements and capacitance-voltage sweeps to assess pinch-off voltage and electron charge density in the channel. These tests were used to confirm the presence of a two-dimensional electron gas (2DEG) in the HEMTs. Throughout this report, shorthand names in the format of $Y_{barrier}$ / $X_{channel}$ will be used to refer to an $Al_YGa_{(1-Y)}N$ barrier / $Al_XGa_{(1-X)}N$ channel compositions. For example, a HEMT comprised of $Al_{0.85}Ga_{0.15}N$ barrier and $Al_{0.7}Ga_{0.3}N$ channel is called out as an 85/70 HEMT.

A cross-sectional view of an AlGaN-channel HEMT is shown in Fig. 1. The 2DEG conduction path between the source and drain is modulated by the gate electrode. As grown, the AlGaN HEMT is innately depletion-mode (d-mode) and modulates at a negative gate voltage (threshold voltage). Structural modifications to the gate, through processes such as recess etching of the barrier or utilizing a p-AlGaN cap under the gate switch the threshold voltage positive, resulting in enhancement-mode (e-mode) devices.

Device fabrication utilized standard contact lithography and photoresists for all patterning steps. For a typical process flow, a global alignment mark of molybdenum (100 nm) was deposited. If the structure had a p-doped top layer for threshold voltage control, the next step was to perform selective area etching to remove the p-type layer from everywhere but the gate area. Next, source and drain

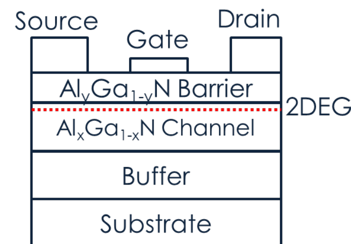

Figure 1. Cross-sectional diagram of a HEMT. AlyGa1-yN barrier / AlxGa1-xN channel.

electrodes made of Ohmic metal [19, 20] consisting of 25 nm Ti / 100 nm Al / 15 nm Ni / 50 nm Au were deposited by electron-beam evaporation and annealed with a rapid thermal annealing (RTA) system for 30 seconds in a 1 mTorr nitrogen atmosphere at 1000°C, unless otherwise noted. Mesa isolation etching was performed in an inductively coupled plasma etching system using boron trichloride, chlorine and argon gases. Next, a 100 nm silicon nitride (SiN) passivation/dielectric layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). Afterwards, selected areas of the SiN were removed to gain access to pre-existing electrodes and the gate regions. To make devices without p-type caps enhancement-mode, a fluorine-based reactive ion etch of the barrier in the gate region was used to shift the device to a positive threshold voltage [7, 21]. Gate metal consisting of either 20 nm Ni /450 nm Au or 200 nm W was then deposited into these openings. Over W pads, a metal layer made of 20 nm Ti / 50 nm Ta / 200 nm Au was deposited to facilitate wire bonding between W and Au wirebonds.

B. Over-Temperature Hall Mobility

Hall characterization samples were fabricated into square Van der Pauw patterns measuring approximately 7 mm per side, with an Ohmic contact on each corner. Ohmic contact metal was electron-beam evaporated onto the samples, and a metal shadow mask patterned each sample. Rapid thermal annealing was used to alloy the contacts.

A Lakeshore 8404 Hall Effect Measurement Setup with an oven insert was used to characterize electron mobility, sheet carrier concentration, and sheet resistance over a broad temperature range. During the measurement, a magnetic field of 0.9 T was applied, the sample chamber was in an argon atmosphere, and tungsten probes were used to contact the samples. Measurements were recorded at steps of approximately 50 ºC: beginning at 30 ºC, progressing to 500 ºC, and returning to 30 ºC; the measured sample temperature was recorded at each step. At the start of each measurement, current-voltage sweeps were used to confirm Ohmic behavior between contacts on the sample.

C. High Temperature Probe Station

For devices grown on substrates with low thermal conductivity (thick sapphire (Al_2O_3) substrates), a large

temperature offset between the devices at the top of the wafer and the chuck temperature under the substrate were accounted for. To characterize the offset, an Al_2O_3 substrate was heated from 50°C to 600°C and thermocouple data were collected from the probe station chuck and top side of the substrate. The tests revealed a maximum temperature offset of 72°C, which was then accounted for in over-temperature device characterization. For all high temperature data collection, the temperature was allowed to stabilize for a minimum of 10 minutes prior to testing. DC electrical sweeps were conducted with a semiconductor parameter analyzer.

D. Inverter Design

All inverters discussed in this report had a d-mode load and e-mode driver configuration. The ratio of gate width (W) over gate length (L) for the e- and d-mode devices within each inverter impacts its electrical characteristics. Equation (1) shows driver-load transconductance ratio [22] and has E and D subscripts that specify enhancement- and depletion-mode transistor values, respectively:

$$\beta_R \propto \frac{W_E/L_E}{W_D/L_D} \quad (1)$$

β_R values of 1.5, 6, and 16 were chosen for this study. A higher β_R reduces the resistance of the E-mode device in the on-state (V_{IN} = high, V_{OUT} = low), allowing for greater modulation of the inverter. Having a variety of β_R values is practical in a high operating temperature test mask because HEMT sheet resistance increases with increasing temperature and higher β_R values may be required for maintaining consistent inverter modulation over a broad temperature range.

III. Results and Discussion

A. Over-Temperature Hall Characterization

For high temperature electronics, it is essential to understand how carrier transport varies over a broad temperature range and is impacted by epitaxial design. This study experimentally characterized temperature-dependent mobility, sheet charge density, and sheet resistance. It is desirable to maximize mobility and sheet carrier concentration, which combine to positively impact (reduce) sheet resistance.

Fig. 2 plots the resulting mobility versus temperature from the Hall characterization for five different samples with barrier/channel aluminum compositions of 26/0, 45/30, 100/60, 86/70, and 85/50. The immediate observation is that mobility reduces with increasing temperature for all epitaxial compositions. Whereas the GaN-channel HEMT experienced a 6.9x mobility reduction, all AlGaN-channel HEMTs only experienced a 3.1x reduction. Therefore, even though AlGaN has overall lower mobility than GaN, its

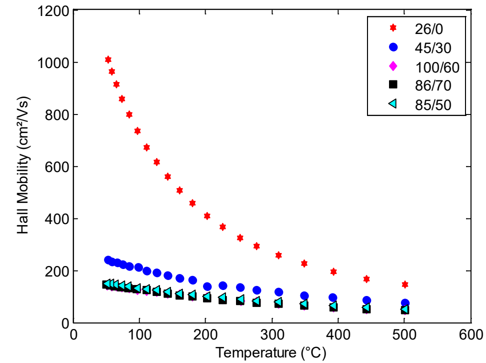

Fig. 2. Mobility versus temperature characterized by Hall measurements for five different HEMT structures.

mobility is less variable over temperature and could provide more stable device operation for variable temperature applications. Among the AlGaN samples, the HEMTs with channel compositions of 50%, 60%, and 70% aluminum had similarly low (~140 cm²/Vs) mobility values. In contrast, the 30% channel HEMT had 1.7x higher mobility (240 cm²/Vs) than the other AlGaN compositions. These results show that for the range of channel compositions studied, channels with lower aluminum compositions have higher electron mobility.

The sheet carrier concentration, where high carrier concentration is desirable to minimize sheet resistance is displayed in Fig. 3. The 100/60 and 85/50 HEMTs have the highest carrier concentrations ($1.6\text{-}1.9 \times 10^{13}$ cm^{-2}) which are about 2x those of the 26/0, 45/30, and 86/70 HEMTs ($4\text{-}9 \times 10^{12}$ cm^{-2}). The 100/60 and 85/50's advantage is due to the large compositional contrast between the barrier and channel. Unlike the mobility, the sheet carrier concentration is relatively stable over a broad temperature range. This high stability makes the carrier concentration an important consideration for high temperature device design. Maintaining a high concentration will ensure low sheet resistance over a broad temperature range and could potentially offset the low mobility disadvantage of the AlGaN channel HEMTs relative to the GaN-channel ones.

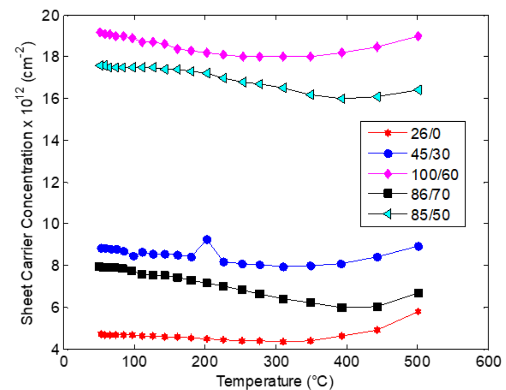

Fig. 3. Sheet carrier concentration versus temperature.

Finally, the sheet resistance extracted from the Hall measurements is displayed in Fig. 4. A high sheet resistance is undesirable, as exemplified in the 85/70 HEMT. The sheet resistance (R_{SH}) is related to mobility (μ) and carrier concentration (n_s) by:

$$R_{SH} \propto \frac{1}{q\mu n_s} \quad (2)$$

where q is electronic charge. All samples other than the 86/70 HEMT exhibited comparable sheet resistance values that trended similarly with increasing temperature. The combination of poor mobility and low carrier concentration generates high sheet resistance epitaxial structures, leading to non-linear current-voltage sweeps that are typical of poor Ohmic contacts. To achieve a desirable sheet resistance and thus linear Ohmic contacts, either mobility or carrier concentration need to be high.

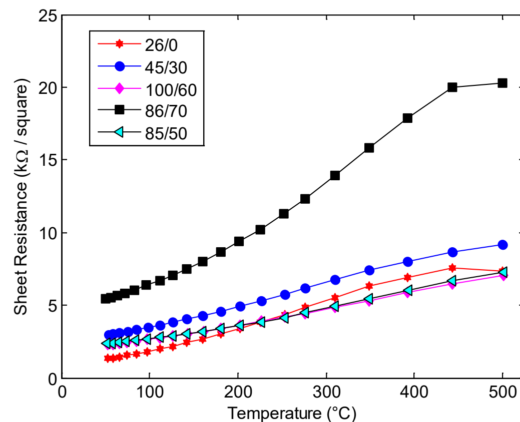

Fig. 4. Temperature-dependent sheet resistance.

B. Gates for High Temperature Electronics

Developing a robust gate process for high temperature electronics is challenging because such environments can change metal properties and thermal cycling can cause delamination. The goal was to identify a gate metal that would work well for high temperature electronics. It was critical that such a gate metal (1) is a Schottky contact to AlGaN that maintains desired electrical and mechanical properties when heated, (2) has good adhesion, and (3) is compatible with process steps. This study evaluated three gate metals by characterizing electrical changes caused by thermal cycling. While not extensive, this investigation identified tungsten (W) as a good candidate gate metal for high temperature applications.

Standard gate metal for III-N HEMTs is 20 nm nickel (Ni) / 450 nm gold (Au) and is intended to be a Schottky contact. After thermal cycling above 300°C, degradation of the gate metallization was observed by optical microscope [23, 24]. Transmission electron microscope (TEM, not shown) imaging of the gate metal revealed heat-induced migration of Ni from the metal-semiconductor (MES) interface to the top of the Au. This migration changes the composition of the MES interface and permanently modifies the electrical properties of the transistor.

To alleviate this problem, we evaluated new gate metals for high temperature applications. Metal selection criteria included work function, low resistivity, and high melting point. Three metal stacks, W (200 nm), Pd (200 nm), and Pt/Au (20 nm / 200 nm) were selected for the investigation. The first task was to identify which electrical characteristics degraded because of thermal cycling and to determine which gate metal was most immune to these degradations. The epitaxy used for this study was an 85/70 HEMT. Gates were patterned, and metal was deposited either by sputtering (W), or evaporation (Pd, Pt/Au). SiN 100 nm thick encapsulated the gates and ohmic metals; openings were etched through the SiN for electrical access points. Each device was electrically characterized, individual die were diced from the main wafer and subjected to a series of 500°C rapid thermal anneals for 10 minutes in nitrogen, and electrically characterized again. Degradation due to thermal cycling was seen with reduced drain-to-source current, changes in on/off current ratio, and threshold voltage shift. Table 1 compares results for each metal. Tungsten (W) had the most favorable results, with a minor reduction in current, improved on/off current ratio after thermal cycling, and an estimated -0.26 V threshold voltage shift. Due to these results, the W gates were selected for use in subsequent high temperature device studies.

Table 1. Summary of gate metal study.

Metal Stack	% I_{DS} Reduction After Thermal Cycle	On/Off Current Ratio Pre-RTA	Post-RTA	Threshold voltage shift (V) from 25°C to 300°C
200 nm W	22%	$3x10^5$	$1.8x10^6$	-0.26
200 nm Pd	50%	$1 x10^8$	$2.8x10^6$	+0.1
20 nm Pt / 200 nm Au	74%	$8 x 10^7$	$5.4x10^8$	-0.04

C. Over-Temperature Device Characterization

Since the combination of e- and d-mode transistors were used to build and demonstrate high temperature inverters, it was critical to examine the over-temperature behavior of both types of discrete HEMTs. Devices were tested on high temperature probe stations spanning chuck temperatures of (1) 25°C to 300°C and (2) 25°C to 600°C. Fig. 5 compares drain current as a function of gate voltage for e- and d-mode 85/70 HEMTs from 25°C to 300°C. In the temperature range examined the threshold voltage was stable and on-off current ratios were greater than $1x10^6$. These metrics show that over-

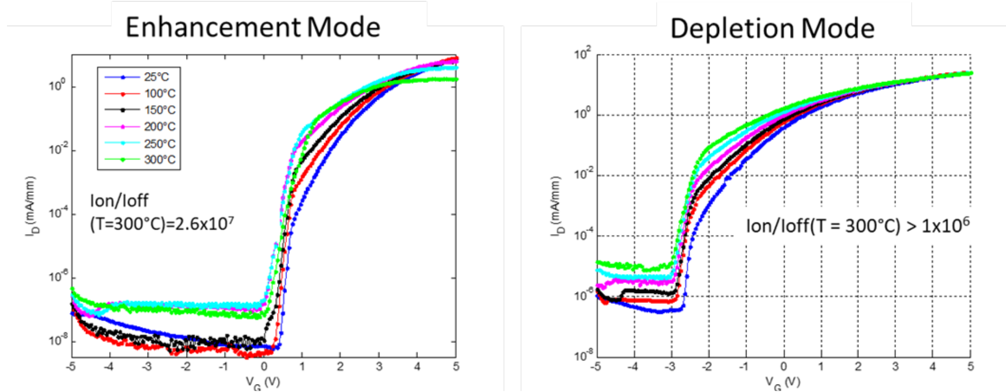

Fig. 5. 85/70 HEMT logscale plots of drain current versus gate voltage for both e- and d-mode devices from room temperature to 300°C. E-mode HEMTs exhibit a reduction in drain current above 200°, not seen in d-mode devices.

temperature these discrete devices have both sufficient modulation and a relatively invariant threshold voltage. However, also revealed within these measurements was a drain current degradation of the e-mode device starting above 200°C, that was not observed for the d-mode HEMT (for T = 25 – 300°C). This was problematic because in an inverter circuit with both e- and d-mode devices, only the resistance of e- mode transistor would independently rise, effectively reducing the inverter β_R with increasing temperature.

Fig. 6 shows results of high temperature inverter voltage transfer curves for (A) 85/70 HEMTs with e-mode devices fabricated by barrier recess etching and (B) 45/30 HEMTs with e-mode devices fabricated with a p-AlGaN capped barrier under the gate. For both inverters, β_R was 16.

Two shortfalls are seen in the 85/70 HEMT data. First, the output low voltage (V_{OL}) is high (about 1.5 V) at room temperature, indicating that the e-mode driver is resistive compared to the d-mode load. This is a consequence of the high sheet resistance (6500 Ω/sq) of the 85/70 HEMT. The high resistance can be reduced by dropping the aluminum composition of the channel, which will increase both the mobility and carrier concentration. Alternately, increasing β_R by layout modifications would also reduce driver resistance. Second, as the temperature increases the V_{OL} begins to rise (degrade) above 200°C, which results from the imbalance created by the decreasing e-mode HEMT drain current with increasing temperature, relative to the stable d-mode drain current. This effect can be alleviated by making the threshold voltages of the driver and load closer in value, and by targeting a driver threshold voltage near zero.

In contrast, the 45/30 HEMT resulted in a more desirable inverter. The sheet resistance is relatively low because of the reduced aluminum composition in the channel, which pushes the room temperature V_{OL} down to about 0 V. Also, since the driver threshold voltage is near 0 V, the V_{OL} stays low as the temperature is increased. One downside is that the low inverter threshold voltage will require level shifting, which for a real application entails adding negative voltage biasing that increases overall circuit complexity. A post thermal cycle sweep overlays well with the initial sweep, indicating that thermal cycling did not significantly modify the

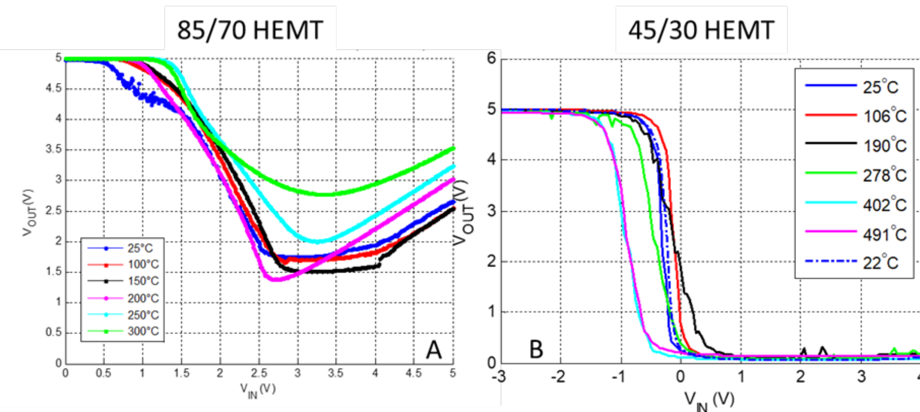

Fig. 6. Inverter over temperature results for: (A) 85/70 HEMT with β_R = 16 and recessed barrier etching E-mode devices tested from 25°C to 300°C and (B) 45/30 HEMT with β_R =16 and p-AlGaN capped E-mode devices tested from 25°C to 491°C.

inverter's electrical properties from its starting point.

IV. Conclusions

AlGaN HEMT-based logic gates and epitaxial structures were designed and tested for direct insertion into high temperature environments. The over-temperature Hall characterization revealed that although AlGaN HEMTs have lower mobility than GaN-channel HEMTs, they have more stable transport properties from 25°C to 500°C. Gate metals were evaluated for high temperature operation and W was selected. A mask set consisting of simple inverting logic gates and their discrete constituent transistors was designed for high temperature device testing. Combined enhancement/depletion-mode transistors were used to implement inverter gates. Finally, operation of AlGaN-based HEMT logic gates were demonstrated from room temperature to 500°C. The efforts from this project have established a foundation for more advanced high-temperature AlGaN HEMT circuitry maturation.

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References

[1] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-Temperature Electronics—A Role for Wide Bandgap Semiconductors?," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 1065 - 1076, 2002.

[2] T. Nanjo *et al.*, "AlGaN channel HEMTs on AlN buffer layer with sufficiently low off-state drain leakage current," *Electronics Letters,* vol. 45, no. 25, 2009.

[3] T. Nanjo *et al.*, "First Operation of AlGaN Channel High Electron Mobility Transistors," *Applied Physics Express* vol. 1, no. 011101, 2008.

[4] N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, H. Tokuda, and M. Kuzuhara, "AlN/AlGaN HEMTs on AlN substrate for stable high-temperature operation," *Electronics Letters,* vol. 50, no. 3, pp. 211-212, 2014.

[5] H. Tokuda *et al.*, "High Al Composition AlGaN-Channel High-Electron-Mobility Transistor on AlN Substrate," *Applied Physics Express,* vol. 3, no. 121003, 2010.

[6] A. G. Baca *et al.*, "An AlN/Al0.85Ga0.15N high electron mobility transistor," *Applied Physics Letters,* vol. 109, no. 033509, 2016.

[7] B. A. Klein *et al.*, "Enhancement-mode $Al_{0.85}Ga_{0.15}N/Al_{0.7}Ga_{0.3}N$ high electron mobility transistor with fluorine treatment " *Applied Physics Letters,* vol. 114, no. 112104, pp. 112104-1,5, 2019.

[8] A. G. Baca *et al.*, "Al0.85Ga0.15N/Al0.70Ga0.30N High Electron Mobility Transistors with Schottky Gates and Large On/Off Current Ratio over Temperature," *ECS Journal of Solid State Science and Technology,* vol. 6, no. 12, pp. Q161-Q165, 2017.

[9] A. G. Baca *et al.*, "High Temperature Operation of Al0.45Ga0.55N/Al0.30Ga0.70N High Electron Mobility Transistors " *ECS Journal of Solid State Science and Technology,* vol. 6, no. 11, pp. S3010-S3013, 2017.

[10] E. A. Douglas *et al.*, "Ohmic contacts to Al-rich AlGaN heterostructures," *Physica Status Solidi A,* vol. 214, no. 8, 2017.

[11] A. G. Baca *et al.*, "RF Performance of $Al_{0.85}Ga_{0.15}N/Al_{0.70}Ga_{0.30}N$ High Electron Mobility Transistors with 80 nm Gates," *IEEE Electron Device Letters,* vol. 40, no. 1, pp. 17-20, 2019.

[12] A. M. Armstrong *et al.*, "Ultra-wide band gap AlGaN polarization-doped field effect transistor," *Japanese Journal of Applied Physics,* vol. 57, no. 074103, 2018.

[13] H. Xue *et al.*, "$Al_{0.65}Ga_{0.35N}/Al_{0.4}Ga_{0.6}N$ Micro-Channel Heterojunction Field Effect Transistors With Current Density Over 900 mA/mm," *IEEE Electron Device Letters,* vol. 41, no. 5, pp. 677-680, 2020.

[14] H. Xue *et al.*, "$Al_{0.75}Ga_{0.25}N/Al_{0.6}Ga_{0.4}N$ heterojunction field effect transistor with f_T of 40 GHz," *Applied Physics Express,* vol. 12, no. 066502, 2019.

[15] S. Bajaj, F. Akyol, S. Krishnamoorthy, Y. Zhang, and S. Rajan, "AlGaN channel field effect transistors with graded heterostructure ohmic contacts," *Applied Physics Letters,* vol. 109, no. 133508, 2016.

[16] S. Bajaj *et al.*, "Graded AlGaN Channel Transistors for Improved Current and Power Gain Linearity," *IEEE Transactions on Electron Devices,* vol. 64, no. 8, pp. 3114-3119, 2017.

[17] S. Bajaj *et al.*, "High Al-Content AlGaN Transistor With 0.5 A/mm Current Density and Lateral Breakdown Field Exceeding 3.6 MV/cm," *IEEE Electron Device Letters,* vol. 39, no. 2, pp. 256-259, 2018.

[18] S. Muhtadi *et al.*, "High Electron Mobility Transistors With Al0.65Ga0.35N Channel Layers on Thick AlN/Sapphire Templates," *IEEE Electron Device Letters,* vol. 38, no. 7, pp. 914-917, 2017.

[19] B. A. Klein *et al.*, "Planar Ohmic Contacts to $Al_{0.45}Ga_{0.55}N/Al_{0.3}Ga_{0.7}N$ High Electron Mobility Transistors," *ECS Journal of Solid State Science and Technology,* vol. 6, no. 11, pp. S3067-S3071, 2017.

[20] G. Greco, F. Iucolano, and F. Roccaforte, "Ohmic contacts to Gallium Nitride materials," *Applied Surface Science,* vol. 383, pp. 324-345, 2016.

[21] Yong Cai, Yugang Zhou, Kei May Lau, and K. J. Chen, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment:From Depletion Mode to Enhancement Mode," *IEEE Transactions on Electron Devices,* vol. 53, no. 9, pp. 2207-2215, 2006.

[22] J. P. Uyemura, *Fundamentals of MOS Digial Integrated Circuits*. Reading Massachusetts: Addison-Wesley Publishing Company, 1988.

[23] P. H. Carey *et al.*, "Operation Up to 500°C of Al0.85Ga0.15N/Al0.7Ga0.3N High Electron Mobility Transistors," *Journal of the Electron Devices Society,* vol. 7, pp. 444-452, 2019.

[24] P. H. Carey *et al.*, "Extreme Temperature Operation of Ultra-WideBandgap AlGaN High Electron Mobility Transistors," *IEEE Transactions on Semiconductor Manufacturing,* vol. 32, no. 4, pp. 473-477, 2019.