Location dependent down-rating of voids in high power solder connections for automotive power modules

Bettina Ottinger[1], Simon Murk, Sebastian König[1], Antonio Zangarro[1], Michael Müllmaier[1], Dr. Lars Müller[1], Prof. Dr. Jörg Franke[2]

Vitesco Technologies Germany GmbH, Nordostpark 76, D-90411 Nuernberg, Germany [1]
Institute for Factory Automation and Productions Systems, Friedrich-Alexander University, Fuerther Straße 246b, D-90429 Nuremberg, Germany[2]
bettina.ottinger-EXT@vitesco.com

Abstract

The development of cost-effective, void- and lead-free high-power die attach for automotive power modules has been a major challenge for the last decades. Particularly voids at the die attach have the potential of reducing the lifetime of the interconnection between the die and the direct copper bonded (DCB) substrate demonstrably, caused by overheating of the die [1]. This study evaluates a method to determine the influence of the void position and size on the local thermal resistance of the solder interconnection. The formular of the local thermal resistance generated by using FEM simulation shows, that the permitted local maximum void size depends on the position of the void. The defined correlation factor reduces the individual void areas according to their position and thus the permitted thermal resistance is not exceeded.

Key words

die attach, FEM, location, power module, soldering, voids

I. Introduction

Voiding between die and DCB substrate is one of the major reliability concerns because of local thermal hotspots, runaway of electrical parameters and localized stress concentration [2]. Different complex factors affect the void formation and make it difficult to avoid the formation of voids during manufacturing process. The primary cause of void formation during reflow soldering is the outgassing formed by reactions among the materials and fluxes. Other causes could be poor wetting of the solder due to contamination, surface defects or solder flux residues. In terms of thermal properties, voids at the die attach have a negative impact on the thermal performance of the component [3-5]. Usually, the voids are filled with gas e.g., nitrogen. Since the thermal conductivity of nitrogen (0.026 W/mK) [6] is significantly lower compared to soft solder materials for example SAC305 (58.7 W/mK) [7], the presence of voids decreases the local heat dissipation in the solder layer between die and DCB substrate. Due to the lower heat dissipation, local temperature hotspots can arise which lead to the destruction of the component [8]. Therefore, a limited void ratio of approximately 5% - 10% of the connection area over the entire die is usually required in the industry [9]. The limited void ratio is commonly defined by a worst-case study on the maximum thermal void impact. It often results in high product cost and scrap rates [10]. Various researchers studied the influence of voids on thermal performance of different electronic packages. Chang. et al. [9] investigated the effect of the void size and location on the thermal resistance of power devices using 3D finite element modeling. The study suggested an increase of chip temperature and thermal resistance with the increase of void percentage. Chen et al. [10] concerned the thermal impact of randomly distributed solder voids. An analytical expression describing the additional thermal resistance caused by voids as a function of thickness, die area and void radius was found. Otiba et al [3] used numerical studies to investigate the thermal impact of various void configurations and the void location. The results showed that a large single void has more impact on the thermal resistance compared to many small distributed voids of equivalent void percentage. For the void location it was determined that the highest thermal resistance occurs near the center of the heat source.

This study investigates the thermal impact of the void size at defined positions via finite element modeling (FEM). A polynomial equation between the local thermal resistance and the void position could be found to calculate the permitted local void size individually and therefore provide a way to either increase yield or power rating.

II. FEM Simulation and the local thermal resistance Rth*

The FEM simulation is used to evaluate the influence of the position and size of the void on the thermal resistance. Therefore, the local thermal resistance (Rth*) was simulated with a FEM model. The model consists of a silicon IGBT, SAC305 solder layers, direct copper bonded (DCB) substrate and an aluminum cooler (Fig.1 and table 1).

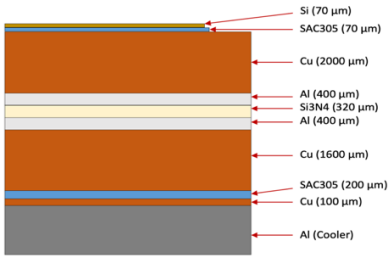

Figure 1: Schematic cross section of the FEM simulation model

Table 1: Material properties [11]

Material	Material properties		
	Density $\frac{kg}{m^3}$	Thermal conductivity $\frac{W}{m*K}$	Specific heat $\frac{J}{kg*K}$
Si (IGBT)	2330	90	80
SAC305 (solder)	7250	60	230
Cu (DCB)	8930	385	395
Al (DCB)	2689	237.5	951
Si_3N_4 (DCB)	3220	65	724
Al (Cooler)	2730	160	892

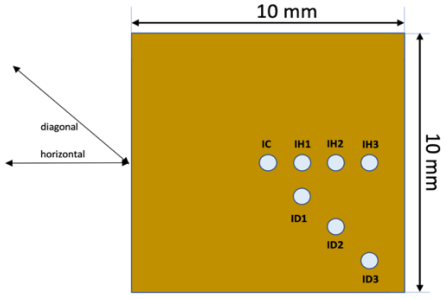

Figure 2: Schematic drawing of the void position in horizontal and diagonal displacement

The voids were set between the IGBT and the DCB substrate as shown in Fig. 2. There is one void in the center (IC) of the IGBT. Additional three voids with defined distances have been placed in lines horizontally (IH1-IH3) and diagonally (ID1-ID3) from the center. The simulated circular voids are extended cylindrically through the entire solder layer. During the simulation, only one void in each chip area was active and filled with air. The remaining voids were filled with solder and had no influence on the results. The local thermal resistance $R^*_{th}$was determined from the center of the void. The simulation was conducted for three void sizes (0 mm^2, 0.5 mm^2 and 1.5 mm^2). A uniform chip and solder thickness as well as an even power dissipation over the entire die surface was assumed.

At first the influence of the position was determined. Successively the position dependent local thermal resistance (R^*_{th}) was measured individually. The simulated R^*_{th}values with and without voids were then plotted against the distance from the die center along the horizontal and diagonal cutting lines. The graph of R^*_{th} without voids (solid black) is the reference on which the graphs for voids were placed at the corresponding void positions (red, purple, blue and green). By connecting the maxima of the individual void graphs, a graph for the change of the local thermal resistance with voids could be approximated. This was done for the horizontal and diagonal displacement (black dashed). The shape of the modeled graph corresponds to the reference graph without voids, but with a different Y-offset. The figure 3 shows diagrams for the simulation with a void size of 0.5 mm^2 after horizontal (a) and diagonal (b) void displacement.

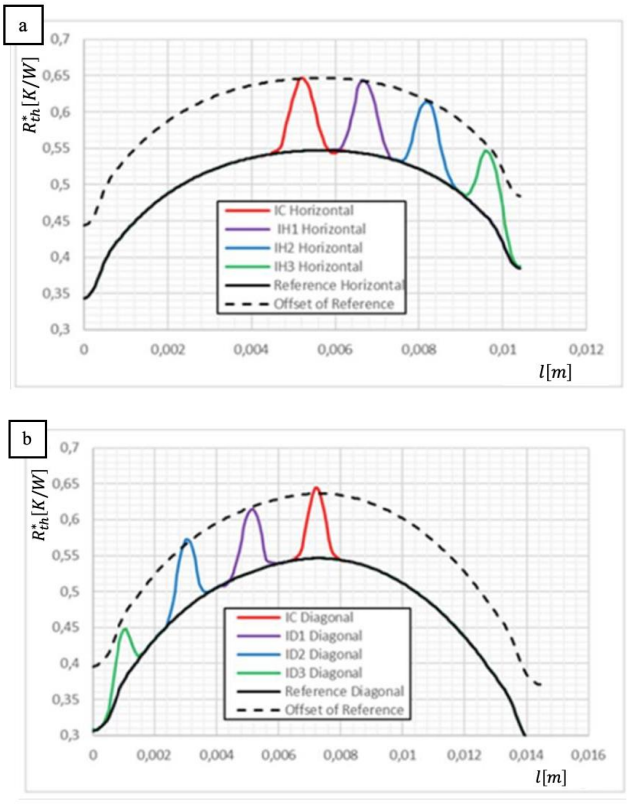

*Figure 3: Rth*across the die surface after horizontal (a) and diagonal (b) displacement (void size 0.5 mm^2)*

The simulation was then repeated with a void size of 1.5 mm^2. Figure 4 summarizes the modeled graphs of the IGBT for horizontal and diagonal displacement with void sizes of 0 mm^2, 0.5 mm^2 and 1.5 mm^2 and the graphs were fitted with a 2nd degree polynomial equation (figure 4). The fitted parabolic graphs of the different void sizes were almost identical in shape and only shifted on the Y-axis.

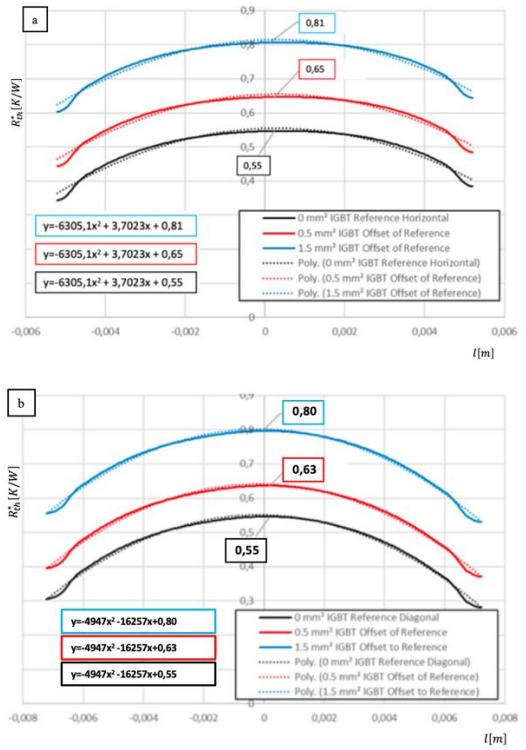

*Figure 4: Simulated R_{th}*values and the fitted parabolic graphs for different void sizes after horizontal (a) and diagonal (b) displacement*

By means of linear regression analysis a function to describe the offset of the graphs for the horizontal shift was determined:

$$R^*_{th}(x, A_{void}) = 0{,}174 * A_{void} + R^*_{th,0}(x) \quad (1)$$

and

$$R^*_{th,0}(x) = -6305.1 * x^2 + 3.70 * 2 + R^*_{th,max,0}(x) \quad (2)$$

Where R^*_{th} is the local thermal resistance at a certain location, A_{void} is the size of the void, $R^*_{th,0}$ is the thermal resistance at a certain location without void, $R^*_{th,max,0}$ is the maximum void free thermal resistance of the die at its center (= 0.5544 K/W) and x is the distance from the die center. For the fitted graphs of the different void sizes in diagonal shift the same method was applied. It results the universal polynomial equation (3), where the parameters a, B and C must be selected from table 2 depending on the direction of displacement.

$$R^*_{th}(x, A_{void}) = B * x^2 + C * a * A_{void} + R^*_{th,max,0}(x) \quad (3)$$

Table 2: Parameters for the universal polynomial equation

die	shift	a $\frac{K}{m^2} * W$	B $\frac{K}{m^2}$	C $\frac{K}{W} * m$	$R_{th,max,0}$ $\frac{K}{W}$
IGBT	horizontal	0.1714	6305	3.7	0.56
	diagonal		4947	1.6	

Initially polynomials had been obtained for voids placed horizontal or diagonally across the die. In order to simplify the calculation, the diagonal polynomial was used to calculate a correlation factor for the complete area of the die.

III. Maximum void size and the correlation factor

The FEM simulation for the local thermal resistance of voids has shown that the local thermal resistance is strongly dependent on the position of the void. Using the universal polynomial equation for R^*_{th} the permitted maximum local void size can be calculated according to their position, assuming the worst-case value for the local thermal resistance ($R^*_{th,max}$) on the entire die area. The maximum permitted $R^*_{th,max}$ describes the value that a void creates in the center of the IGBT with the limited void size (A_{limit}). The $R^*_{th,max}$ for a void in the center of the IGBT with distance ($x = 0$) can be calculated:

$$R^*_{th,max}(A_{limit}) = a * A_{limit} + R^*_{th,max,0} \quad (4)$$

Further the obtained formula for R^*_{th} was rearranged for the permitted local maximum void size $A_{void,max}$ and 4 was insert in 5:

$$A_{void,max}(x, A_{limit}) = \frac{R^*_{th,max}(x,A_{limit}) - B*x^2 - C*x - R^*_{th,max,0}}{a} \quad (5)$$

$$A_{void,max}(x, A_{limit}) = \frac{a*A_{limit} - B*x^2 - C*x}{a} \quad (6)$$

Equation 6 allows the calculation of the permitted local maximum void size using the maximum $R^*_{th,max}$ obtained from FEM simulation which does not violate maximum temperature limits in the hotspot. To determine the local correlation factor k, the limited void size A_{limit} has to be divided by the permitted local maximum void size $A_{void,max}$.

$$k = \frac{A_{limit}}{A_{void,max}(x,A_{limit})} = \frac{a*A_{limit}}{a*A_{limit} - B*x^2 - C*x} \quad (7)$$

So the correlation factor k can be calculated and be used to grade all voids according to their location. Figure 5 shows the distribution of the correlation factor over the IGBT area with $A_{limit} = 0.8 * 10^{-6} m^2$ mapped over the die area.

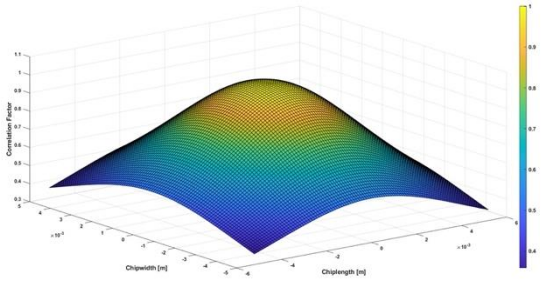

Figure 5: 3D mapping of the position dependent correlation factor for the IGBT area

IV. Summary and Conclusion

This study evaluates a method to estimate the local influence of the void position and size on the thermal resistance of the solder interconnection.

First, the influence of position and size of the void on the thermal resistance was simulated. A correlation between the position and size (local overheating) of the void was found and could be described by a polynomial equation. From the parameters of the polynomial equations and the linear regression analysis an equation could be determined to calculate the local thermal resistance (R^*_{th}) values in the solder layer according to the position and void size. With the FEM simulation and the resulting formula, the local thermal resistance in thermal hotspots (voids) could be estimated. Afterwards the obtained formula for R^*_{th} was rearranged for the permitted local maximum void size ($A_{void,max}$). This equation allows the calculation of the local permitted maximum void size using the R^*_{th}obtained from the FEM-simulation whereby the maximum valid temperature limit in the hotspot is not exceeded.

By using the ratio of the limited void size A_{limit} and the permitted local maximum void size $A_{void,max}$ the correlation factor k is defined. The correlation factor reduces the individual void areas according to their position and thus the prevailing thermal resistance. Hence the factor can then be mapped to the whole die and be used by inspection systems either to increase production yield or to allow for higher maximum design currents by setting higher maximum void limits.

Despite the contribution of this work, there are clear opportunities to make additional advances. Further investigations are focused on preparation regarding the solder materials, die attach thickness and die geometry.

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