Additive Prototyping for Rapid Circuit and Interface Development at 200°C+

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Abstract

A major challenge in the process of designing analog and digital circuits for high-temperature applications is the usefulness and completeness of information supplied by component manufacturers. The models supplied in datasheet packages require verification and/or extension to be integrated into systems that function at or above 200°C. Between 85°C and 175°C this activity is accomplished through breadboarding and population of bespoke printed circuit boards respectively. Before investing in a fabrication run, rapid additive prototyping can be used to verify designs and inform designers if modification is required. Additively manufactured modules can also interface with final products and can be easily integrated with other high temperature modules such as Ozark IC's XNode® single board high-temperature computers. The materials used for fabrication of the high-temperature prototype module are selected in a manner that is compatible with the components used for fabrication. Compatible materials are required for all interfaces; connector-to-board, board-to-passive, board-to-wirebond, and wirebond-to-die. Using proper materials and packaging techniques, operation at 200°C for over 7000 hours has been achieved. Ozark IC has developed a post-fire process that allows for maskless single-layer board fabrication, from design to electrical test, in less than one week. Currently in development is an additive dielectric deposition process, which will enable multilayer board fabrication using commercially available metal and dielectric inks. This process was used to fabricate a Resistance Temperature Detector readout function (RTD board) with the dimensions of 5 cm X 5 cm which was then integrated with an XNode AQ200 module and tested at temperatures up to 200°C. This material system was used to fabricate the single-layer and multilayer additively manufactured substrates which have tested successfully at temperatures up to 800°C.

Key words

Additive manufacturing, high-temperature electronics, reliability testing, quick turn manufacturing

I. Introduction

The emerging application space of high-temperature electronics is demanding rapid development of circuit IP and accumulation of high temperature testing data [1]. Many of the components, active and passive, that are available for purchase off the shelf do not provide detailed enough datasheets or models for real world applications. It is frequently possible to extend the temperature range of these devices, sometimes at the expense of component lifetime. Being able to gather this information quickly and inexpensively is a major differentiating factor in the "first-time right" design and cost-effectiveness of manufacturing high temperature electronics[2].

II. Manufacturing Methods for Circuit and Material Testing

A. Traditional Methods for Fabrication

While not subtractive in nature, screen printing fabrication of test boards is identical to mass manufacturing techniques. The manufacturing of the screens is subtractive with 5-sigma patterning quality at a grid scale of 50 microns. Consequently, the non-recurring expenses (NRE) related to material and equipment setup introduce both expense and significant cycle time in the design-to-test loop. Screen printing is typically the method that is used to pattern the conductive inks and/or dielectrics onto the substrates, which are then dried, fired, and inspected for yield.

Most design companies do not have the capability to produce screens and stencils in-house, which are required for the patterning of metal layers and vias respectively, as the processing overhead to support that capability can be impractical. Thus, each new design that an engineer wishes to test, or each component or die that an engineer wishes to model, would require a new order for the NRE materials to fabricate the design in the material system of their choosing. This waiting and expense is incurred between each revision cycle.

B. Advantages of Additively Manufactured Substrates

Removing the requirement for NRE such as screens and stencils in the design-to-test loop offers substantially faster IP development. Shown in Figure 1 is an overview of the process flow that compares the differences between traditional manufacturing for test and additive prototyping.

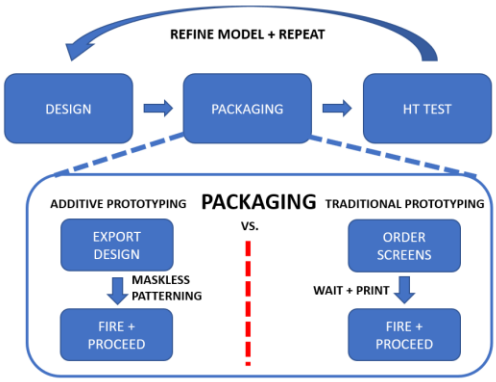

Figure 1: Process flow diagram for design-to-test loop comparing traditional methods vs. additive manufacturing methods.

The critical change in the fabrication flow is the removal of the NRE requirements for screen printing that enables execution of full design-to-test cycles in as little time as one working week. This approach has enabled Ozark IC to build a large database of temperature performance data for a wide variety of both passive and active components for use in high-reliability circuit designs.

The equipment that is used for the maskless patterning of the designed circuits is an NScrypt 3DN tabletop dispensing system[3]. This system enables direct-write printing of designs at resolutions substantially higher than traditional dispensing systems. Shown in Figure 2 is the system as installed in Ozark IC's fabrication laboratory. The footprint and overhead of this system offers substantial advantages vs. the facility requirements and safety considerations to install screen and stencil fabrication in-house.

Figure 2: NScrypt 3DN tabletop system installed in Ozark ICs fabrication laboratory.

Figure 3 is a close-up of the direct write printing process of the Nscrypt system. This layout was then populated and tested at 200°C. The results from this test are presented in the next section.

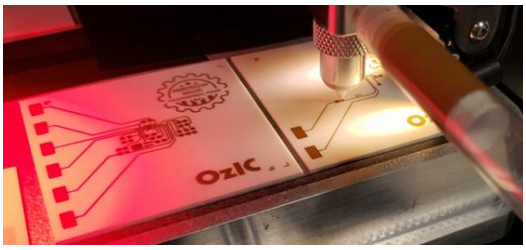

Figure 3: Direct-write deposition of test structure in-progress on the Nscrypt 3DN tabletop system.

C. Experimental Results for Single-Layer Additively Manufactured Prototype Circuits

The circuit shown being printed in Figure 3 was populated and packaged (Figure 4). The substrate size of the device in Figure 4 is 2.5 cm 2.5 cm.

Figure 4: Finished circuit after component attach and wirebonding.

This circuit contains passive components as well as active components for a resistance temperature detector (RTD) readout and provides a complete temperature sensing solution for extreme environments. Ozark IC can complete all the packaging steps in-house. This experiment allowed the design engineer to calibrate the RTD in the design at low expense, targeting a known gap in understanding which can then be filled to build the full electronics module with improved confidence. Design rules were then codified into an additive ceramic Process Design Kit (PDK) to facilitate design automation activities [4]. The results from this experiment are shown in Figure 5, which shows the temperature measured at the test location in the oven vs. the analog to digital converter (ADC) counts reported by the device under test (DUT).

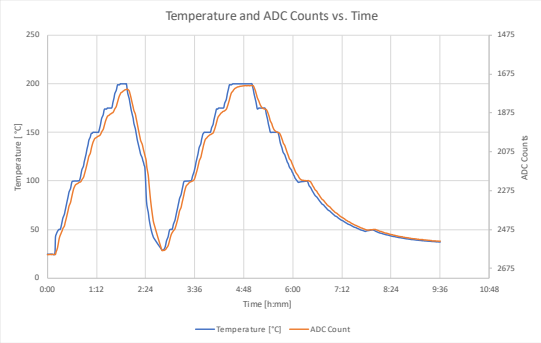

Figure 5: Temperature and ADC counts vs. time.

Temperature was raised in 50°C increments up to a maximum temperature of 200°C. The test was then repeated, and held for 1 hour at 200°C. The ADC counts (orange) lag the measured temperature (blue) inside the oven, as the circuit is printed atop a ceramic substrate which will delay the heating of the surface-mounted RTD.

III. Multilayer Substrates

Multilayer substrates are currently in development and offer substantial benefits over single layer printed modules. The addition of a dielectric layer enables integration of more sophisticated circuits on a single substrate at the cost of manufacturing complexity, but additive deposition of the metal layers is still possible with this system. The multilayer system also enables lower leakage currents between parallel traces, even at extreme temperatures as high as 800°C, which may be useful for high fidelity, low noise systems in extreme environments. Hardware validation through manufacturing and at high-application development is discussed next.

Additionally, the NScrypt is capable of via-less integration, where metal layers are printed over the edge of the dielectric region. Traditional vias can be formed with this system, if desired, but screens and stencils would need to be ordered to pattern those structures. Theoretically the maskless direct-write system could be used to fabricate vias, but process control would need to be improved to realize high enough yield to make such a process practical.

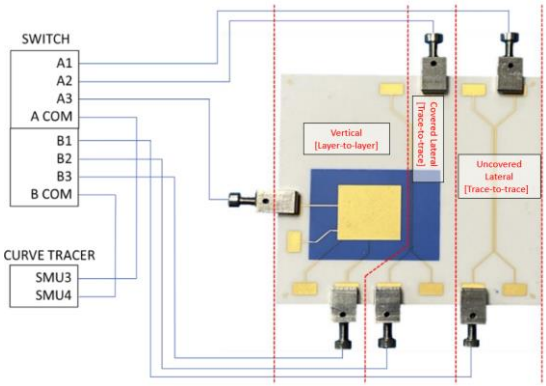

Figure 6: Multilayer additively manufactured material system test substrate.

To evaluate the temperature performance of the multilayer additively manufactured material system, Ozark IC designed and fabricated the substrate shown in Figure 6 on a 5 cm x 5 cm ceramic substrate. This substrate includes three main test features, each intended to demonstrate an important aspect of the thermal performance of the multilayer additively manufactured material system. The terminals on this device have been previously tested to verify their thermal performance, and have been demonstrated not to have any measurable effect on the DUT [5].

Firstly, there is the structure referred to as “VERT,” a vertical structure comprised of two large metal pads separated by the dielectric material. This vertical structure is intended to extract material constants such as dielectric constant “k,” leakage current, and maximum electric field over temperature. This structure mainly describes the thermal and electrical characteristics of interlayer effects.

The remaining two structures on this test substrate are to test interlayer trace to trace leakage, and they are labeled “LAT_AIR” and “LAT_COV”. The LAT_AIR structure consists of two traces, printed at minimum design rule spacing and exposed to air (unpassivated) for the length that the two traces are at minimum spacing. The LAT_COV structure is similarly designed to the LAT_AIR structure, however this structure is covered by the same dielectric that composes the VERT structure in the

design. The purpose of these two structures is to extract what effect, if any, there is on intralayer metal traces when covered by a dielectric material. The "via-less" metal stepover printing fidelity is shown in Figure 7.

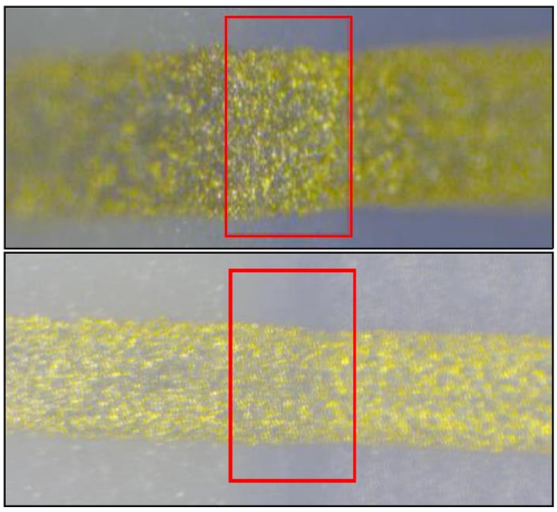

Figure 7: "Via-less" metal stepover feature at minimum space and trace. Micrographs taken at 100X magnification at 45-degree angle (top) and orthogonal (bottom) relative to surface.

The micrographs shown in Figure 7 are taken at two angles to verify the continuity of the trace as it steps over the dielectric boundary. This process enables maskless deposition of subsequent metal layers on top of deposited dielectric layers.
This circuit was then thermally tested according to the profile shown in Figure 8.

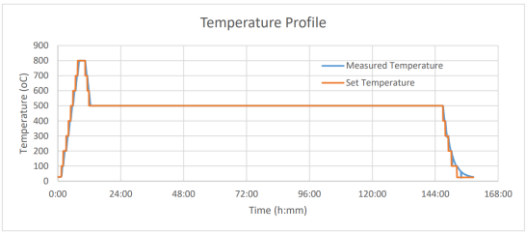

Figure 8: Multilayer additively manufactured substrate temperature test profile.

The sample was brought to 800°C in 100°C steps, with dwell times of 15 minutes at each step to equilibrate and extract circuit performance over temperature. The sample was then held at 500°C for 141 hours in the first run, and 138 hours for the second run. Extracted resistances and leakage currents are shown in Figure 9.

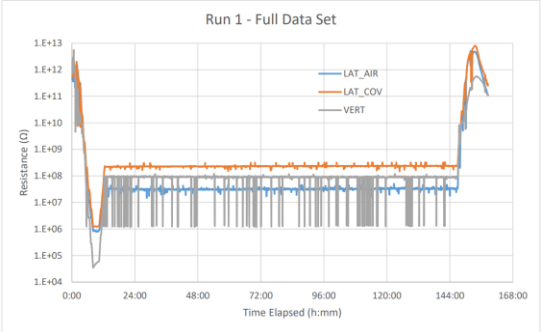

Figure 9: Resistance measurements vs. time for multilayer additively manufactured test substrate.

Analyzing the resistance of the three test structures at 500°C, the lowest resistances (highest leakage) are seen in the LAT_AIR structure, shown in blue. The LAT_COV structure has the highest resistance of the structures measured at 500°C, and the VERT structure is the second most resistive. This test was held at 500°C for 141 hours, and no substantial change in the resistances was observed. This test was also repeated for a second time for 138 hours at 500°C and allowed to cool completely to room temperature between tests. No shift in performance was noted between the two tests.
Notably, at 800°C the vertical structure begins to leak substantially more than the two lateral structures, and the benefits of the dielectric covering begin to diminish. The resistances of the LAT_AIR and LAT_COV structures are not as significantly different, but the LAT_COV structure still shows improved performance. If the performance of a vertical structure is required for a given circuit design, then the thickness of the dielectric layer could be increased; otherwise, the interlayer leakage can be avoided by instantiating a design rule that requires vertical metal trace staggering.

IV. Conclusion

Ozark IC has demonstrated the viability of rapid prototyping materials systems; both single layer and multilayer circuits can be fabricated, as required. The fabrication techniques can be modified to suit the requirements for thermal hardness of these test circuits, and results have been presented that demonstrate the practical benefits of developing high-reliability, high-performance modules through inexpensive and rapid subcircuit validation at temperature. The limited selection and performance of available components requires every individual component and integration method to be tested at temperature to ensure proper and expected function [2].

This design and fabrication methodology enables the accumulation of a library of models to support further circuit development in the high-temperature space that might otherwise be impractical or impossible due to the time and expenses that would be required to build the database. The time and effort expended performing this modeling is often recovered when complex circuits involving a dozen or more screens and stencils, as well as expensive materials, are committed to a manufacturing run.

Acknowledgment

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References

[1] A. M. Francis, “Smart Nodes for High Temperature: Design, Process and Integration (Invited Keynote),” presented at the High Temperature Electronics Conference (HiTEC), Online, Apr. 27, 2021. [Online]. Available: https://imaps.org/technology_crossover_agenda.php

[2] J. Kupernik, M. Bakowski, C. Nicholas, B. Matthew, D. Brandon, and A. M. Francis, “Advancing Reliable High-Temperature Electronics Through Compatible Material Interfaces,” *International Symposium on Microelectronics*, vol. 2022, no. 1, Fall 2022.

[3] “3Dn Series – nScrypt.” https://www.nscrypt.com/3dn-series/ (accessed Jun. 23, 2020).

[4] J. Holmes, A. M. Francis, I. Getreu, and M. Glover, “A Unified ASIC and LTCC Module Design Kit for High-Temperature High-Density Circuits,” in *Proc. of Ceramic Interconnect and Ceramic Microsystems Technologies*, May 2016, vol. 2016, pp. 000169–000172. doi: 10.4071/2016CICMT-WP43.

[5] N. Chiolino, A. M. Francis, J. Holmes, M. Barlow, and C. Perkowski, “470 Celsius Packaging System for Silicon Carbide Electronics,” *Additional Papers and Presentations*, vol. 2021, no. HiTEC, pp. 000083–000088, 2021.