Gate Driver Design in 180 nm SOI CMOS Process for Heterogeneous Integration Inside SiC Power Module

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Abstract

This paper presents the design and test results of a non-isolated single-channel gate driver for heterogeneous integration inside a SiC power module. The driver is designed on a 180 nm silicon-on-insulator (SOI) CMOS process that can safely operate up to 175ºC, most likely even beyond this figure, to survive at the expected junction temperature. The gate driver consists of four pull–up (PMOS) slices and four pull-down (NMOS) slices placed in parallel as the current sourcing and sinking components. Each slice can be activated individually through a controller block, making the gate driver's drive strength variable. To mitigate the parasitic turn-on effect due to the Miller capacitor, an active Miller clamping circuit is integrated with the driver without overly compromising the device's switching performance. Under-voltage lockout (UVLO) is another key feature of this driver that ensures the system is protected against bias supply failure. A desaturation detection scheme is also integrated with the gate driver as a system protection feature to detect excessive current flowing through the power devices. The gate driver die area is approximately 5.4 mm x 3.3 mm with a pad area of 100 µm x 100 µm suitable for wire bonding inside the module.

Key words

Gate driver IC, heterogenous integration, high-temperature electronics, SiC power module, SOI CMOS process.

I. Introduction

The movements toward electrification in transportation systems like electric aircraft and vehicles and hybrid electric vehicles pose a serious challenge to future power electronic converters [1]–[3]. SiC devices can be a promising candidate to meet these challenges, featuring normally off-state, lower conduction and switching loss, expanded operating temperature capabilities, higher thermal conductivity, and breakdown voltage [4]–[8]. However, to avoid probable oscillation across the power devices resulting from faster switching inside the SiC power module, the interconnect parasitics between the module housing and the gate driver need to be minimized as much as possible. Gate driver integration inside the module can reduce the stated effects to a large extent. Also, by eliminating the need for aggressive active and passive cooling systems for such a heterogeneously integrated system, higher power-to-volume and power-to-weight ratios can be achieved. Conventional silicon-based gate drivers fail to survive at such a high junction temperature in SiC modules. Therefore, research is underway to integrate high-temperature gate drivers with SiC power modules. In [9]–[14], a high-temperature gate driver on a silicon-on-insulator (SOI) process with high-temperature passive components is integrated into the power package to demonstrate the concept. However, they either only implement the basic driving function, or the current sourcing and sinking capabilities are below or around 2 A. In [15], drivers with up to 4 A fixed sourcing and sinking current capacity are reported. This work presents the design of a high-current, non-isolated single-channel gate driver for heterogeneous integration inside a SiC power module with a dynamically adjustable drive strength feature. Active Miller clamping, over-current detection, and under-voltage lockout circuits are also incorporated within the gate driver as system protection features. Special care has been taken to minimize the number of I/O pads while designing the circuits to make the driver die integrable inside the module. Detailed design techniques and preliminary test results of

the fabricated gate driver are presented here. Also, towards the end, a conceptual power module system integration using the die is outlined.

II. Gate Driver Design and Test Results

The gate driver design is realized on XFAB's 180 nm silicon-on-insulator (SOI) CMOS process, which can safely operate up to 175 °C and most likely even beyond this figure to survive at the expected junction temperature inside the module. The following subsections briefly describe the top-level building blocks of the gate driver without elaborating much on the transistor-level circuit design and present some key test results.

A. The Driver Core

The gate driver core consists of four pull-up (PMOS) slices and four pull-down (NMOS) slices placed in parallel as the current sourcing and sinking components. Each slice can be activated individually through a controller block, ensuring a variable drive strength feature for the gate driver. Since the input capacitances of these drive slices are significant due to their relatively larger width, a CMOS buffer chain has been designed to drive these slices. The length of the buffer chain and transistor sizing inside the chain are optimized to reduce the loading effect on the pre-driving circuits, thereby reducing the PWM input to gate driver output propagation delay. Fig. 1 shows the schematic of a single pull-up slice along with its buffer chain. The positive and negative voltage rails for the chain and the drive slice are +15 V and -3 V, respectively. Four parallel pull-up slices driven by buffer chain (to source current to the gate driver output) and four parallel pull-down slices driven by buffer chain (to sink current from the gate driver output) constitute the driver core.

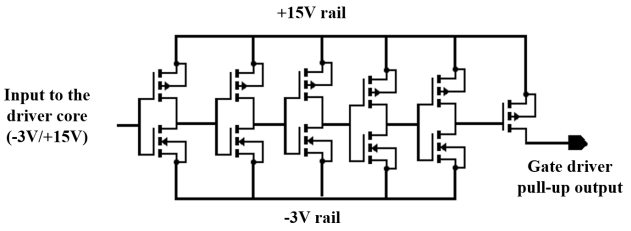

Fig. 1. A single pull-up slice driven by CMOS buffer chain

Fig. 2 shows the block-level schematic of the controller unit. Depending on the magnitude of the analog control voltage it receives, the number of drive slices is activated to facilitate the drive strength variability. The logic block synchronizes the PWM input signal with the output of the converter to ensure the activated PMOS and NMOS drive slices are switching in a complementary fashion, whereas the non-activated drive slices maintain their non-switching states during the gate driver operation. The level shifter generates the +15V/-3V input swing necessary to operate the drive slices inside the driver core. Table I summarizes the triggering voltages for the drive slices. Thus, through two analog voltages, the effective drive strength of the gate driver can be controlled. However, by pulling the control voltage below -2V, the gate driver can be disabled.

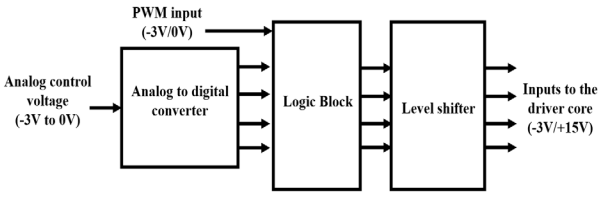

Fig. 2. Block level schematic of the controller unit

TABLE I. TRIGGERING VOLTAGES FOR THE DRIVE SLICES (PMOS AND NMOS)

Control voltage	Number of active drive slices
< -2	0
> -2 & <-1.7	1
> -1.7 & <-1.4	2
> -1.4 & <-1.1	3
> -1.1	4

Fig. 3 shows the input-output response of the gate driver under a continuous pulse train, whereas Table II summarizes the gate driver's performance both at room temperature and at an elevated temperature of 175°C. The driver's performance degrades a bit as we go up in temperature. This is due to the decreased carrier mobility at higher temperatures, an intrinsic property of the SOI process. However, the robust operation of this driver even at 175°C puts it much ahead of its silicon (Si) counterparts.

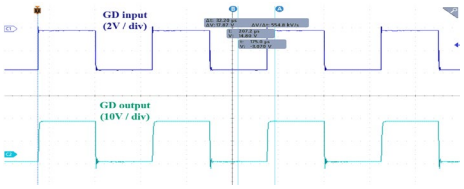

Fig. 3. Input-output response of the gate driver under continuous pulse train.

TABLE II. PERFORMANCE FIGURES OF THE GATE DRIVER

Test Condition	Parameter	Measured Value (25°C)	Measured Value (175°C)
R_g = 1.2 Ω , C_{load} = 16 nF Gate driver in full drive strength	Output voltage swing	+ 15 V / - 3 V	+ 15 V / - 3 V
	Peak source / sink current	4.15 A / 6.38 A	4.01 A / 6.06 A
	Rise time	272 ns	298 ns
	Fall time	163 ns	179 ns

The load is equivalent to two CPM3-1200-0013 power die placed in parallel inside the module (an illustrative power module that the gate drive aims to drive).

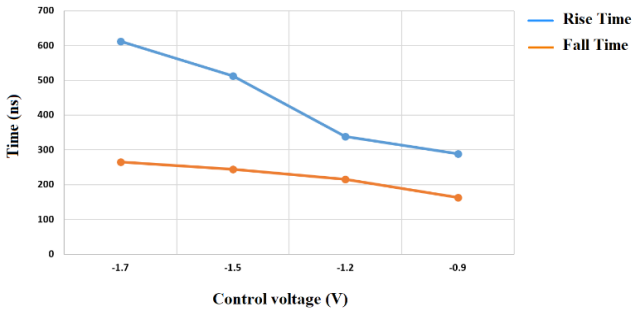

Fig. 4. Varying rise and fall times at room temperature with external control voltage having same loading condition as Table II.

B. *Active Miller Clamp*

Due to its faster switching speed, one of the common problems when operating a SiC power module is parasitic turn-on due to the gate-drain coupling through the Miller capacitor. In such a case, a high dv/dt transient created during MOSFET turn-off can induce a gate voltage spike (parasitic turn-on), which can cause potential damage to the module. Fig. 5 shows the block-level schematic of the active Miller clamping circuit with all its major components integrated with the gate driver to mitigate such phenomena. The clamp switch is an NFET switch. Its drain is connected to the Power-FET gate so that any unwanted current spike at this node when the gate driver steadily turns off the Power-FET gate can be discharged through the switch, bypassing the gate resistor, thus avoiding any spurious voltage spike. The active Miller clamp controller block using a feedback mechanism technique ensures proper timing between the clamp switch activation signal and the gate driver output.

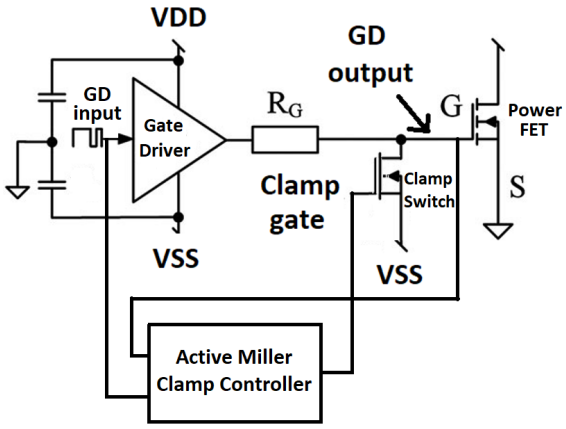

Fig. 5. Block level schematic of the active Miller clamping circuit

During the 'turn on' transition state, it ensures the clamp switch gets deactivated first so that all the source current provided by the driver is used to charge the power-FET gate without leaking through the clamp switch. During the 'turn off' transition state, however, it ensures that the power-FET gate is discharged through the gate driver path first. Once the gate driver output gets low, the clamp switch is activated, holding the power-FET gate firmly to the negative reference voltage to allow any unwanted current spike to be discharged through it. Fig. 6 shows this timing sequence.

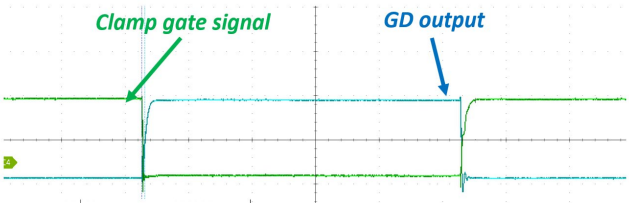

Fig. 6. Active Miller clamp switching timing

C. *Under-voltage lockout (UVLO)*

An under-voltage lockout (UVLO) circuit is also integrated into the gate driver to ensure the system is guarded against bias supply failure. If the turn-on voltage for the SiC FET gets low, it can undergo significant conduction losses and thermal dissipation. As shown in Fig. 7, the UVLO output goes high if the positive power supply falls below ~ 9.5 V, indicating the gate driver turn-on voltage is too low. Once the power supply goes above ~ 10 V, the UVLO output goes low (around 500 mV in the hysteresis loop).

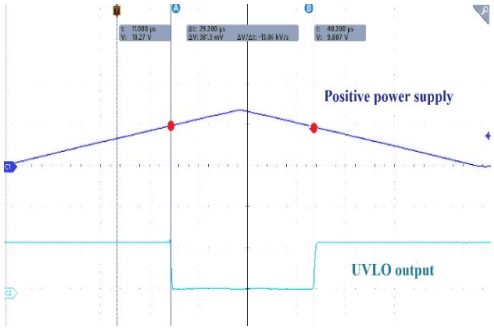

Fig. 7. UVLO functionality test results

D. *Over-current detection*

A desaturation detection circuit is also integrated with the gate driver as an overcurrent protection feature for the power module. For simulation purposes, a simple H-bridge module containing two power die is built in a DPT configuration, as shown in Fig. 8. Manufacturer-provided LTspice models for the CPM3-1200-0013A power die and the CPW41200S002B diode are used for simulation.

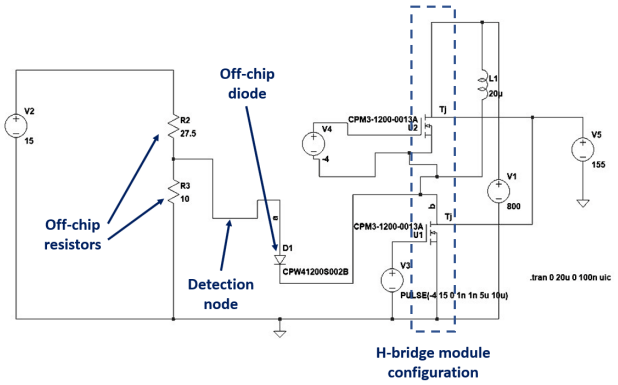

Fig. 8. LTspice testbench to demonstrate desaturation detection feature

The simulation results in Fig. 9 show that the detection node voltage increases with increasing current through the lower switch and clips at 4 V once it goes above 175 A (putting the diode in reverse biased condition). Thus, an on-chip comparator with one of its inputs referenced to 3 V and the other input connected to the detection node can set the maximum current limit through the switch to 113A. However, this threshold can be altered by varying the reference voltage and off-chip resistor values. Fig. 10 shows the block-level schematic of the desaturation detection scheme integrated inside the chip. The level shifter block shifts down the detection node voltage into the appropriate input voltage range required for the comparator referenced to a voltage level. The detection block waits for a specific time from the rising edge of the gate driver output. If the detection node voltage does not go below the reference voltage within this time range (indicating continuous overcurrent flow), it sets the overcurrent detection pin high.

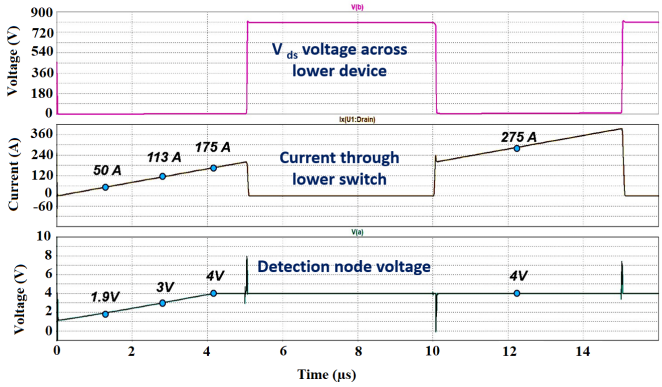

Fig. 9. Simulation results of the LTspice test bench

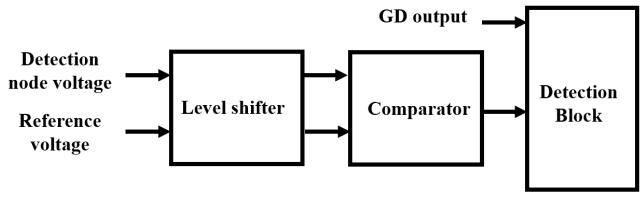

Fig. 10. Block level schematic of the desaturation detection scheme

To evaluate the functionality of the desaturation detection block, a detection node voltage swinging between 2 V and 4 V has been generated externally. The following sections briefly describe different cases during power module switching operations and how the desaturation detection block responds to them. The first case is the normal switching operation of the power-FET. Here, the gate driver output goes from low to high, and V_{ds} voltage goes down. If no overcurrent occurs, the detection node voltage should also go down to the reference voltage. The detection block waits for a certain delay time (~2 us in this case) for this voltage to go below the reference voltage. If it does, it will indicate a normal V_{ds} discharge, and the desat output will stay low. This case is demonstrated in Fig. 11(a).

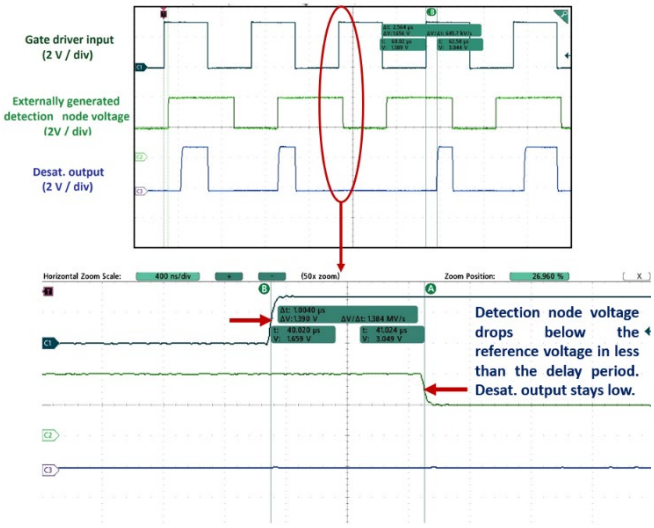

Fig. 11(a). Demonstration of desaturation detection (case 1)

If the detection node voltage stays above the reference voltage for more than this delay time, it will indicate an overcurrent flow, and the desat output goes high, indicating a faulty condition. This is illustrated in Fig. 11(b).

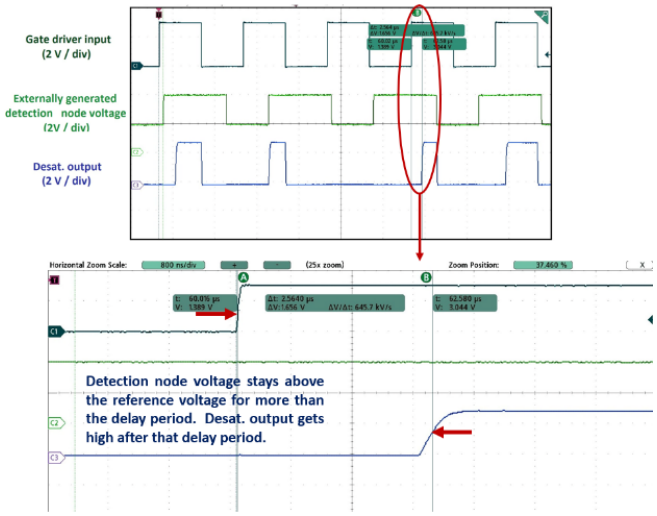

Fig. 11(b). Demonstration of desaturation detection (case 2)

A special case might occur when the normal V_{ds} discharge occurs and then suddenly the detection node voltage goes above the reference voltage, indicating a sudden overcurrent due to short-circuits or some other reason. In this case, the desat output goes high immediately, as demonstrated in Fig. 11 (c).

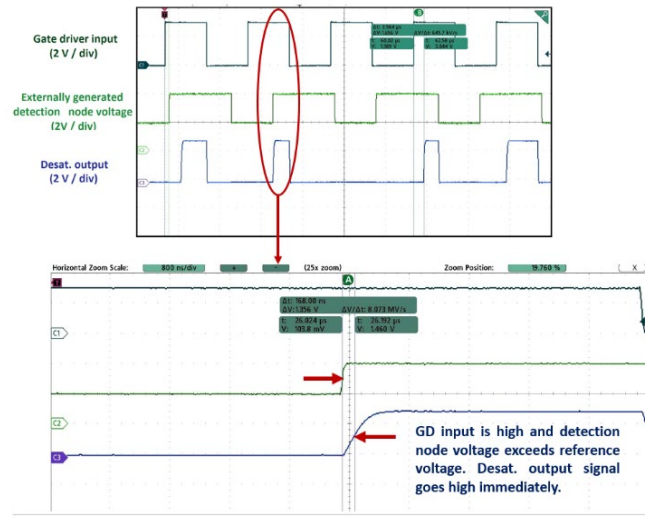

Fig. 11(c). Demonstration of desaturation detection (case 3)

III. Gate Driver Die Packaging and Module Integration

Fig. 12 shows the bare die micrograph of the fabricated SOI gate driver. The die area is approximately 5.4 mm by 3.3 mm. Fig. 13 shows the isometric view of the power module integrable PCB that accommodates the driver die. High-temperature non-conductive epoxy is used for die attach, whereas high-temperature Rogers 4350B material is used for PCB fabrication with all its pad electroless nickel immersion gold (ENIG) platted to facilitate 25 µm Al wire bonds. Connections are made directly from the die pad to the exposed pads on the PCB. The driver die can then be electrically operated through the input and control ports placed at the edge of the PCB, as shown in Fig. 13.

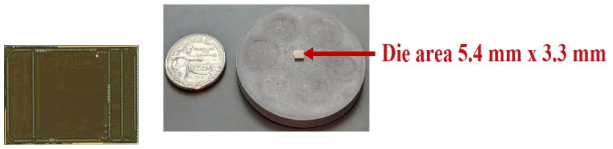

Fig. 12. Die micrograph of the fabricated SOI gate driver

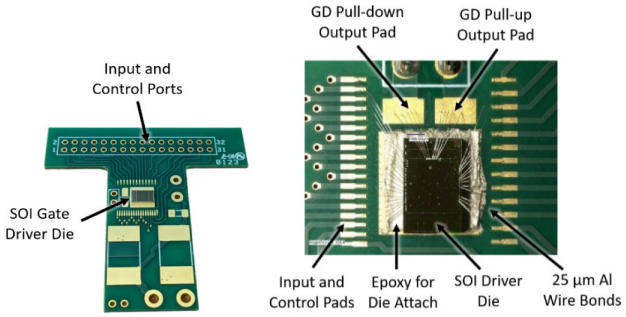

Fig. 13. Fabricated module integrable gate driver PCB

Fig. 14 shows the conceptual diagram of a half-bridge power module where this driver PCB can be integrated. For the sake of simplicity, only the bottom switch substrate of the power module and the driving PCB are shown. A similar configuration can be assembled for the top switch on the other side (left side).

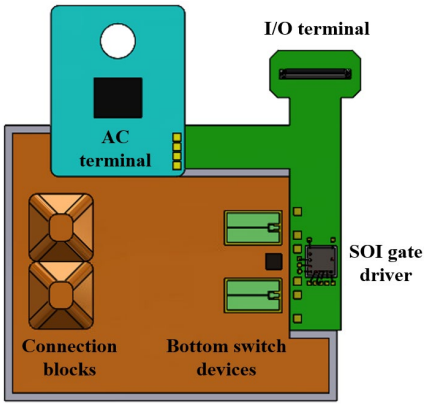

Fig. 14. Conceptual power module system integration

IV. Conclusion

In this work, the design technique and test results of a high-temperature non-isolated single-channel gate driver on a 180 nm SOI CMOS process for heterogeneous integration inside a SiC power module are presented. Two separate analog control voltages can control the driver's active pull-up and pull-down strengths, thus minimizing the I/O pads for this feature. Active Miller clamping, over-current detection, and under-voltage lockout circuits are also incorporated within the gate driver as system protection features. Such heterogeneous integration not only increases the system reliability by reducing the gate loop inductance but also helps improve the power density significantly by integrating the gate driver and the auxiliary protection circuitry into a single chip. Additionally, the SOI process gives them endurance at the anticipated elevated ambient temperature as they are positioned so near to the power die inside the module.

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